Solución Exámen Diseño Lógico Diciembre 2014

Ejercicio 1

a) 8 bits, se puede representar desde el -128 al +127

b) A = 37 = 00100101
B = 126 = 01111110
-C = 73 = 01001001
C = 10110110 + 1 = 10110111

c) X = A + B = 00100101 + 01111110 = 10100011
---- Hay overflow, sumo dos positivos y da resultado negativo

Y = A - C = A + (-C) = 00100101 + 01001001 = 01101110
---- No hay overflow, suma de dos positivos, resultado positivos

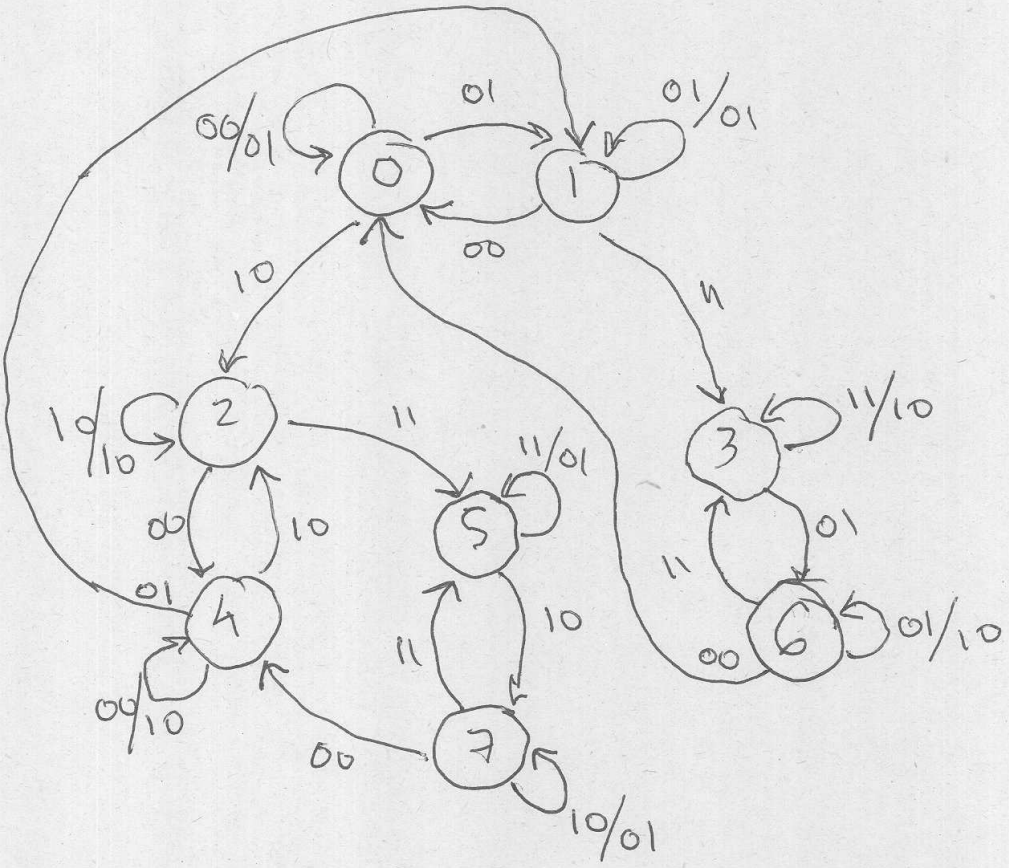
Z = B + C = 01111110 + 10110111 = 1 00110101
Z = 00110101
---- No hay overflow, la suma de un positivo más un negativo siempre da resultado válido

Ejercicio 2

a) T1 = tdmax + tnotmax + tselmax + tsu
T2 = tdmax + txormax + tmuxmax + tsu

b) X a D antes del flanco, el peor caso es el camino por el exor y el mux (el otro camino es solo por el mux)
Ta = txormax + tmuxmax + tsu

X a D después del flanco, el peor caso es el más corto, porque cuanto más rápido cambie más exigente para el thold, eso el camino por el mux con tiempo mínimo
Tb = th - tmuxmin


00/01
01
01/01
0
1
00
10
11
10/10
2
11
11/01
3
11/10
00
10
5
01
11
01
4
10
6
01/10
11
00
00/10
00
7
10/01

$x_1 x_0 / z_1 z_0$

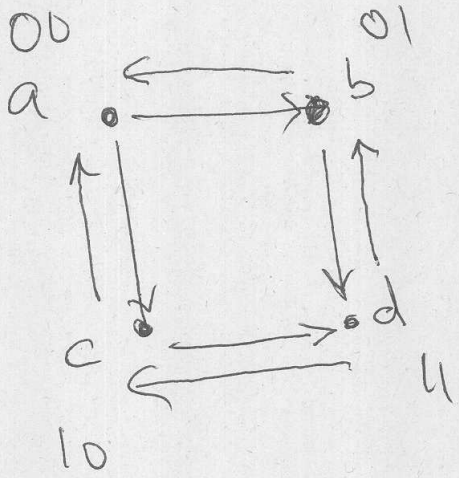
	00	01	11	10	00	01	11	10
0	0	1		2	01			
1	0	1	3			01		
2	4		5	2				10
3		6	3	7			10	
4	4	1		2	10			
5		6	5	7			01	
6	0	6	3			10		
7	4		5	7				01

1	✓					
2	~~04~~	~~04~~				
3	~~16~~	~~16~~	~~35~~ ~~27~~			
4	X	~~04~~	✓	~~16~~ ~~27~~		
5	~~16~~	~~16~~	~~27~~	X	~~16~~ ~~27~~	
6	~~16~~	X	~~04~~ ~~35~~	✓	~~04~~ ~~16~~	~~35~~
7	~~04~~	~~04~~	X	~~35~~	~~27~~	✓ ~~04~~
	0	1	2	3	4	5

a b c d

(01) (24) (36) (57)

		00	01	11	10	00	01	11	10
00	a	a	a	c	b	01	01	XX	XX
01	b	b	a	d	b	10	XX	XX	10
10	c	a	c	c	d	XX	10	10	XX
11	d	b	c	d	d	XX	XX	01	01



Se eliminan las carreras codificando

y_1y_0 \ x_1x_0	00	01	11	10				
a 00	00	00	10	01	01	01	xx	xx
b 01	01	00	11	01	10	xx	xx	10
d 11	01	10	11	11	xx	xx	01	01
c 10	00	10	10	11	xx	10	10	xx

0	0	1	0
0	0	1	0
0	1	1	1
0	1	1	1

$Y_1 = x_1x_0 + y_1x_0 + y_1x_1$

0	0	0	1
1	0	1	1
1	0	1	1
0	0	0	1

$Y_0 = x_1\bar{x}_0 + y_0x_1 + y_0\bar{x}_0$

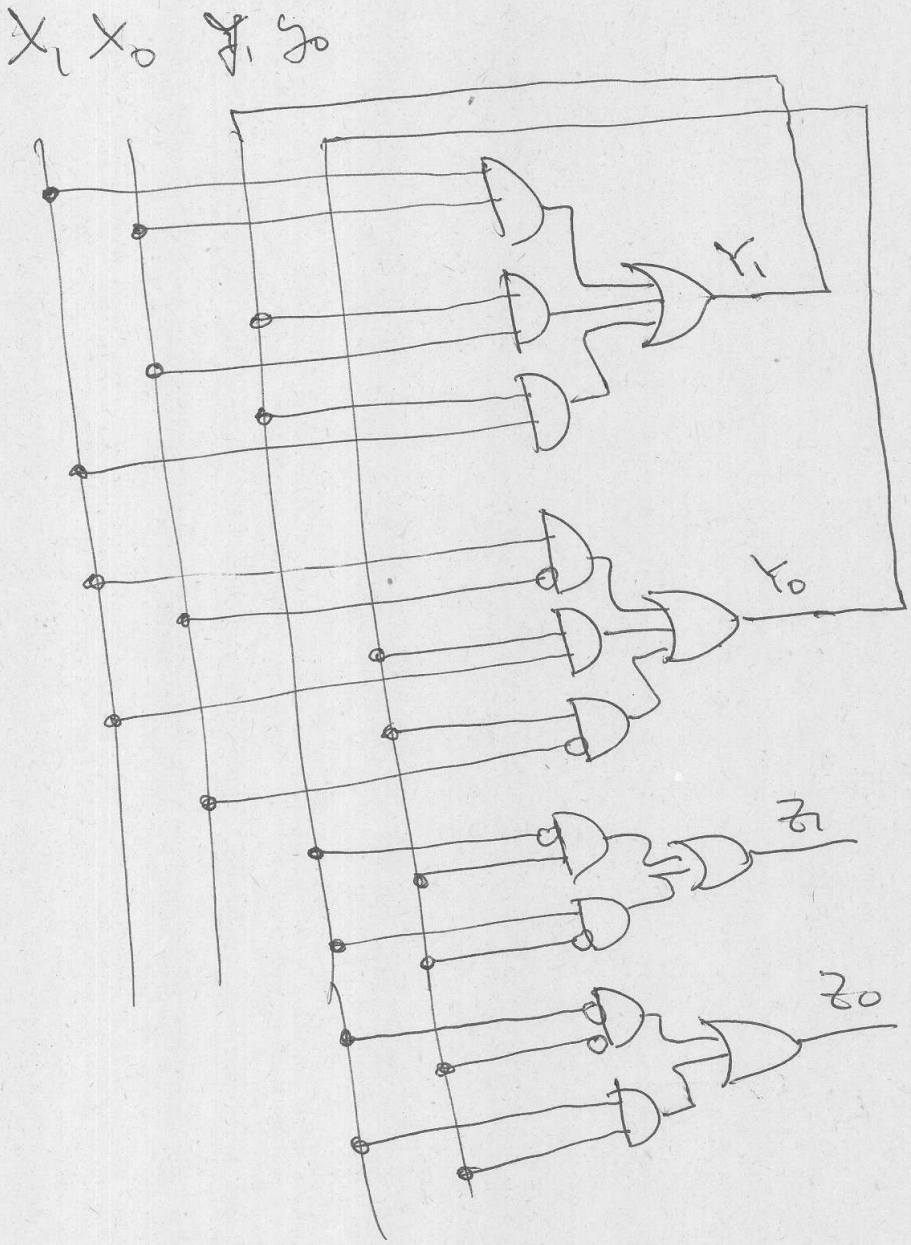
0	0	x	x
1	x	x	1
x	x	0	0
x	1	1	x

$Z_1 = \bar{y}_1y_0 + y_1\bar{y}_0$

1	1	x	x
0	x	x	0
x	x	1	1
x	0	0	x

$Z_0 = \bar{y}_1\bar{y}_0 + y_1y_0$

Se cumple además que $Z_1 = \bar{Z}_0$

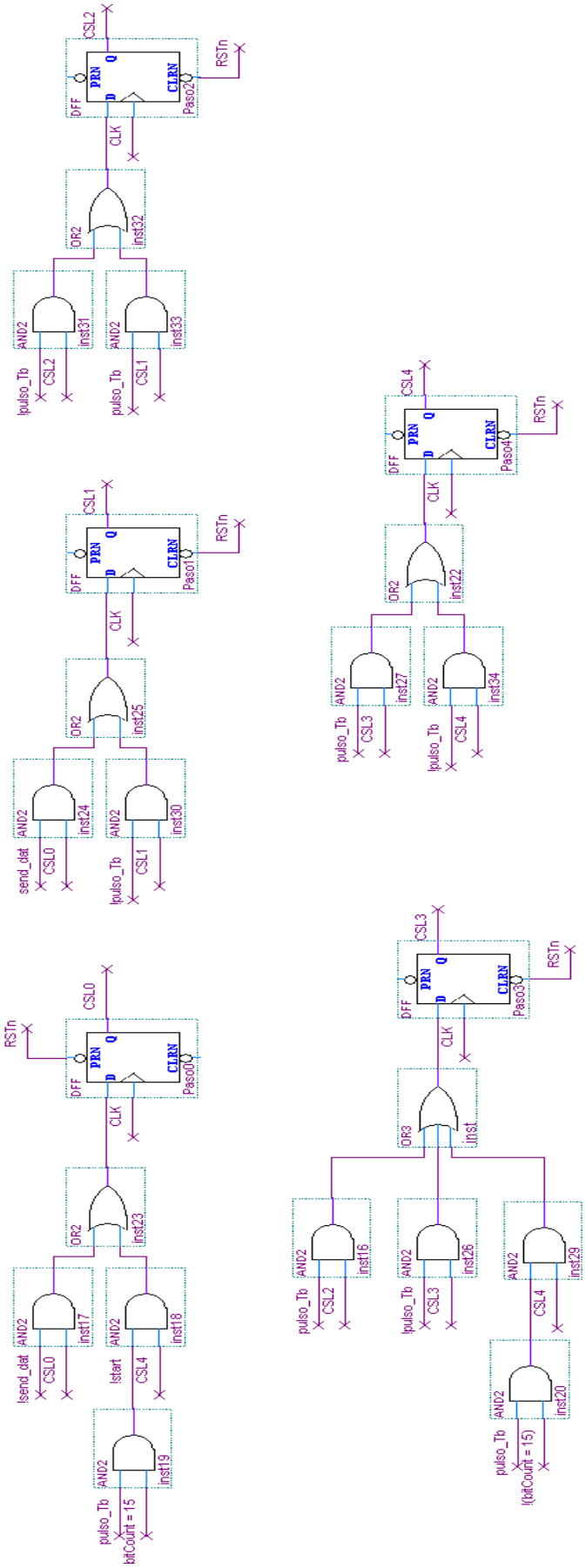
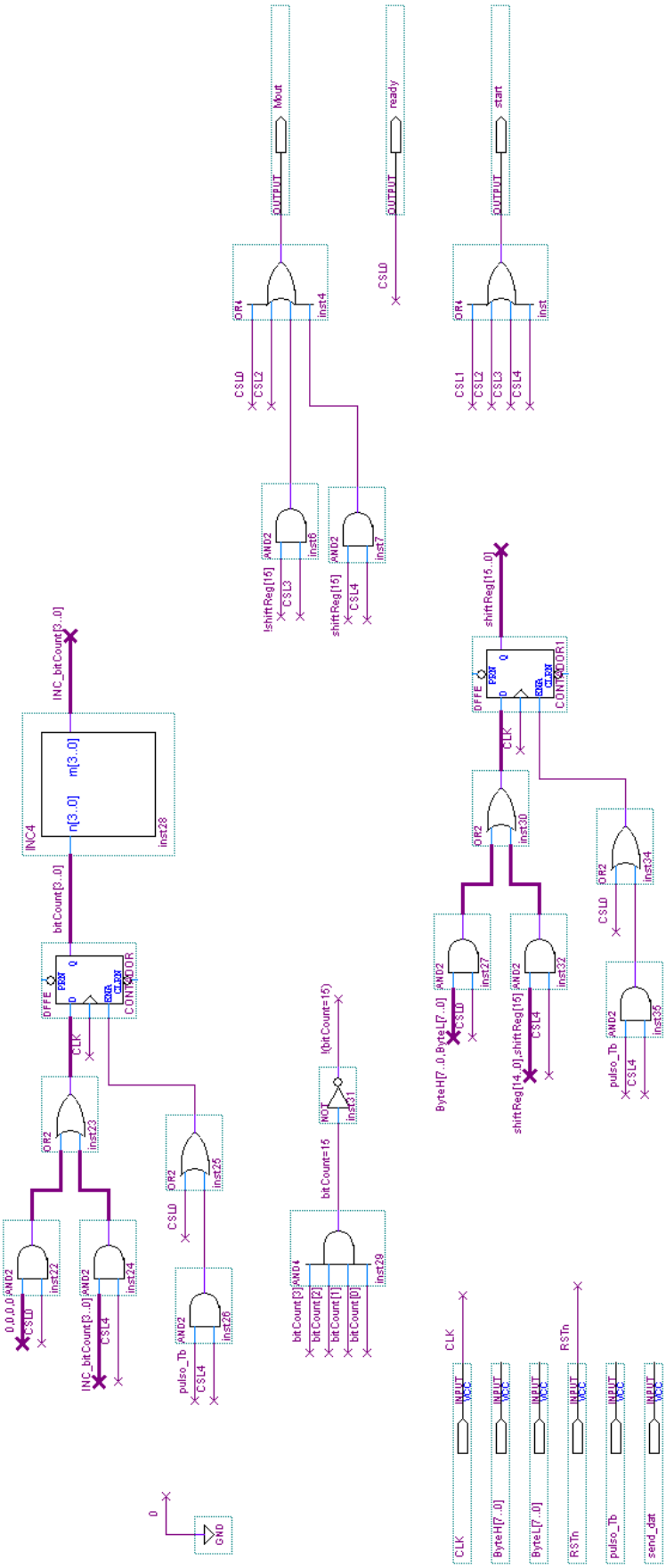

x_1 x_0 y_1 y_0
r_1
r_0
z_1
z_0

Solución Problema 2

Secuencia

```
Module: ExDic14
Inputs: ByteH[7:0], ByteL[7:0], send_data, pulso_Tb
Outputs: Mout, ready, start
Memory: bitCount[3:0], shift_reg[15:0]

0. ; espero send_data
   bitCount[3..0] <- 0
   shift_reg [15:8] <- ByteH[7..0],ByteL[7..0]
   ready = 1
   Mout = 1
   -> (send_data,!send_data)/(1,0)

1. ; start bit parte 1
   Mout = 0
      start = 1
   -> (pulso_Tb,!pulso_Tb)/(2,1)

2. ; start bit parte 2
   Mout = 1
      start = 1
   -> (pulso_Tb,!pulso_Tb)/(3,2)

3. ; bit datos parte 1
   Mout = !shift_reg[15] ; si bit a transmitir 1, 1er 1/2 bit debe ser 0
      start = 1
   -> (pulso_Tb,!pulso_Tb)/(4,3)

4. ; bit datos parte 2
      start = 1
   Mout = shift_reg[15] ; si bit a transmitir 1, 2do 1/2 bit debe ser 1
   bitCount[3..0] * pulsoTb <- INC(bitCount[3..0])
   shift_reg[15..0] * pulsoTb <- shift_reg[14:0],shift_reg[15]
   -> (pulso_Tb.(bitCount = 15), pulso_Tb.!(bitCount=15)),!pulso_Tb)/(0,3,4)

End Sequence
Control Reset(0)
End
```

Bloque de Control



Bloque de Datos