

Type	ID	Message
> i		Running Quartus II 64-Bit Analysis & Synthesis
i		Command: quartus_map --read_settings_files=on --write_settings_files=off Lab1a -c Lab1a
w	20028	Parallel compilation is not licensed and has been disabled
> i	12021	Found 1 design units, including 1 entities, in source file lab1a.bdf
i	12127	Elaborating entity "Lab1a" for the top level hierarchy

- i 12127 Elaborating entity "Lab1a" for the top level hierarchy
- x 275028 Bus name allowed only on bus line -- pin "SW[3..0]"
- x 275028 Bus name allowed only on bus line -- pin "Disp[6..0]"
- x 12153 Can't elaborate top-level user hierarchy

Flow Summary	
Flow Status	Flow Failed - Wed Aug 31 16:25:49 2022
Quartus II 64-Bit Version	13.1.0 Build 162 10/23/2013 SJ Web Edition
Revision Name	Lab1a
Top-level Entity Name	Lab1a
Family	Cyclone III
Device	EP3C16F484C6
Timing Models	Final
Total logic elements	N/A until Partition Merge
Total combinational functions	N/A until Partition Merge
Dedicated logic registers	N/A until Partition Merge
Total registers	N/A until Partition Merge
Total pins	N/A until Partition Merge
Total virtual pins	N/A until Partition Merge
Total memory bits	N/A until Partition Merge
Embedded Multiplier 9-bit elements	N/A until Partition Merge
Total PLLs	N/A until Partition Merge