FLEX 10K

Embedded Programmable Logic Family

June 1996, ver. 2 Data Sheet

Features...

Preliminary Information

- The industry's first embedded programmable logic device (PLD) family, providing system integration in a single device
  - Embedded array for implementing megafunctions, such as efficient memory and specialized logic functions
  - Logic array for general logic functions
- High density
  - 10,000 to 100,000 typical gates (see Table 1)
  - 720 to 5,392 registers
  - 6,144 to 24,576 RAM bits, all of which can be used without reducing logic capacity
- System-level features
  - ClockLock and ClockBoost option for reduced clock delay/skew and clock multiplication
  - In-circuit reconfigurability (ICR) via external configuration EPROM, intelligent controller, or Joint Test Action Group (JTAG) port
  - Fully compliant with the peripheral component interconnect (PCI) standard
  - Built-in JTAG boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990
  - 3.3- or 5.0-V I/O pins on all devices in pin-grid array (PGA), ball-grid array (BGA), and 208-pin quad flat pack (QFP) packages
  - Able to bridge between 3.3-V and 5.0-V systems
  - Low power consumption (less than 1 mA in standby mode)

Table 1. FLEX 10K Device Features

Feature	EPF10K10	EPF10K20	EPF10K30	EPF10K40	EPF10K50	EPF10K70	EPF10K100
Typical gates (logic & RAM)	10,000	20,000	30,000	40,000	50,000	70,000	100,000
Usable gates	7,000 to 31,000	15,000 to 63,000	22,000 to 69,000	29,000 to 93,000	36,000 to 116,000	46,000 to 118,000	62,000 to 158,000
Logic elements	576	1,152	1,728	2,304	2,880	3,744	4,992
Logic array blocks	72	144	216	288	360	468	624
Embedded array blocks	3	6	6	8	10	9	12
Total RAM bits	6,144	12,288	12,288	16,384	20,480	18,432	24,576
Flipflops	720	1,344	1,968	2,576	3,184	4,096	5,392
Max. user I/O pins	134	189	246	189	310	358	406

...and More Features

- Flexible interconnect
  - FastTrack Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions
  - Tri-state emulation that implements internal tri-state nets
  - Up to six global clock signals and four global clear signals
- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Open-drain option on each I/O pin
  - Programmable output slew-rate control to reduce switching noise
- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Flexible package options
  - Available in a variety of packages with 84 to 503 pins (see Table 2)
  - Pin-compatibility with other FLEX 10K devices in the same package
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS II development system for 486- and Pentium-based PCs and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, VeriBest, and Viewlogic

Table 2. FLEX 10K Package Options & I/O Count *Note (1)*

Device	84-Pin PLCC	144-Pin TQFP	208-Pin PQFP & RQFP	240-Pin RQFP	356-Pin BGA	403-Pin PGA	503-Pin PGA
EPF10K10	59	107	134				
EPF10K20			147	189			
EPF10K30			147	189	246		
EPF10K40			147	189			
EPF10K50				189	274	310	
EPF10K70				189			358
EPF10K100							406

Note:
(1) Contact Altera for up-to-date information on package availability.

General Description

Altera's FLEX 10K devices are the industry's first embedded PLDs. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions. With up to 100,000 gates, the FLEX 10K family provides the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device. Table 3 shows FLEX 10K performance for typical applications, as well as the logic elements (LEs) and the embedded array blocks (EABs) required.

Table 3. FLEX 10K Performance

Application	Resources Used		Performance			Unit
	LEs	EABs	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade *Note (1)*	
16-bit loadable counter	16	0	104	97	67	MHz
16-bit accumulator	16	0	104	97	67	MHz
16-to-1 multiplexer, *Note (2)*	10	0	9.4	10.6	13.2	ns
4 × 4 multiplier, *Note (3)*	0	1	105	86	66	MHz
8 × 8 multiplier, *Note (3)*	25	4	30	24	18	MHz
256 × 8 RAM, *Note (3)*	0	1	105	86	66	MHz

Notes:
(1) The -5 speed grade is available for EPF10K50 devices only.
(2) This application uses combinatorial inputs and outputs.
(3) This application uses registered inputs and outputs.

The FLEX 10K architecture is similar to that of embedded gate arrays, the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional "sea-of-gates" architecture. In addition, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays provide reduced die area and increased speed compared to standard gate arrays. However, the embedded megafunctions typically cannot be customized, limiting the designer's options. In contrast, FLEX 10K devices are programmable, providing the designer with full control over embedded megafunctions and general logic while facilitating iterative design changes during debugging.

Each FLEX 10K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide data-path manipulation, and data transformation functions. The logic array performs the same function as the sea-of-gates in the gate array: it is used to implement general logic, such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10K devices are configured at system power-up with data stored in an Altera serial Configuration EPROM device or provided by a system controller. Altera offers the EPC1 Configuration EPROM, which configures FLEX 10K devices via a serial data stream. Configuration data can also be downloaded from system RAM or from Altera's BitBlaster serial download cable. After a FLEX 10K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 200 ms, real-time changes can be made during system operation.

FLEX 10K devices contain an optimized microprocessor interface that permits the microprocessor to configure FLEX 10K devices serially, in parallel, synchronously, or asynchronously. The interface also enables the microprocessor to treat a FLEX 10K device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to reconfigure the device.

Go to the *Configuration EPROMs for FLEX Devices Data Sheet* in this data book and *AN 59 (Configuring FLEX 10K Devices)* for more information.

FLEX 10K devices are supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; full simulation and worst-case timing analysis; and device configuration. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

Go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book for more information.

Functional Description

Each FLEX 10K device contains an embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 2,048 bits, which can be used to create RAM, ROM, FIFO functions, or dual-port RAM. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

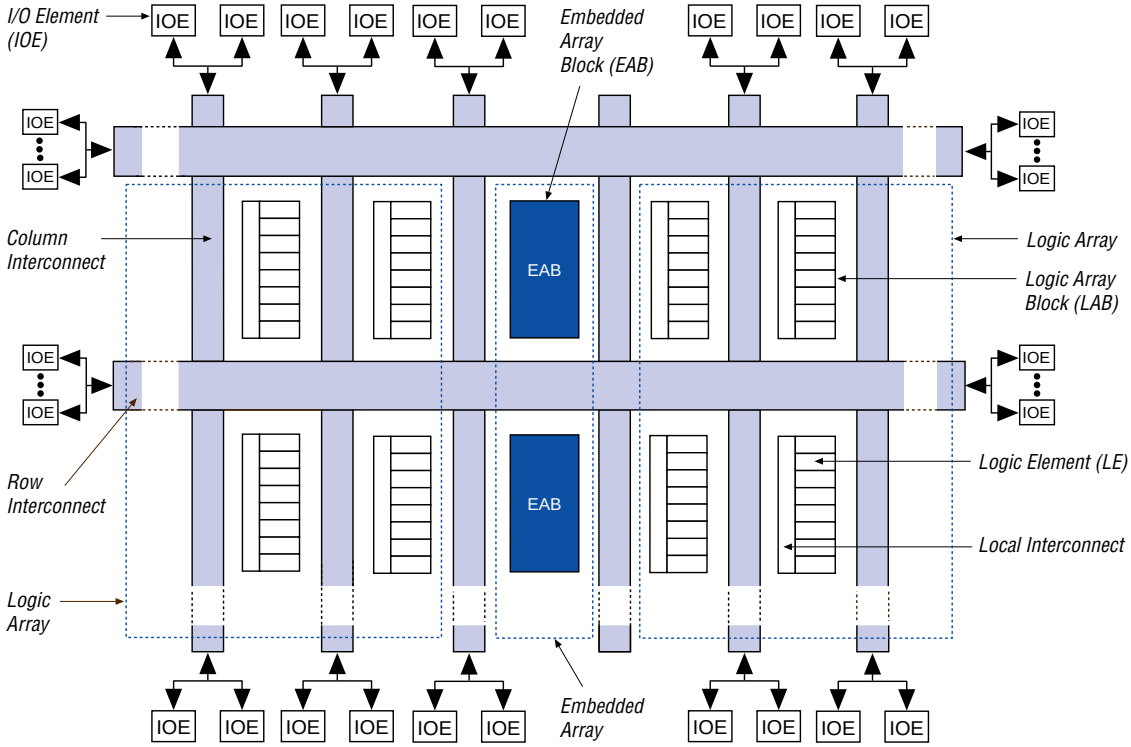
The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10K devices, and to and from device pins, are provided by the FastTrack Interconnect, a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times of less than 8 ns and hold times of 0 ns; as outputs, these registers provide clock-to-output times of less than 8 ns. IOEs provide a variety of features, such as JTAG programming support, slew-rate control, tri-state buffers, and open-drain outputs.

Figure 1 shows a block diagram of the FLEX 10K architecture. Each group of LEs is combined into an LAB; LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect. IOEs are located at the end of each row and column of the FastTrack Interconnect.

Figure 1. FLEX 10K Device Block Diagram



FLEX 10K devices provide six dedicated inputs that drive the control inputs of the flipflops to ensure the efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

Embedded Array Block

The EAB facilitates the implementation of common gate array megafunctions. The EAB is a flexible block of RAM with registers on the input and output ports. However, the size and flexibility of the EAB make it suitable for more than memory, including functions such as multipliers, vector scalars, and error correction circuits. These functions can be combined in applications such as digital filters and microcontrollers.

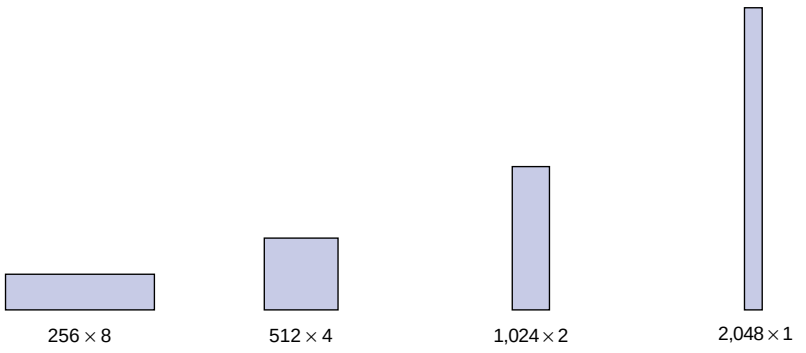
Logic functions are implemented by programming the EAB with a read-only pattern during configuration, creating a large LUT. In this LUT, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions is faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enable designers to implement complex functions in one logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement a 4 × 4 multiplier with eight inputs and eight outputs.

The EAB has advantages over FPGAs, which implement blocks of on-board RAM as arrays of small, distributed RAM blocks. These FPGA RAM blocks contain delays that are less predictable as the size of the RAM increases. In addition, FPGA RAM blocks are prone to routing problems because the small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns. Dedicated EABs are easy to use and provide fast, predictable delays.

The EAB can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the write enable (WE) signal of the RAM, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the EAB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. A circuit using the EAB's self-timed RAM need only meet the setup and hold time specifications of the global clock.

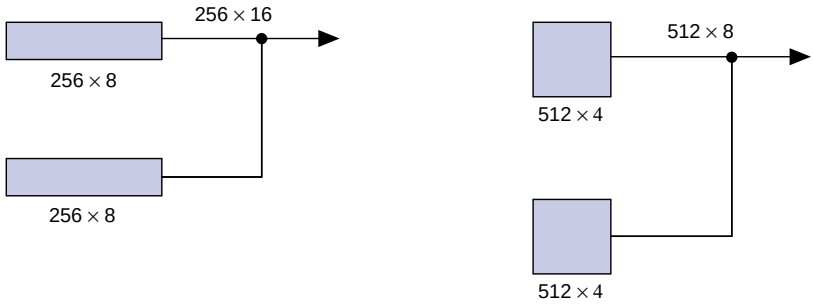
When used as RAM, each EAB can be configured in any of the following sizes: 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. See Figure 2.

Figure 2. EAB Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 8 RAMs can be combined to form a 256 × 16 RAM; two 512 × 4 blocks of RAM can be combined to form a 512 × 8 RAM. If necessary, all EABs in a device can be cascaded to form a single RAM. EABs can be cascaded to form RAMs of up to 2,048 words without impacting timing. Altera's MAX+PLUS II software automatically combines EABs to implement a designer's RAM specifications. See Figure 3.

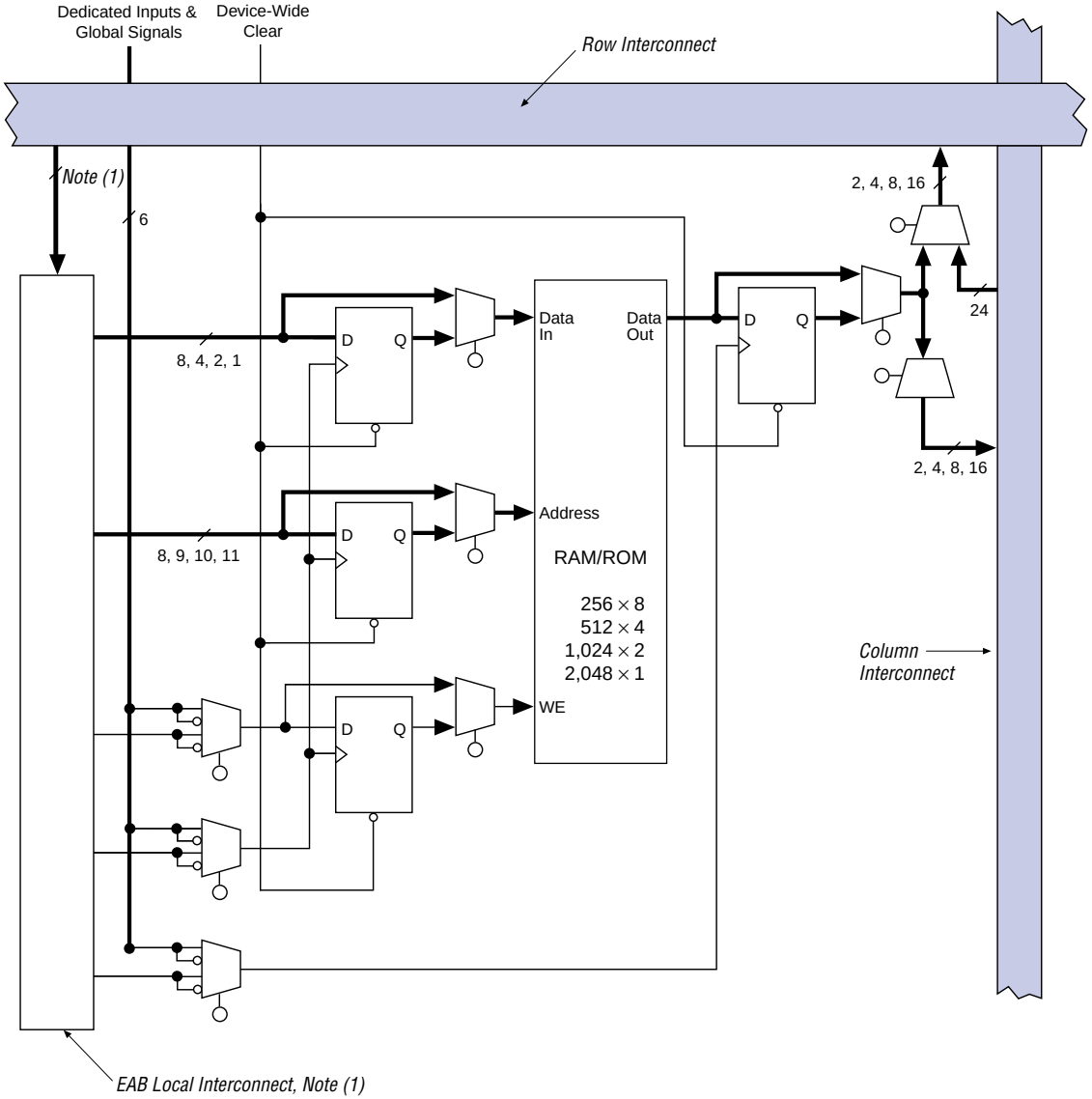
Figure 3. Examples of Combining EABs



The EAB provides flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and WE signals. The global signals and the EAB local interconnect can drive the WE signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the WE signal or the EAB clock signals.

Each EAB is fed by a row interconnect, and can drive out to row and column interconnects. Each EAB output can drive either of two row channels and either of two column channels; the unused row channel can be driven by a column channel. This feature increases the routing resources available for EAB outputs. See Figure 4.

Figure 4. FLEX 10K Embedded Array Block



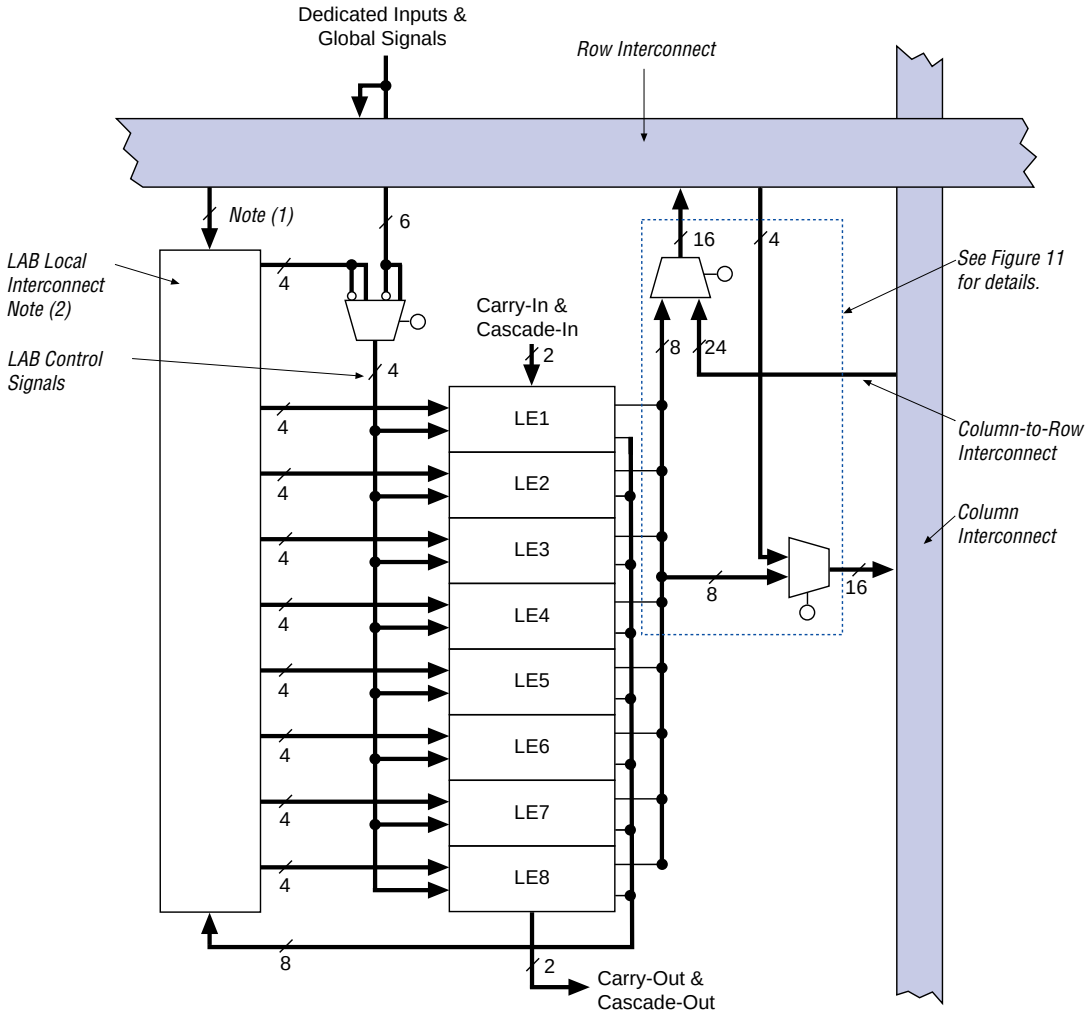
Note:

(1) EPF10K10, EPF10K20, EPF10K30, EPF10K40, and EPF10K50 devices have 22 EAB local interconnect channels; EPF10K70 and EPF10K100 devices have 26.

Logic Array Block

A LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10K architecture, facilitating efficient routing with optimum device utilization and high performance. See Figure 5.

Figure 5. FLEX 10K LAB



Notes:

(1) EPF10K10, EPF10K20, EPF10K30, EPF10K40, and EPF10K50 devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K70 and EPF10K100 devices have 26.

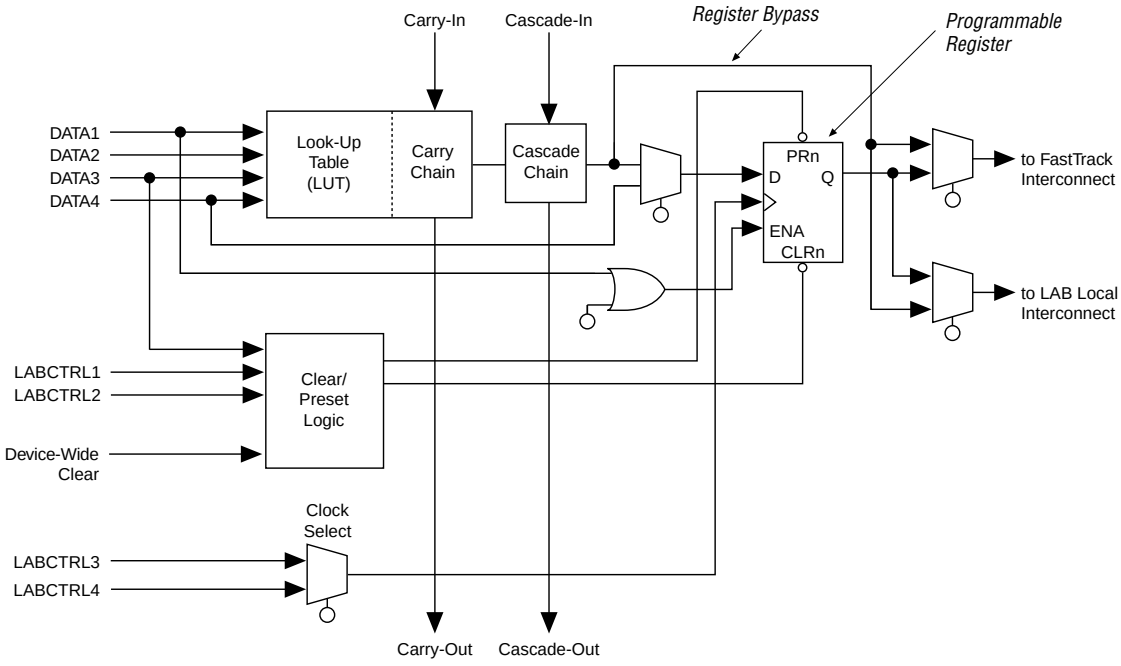
(2) EPF10K10, EPF10K20, EPF10K30, EPF10K40, and EPF10K50 devices have 30 LAB local interconnect channels; EPF10K70 and EPF10K100 devices have 34.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated using LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10K architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect. See Figure 6.

Figure 6. FLEX 10K Logic Element



The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the output of the LE.

The LE has two outputs that drive the interconnect; one drives the local interconnect and the other drives either the row or column FastTrack Interconnect. The two outputs can be controlled independently; for example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

The FLEX 10K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

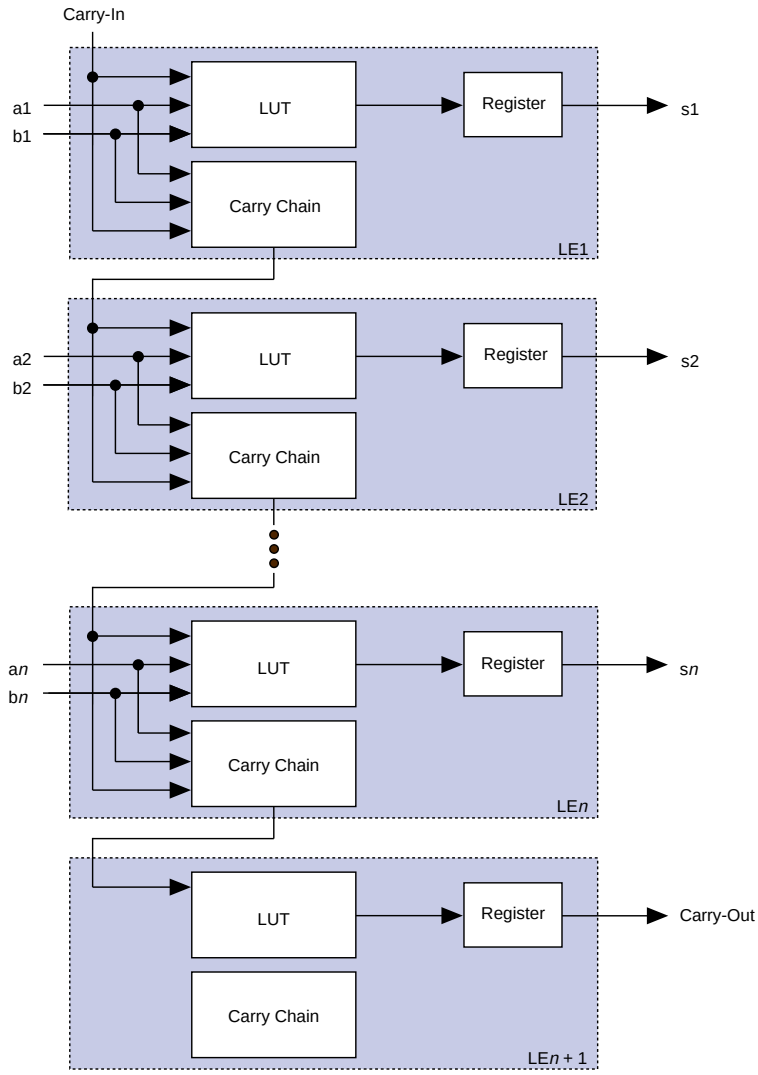
Carry Chain

The carry chain provides a very fast (less than 0.5 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 10K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the MAX+PLUS II Compiler during design processing, or manually by the designer during design entry.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. The last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For example, in the EPF10K50, the carry chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB.

Figure 7 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register is typically bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 7. Carry Chain Operation



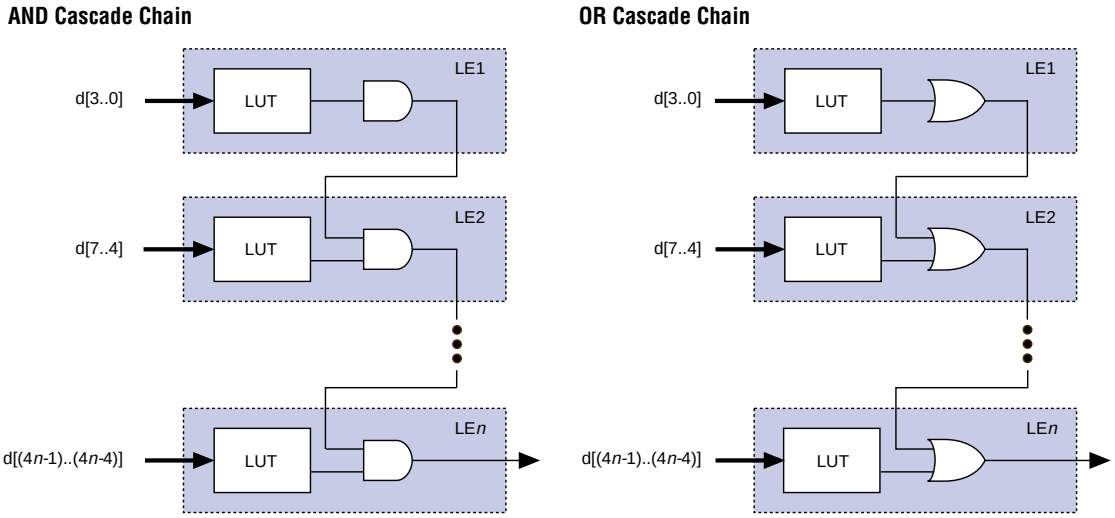
Cascade Chain

With the cascade chain, the FLEX 10K architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 1.1 ns per LE. Cascade chain logic can be created automatically by the MAX+PLUS II Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are automatically implemented by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. The last LE of the first LAB in a row cascades to the first LE of the third LAB. The cascade chain does not cross the center of the row. For example, in the EPF10K50, the cascade chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB. This break is due to the EAB's placement in the middle of the row.

Figure 8 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. The LUT delay is approximately 3.0 ns; the cascade chain delay is 1.1 ns. With the cascade chain, 6.3 ns is needed to decode a 16-bit address.

Figure 8. Cascade Chain Operation



LE Operating Modes

The FLEX 10K LE can operate in one of the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

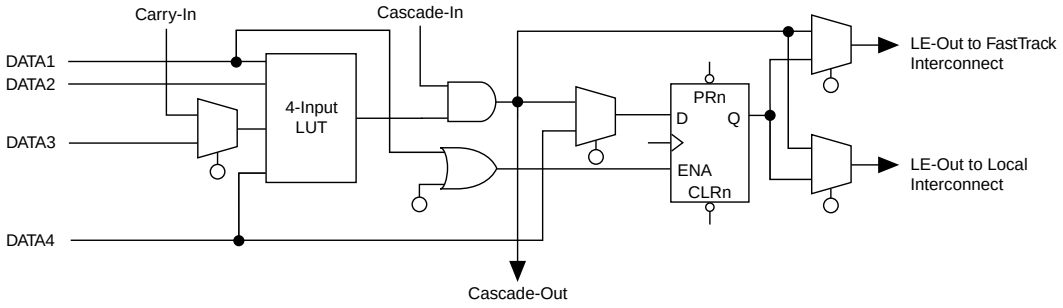
Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can be further enhanced by tailoring the design for the operating mode that supports the intended application.

The architecture provides a synchronous clock enable to the register in all four modes. `DATA1` can be set to synchronously enable the register, providing easy implementation of fully synchronous designs.

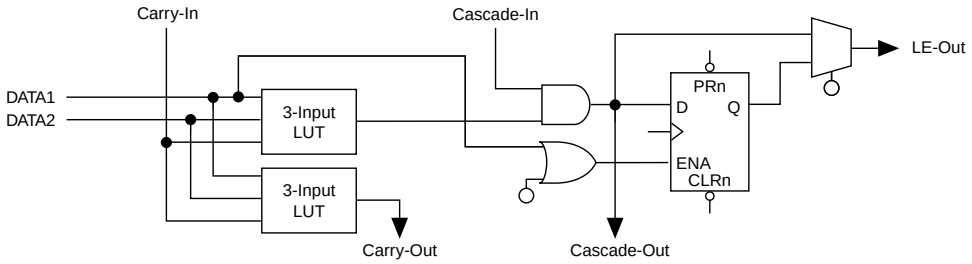
Figure 9 shows the LE operating modes.

Figure 9. FLEX 10K LE Operating Modes

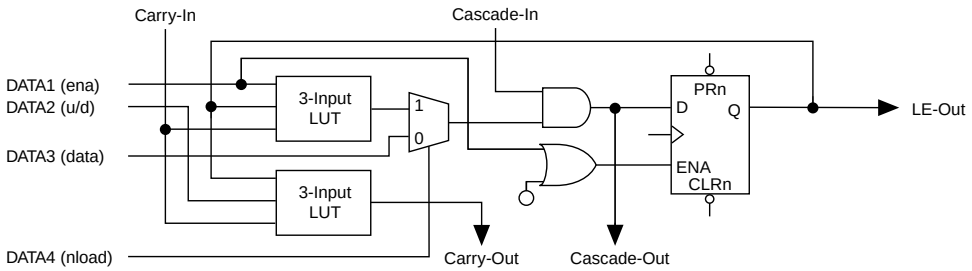
Normal Mode



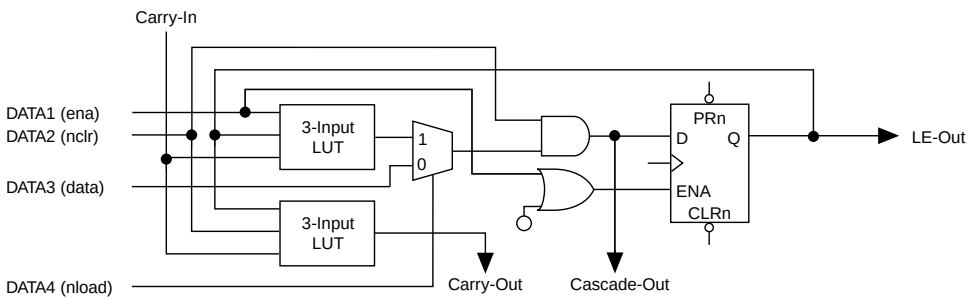
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. To support register packing, the LE has two outputs; one drives the local interconnect and the other drives the FastTrack Interconnect.

The LUT and the register in the LE can be used independently. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect at the same time. Alternatively, in a packed LE, the register can drive the FastTrack Interconnect while the LUT drives the local interconnect, or vice versa.

The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a 3-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a 4-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear and preset signals in the LE.

Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a 3-input function; the other generates a carry output. As shown in Figure 9 on page 46, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. MAX+PLUS II automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. The register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

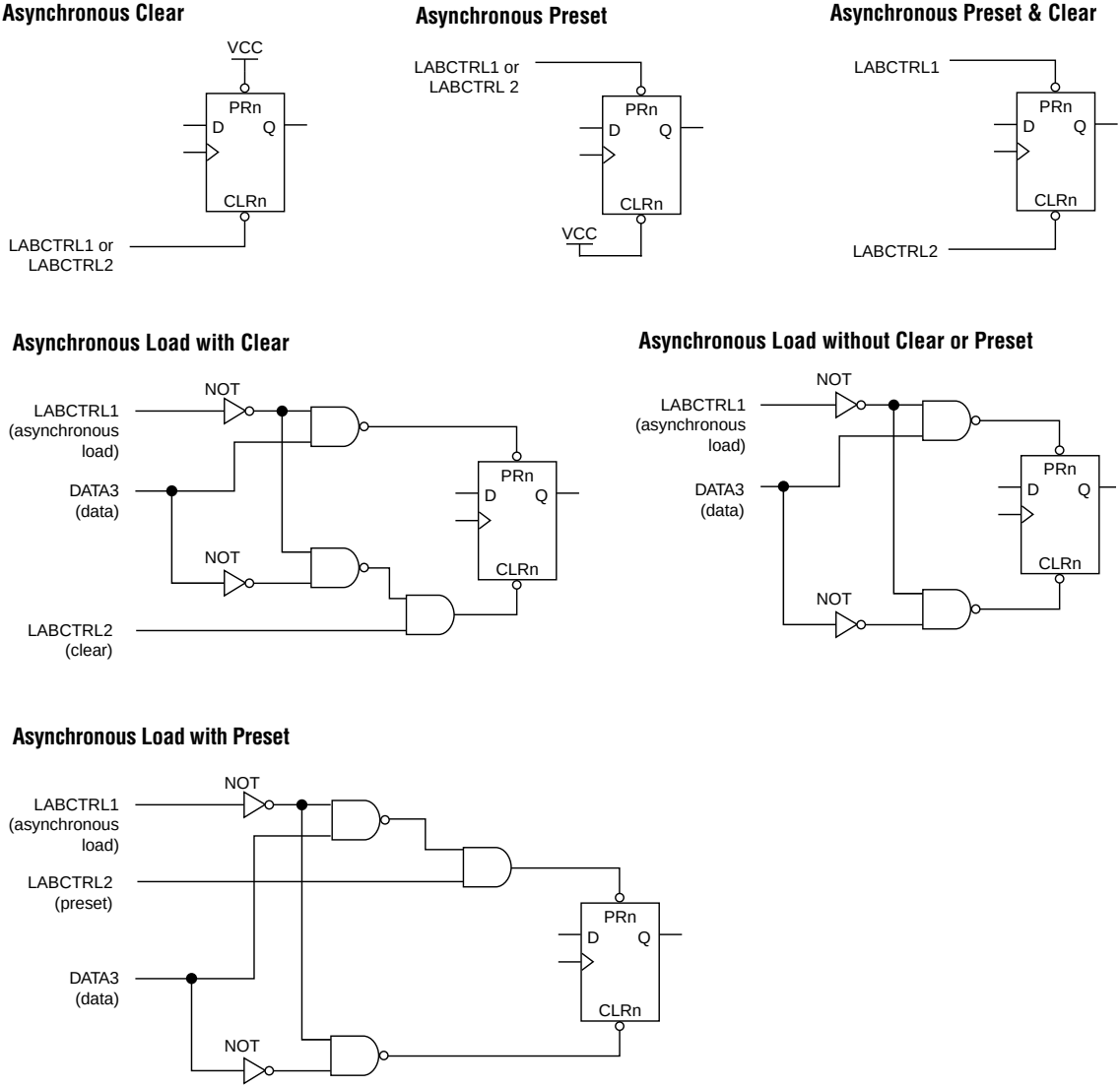
During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

In addition to the six clear and preset modes, FLEX 10K devices provide a device-wide clear pin that can reset all registers in the device. This pin is set during design entry. In any of the clear and preset modes, the device-wide clear overrides all other signals. See Figure 10.

Figure 10. LE Clear & Preset Modes



Asynchronous Clear

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to VCC to deactivate it.

Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, MAX+PLUS II can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to VCC, therefore, asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with the preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. MAX+PLUS II inverts the signal that drives DATA3 to account for the inversion of the register's output.

Asynchronous Load without Clear or Preset

When implementing an asynchronous load without the preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

FastTrack Interconnect

In the FLEX 10K architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

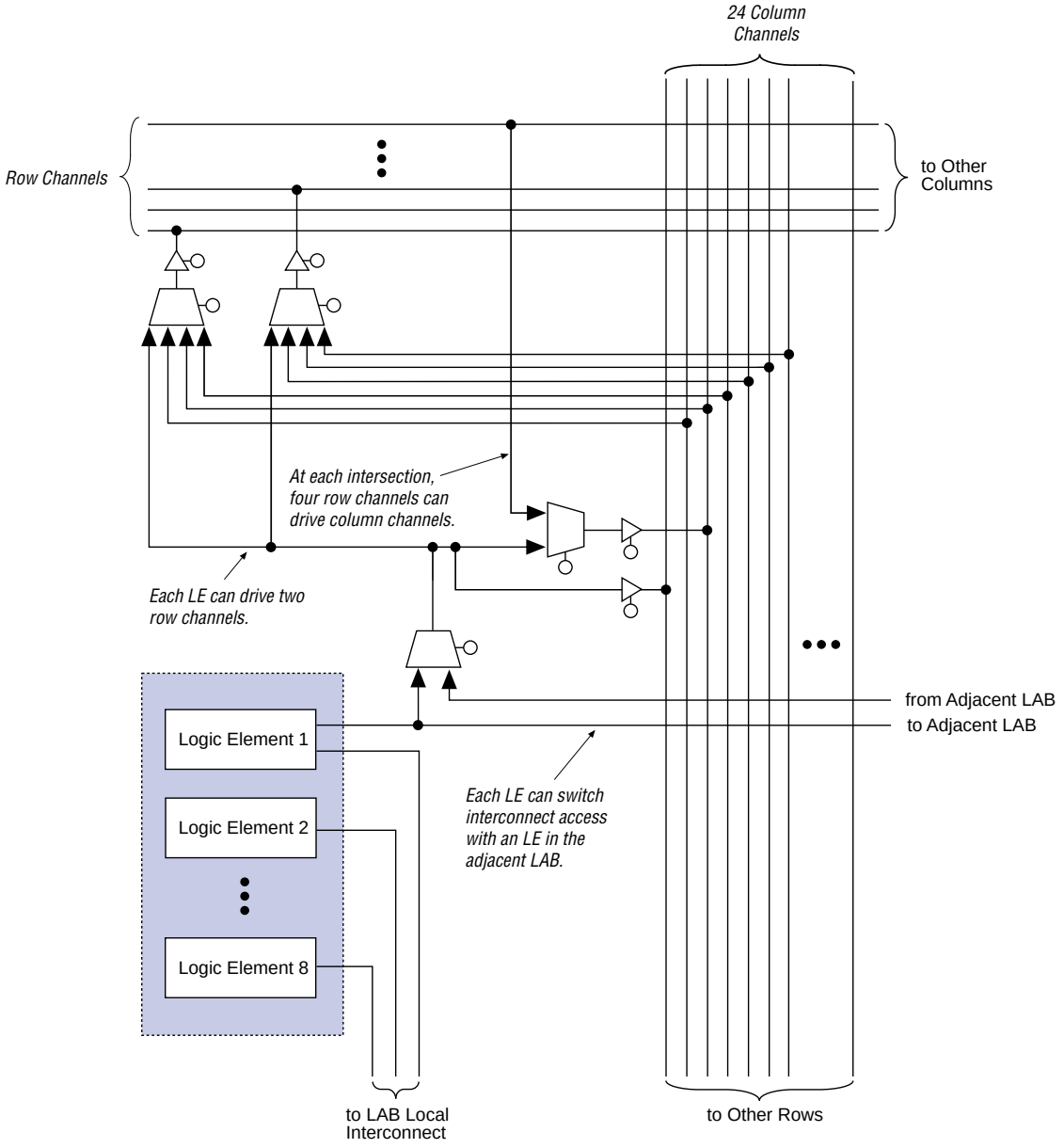
The FastTrack Interconnect consists of column and row interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the device. The column interconnect routes signals between rows and can drive I/O pins.

A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in an LAB drive the row interconnect.

Each column of LABs is served by a dedicated column interconnect. The column interconnect can then drive I/O pins or drive another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must be routed to the row interconnect before it can enter an LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, an LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This routing flexibility enables routing resources to be used more efficiently. See Figure 11.

Figure 11. LAB Connections to Row & Column Interconnect



For improved routability, the row interconnect is comprised of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in one-half of the row. The EAB can be driven by the half-channels in the left half of the row and by the full channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 4 summarizes the FastTrack Interconnect resources available in each FLEX 10K device.

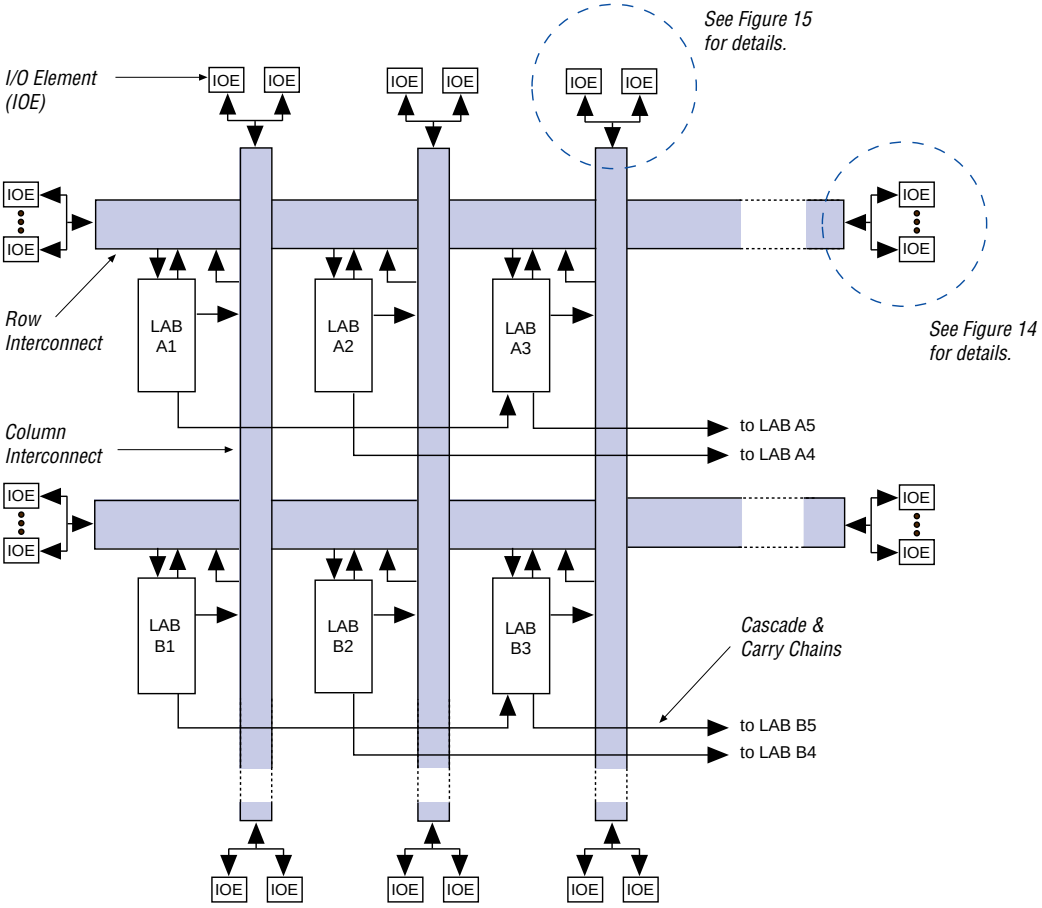
Table 4. FLEX 10K FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF10K10	3	144	24	24
EPF10K20	6	144	24	24
EPF10K30	6	216	36	24
EPF10K40	8	216	36	24
EPF10K50	10	216	36	24
EPF10K70	9	312	52	24
EPF10K100	12	312	52	24

In addition to general-purpose I/O pins, FLEX 10K devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. However, the use of dedicated inputs as data inputs can introduce additional delay into the control signal network.

Figure 12 shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number representing the column. For example, LAB B3 is in row B, column 3.

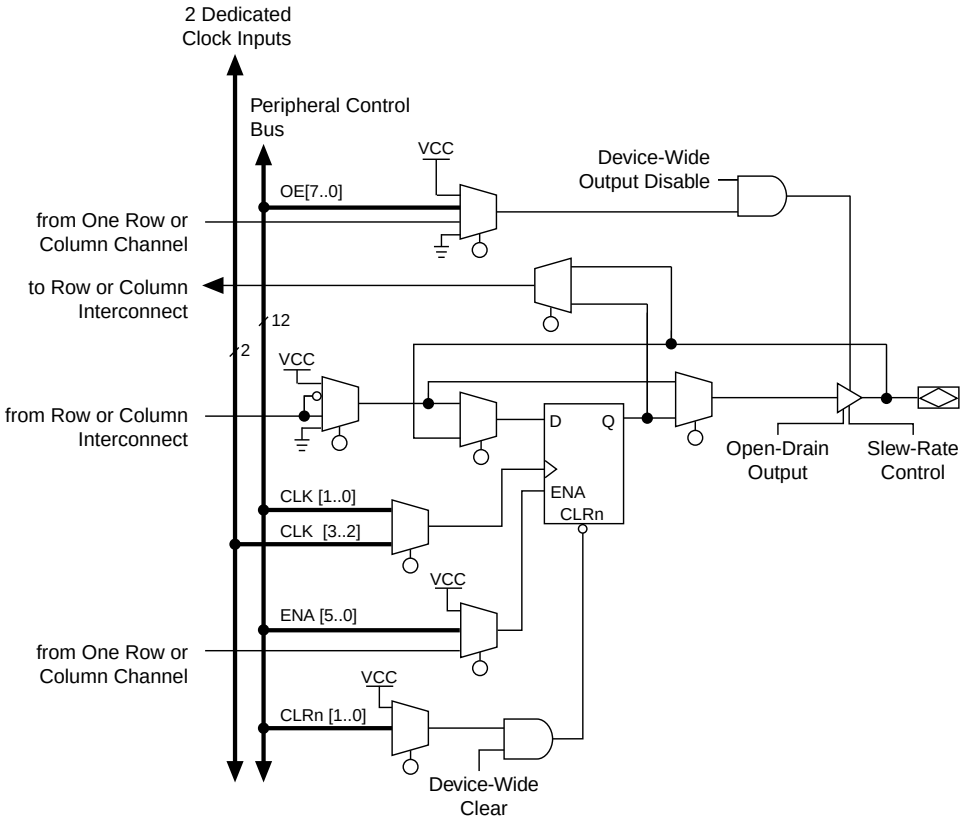
Figure 12. FLEX 10K Device Interconnect Resources



I/O Element

An I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect where appropriate. Figure 13 shows the IOE block diagram.

Figure 13. FLEX 10K Device I/O Element



The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of 4.5 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. Each pin can also be specified as open-drain on a pin-by-pin basis.

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices; it provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by a specific LE. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, an LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal.

Table 5 lists the sources for each peripheral control signal, shows how the output enable, clock enable, clock, and clear signals share the 12 peripheral control signals, and the rows that can drive the global signals.

Table 5. Peripheral Bus Sources

Peripheral Control Signal	EPF10K10	EPF10K20	EPF10K30	EPF10K40	EPF10K50	EPF10K70	EPF10K100
OE0	Row A	Row A	Row A	Row A	Row A	Row A	Row A
OE1	Row A	Row B	Row B	Row C	Row B	Row B	Row C
OE2	Row B	Row C	Row C	Row D	Row D	Row D	Row E
OE3	Row B	Row D	Row D	Row E	Row F	Row I	Row G
OE4	Row C	Row E	Row E	Row F	Row H	Row G	Row I
OE5	Row C	Row F	Row F	Row G	Row J	Row H	Row K
CLKENA0/CLK0/ GLOBAL0	Row A	Row A	Row A	Row B	Row A	Row E	Row B
CLKENA1/OE6/ GLOBAL1	Row A	Row B	Row B	Row C	Row C	Row C	Row D
CLKENA2/CLR0	Row B	Row C	Row C	Row D	Row E	Row B	Row F
CLKENA3/OE7/ GLOBAL2	Row B	Row D	Row D	Row E	Row G	Row F	Row H
CLKENA4/CLR1	Row C	Row E	Row E	Row F	Row I	Row H	Row J
CLKENA5/CLK1/ GLOBAL3	Row C	Row F	Row F	Row H	Row J	Row E	Row L

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Table 5. The internally generated signal can drive the global signal, providing the same low-skew, low-delay characteristics for an internally generated signal as for a signal driven by an input. This feature is ideal for internally generated clear or clock signals with high fan-out.

A device-wide output disable pin is an active-low pin that can be used to tri-state all pins on the device. This option can be set in the design file. Additionally, the registers in the IOE can be reset by the device-wide clear pin.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Eight IOEs connect to each side of each row channel. See Figure 14.

Figure 14. FLEX 10K Row-to-IOE Connections

The values for m and n are provided in Table 6.

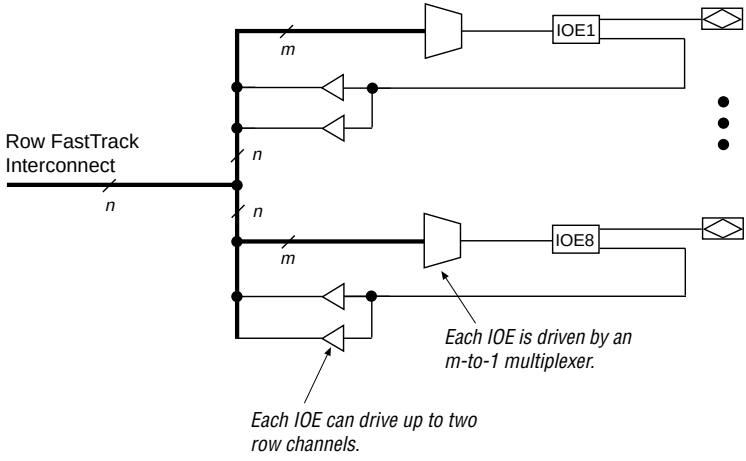


Table 6 lists the FLEX 10K row-to-IOE interconnect resources.

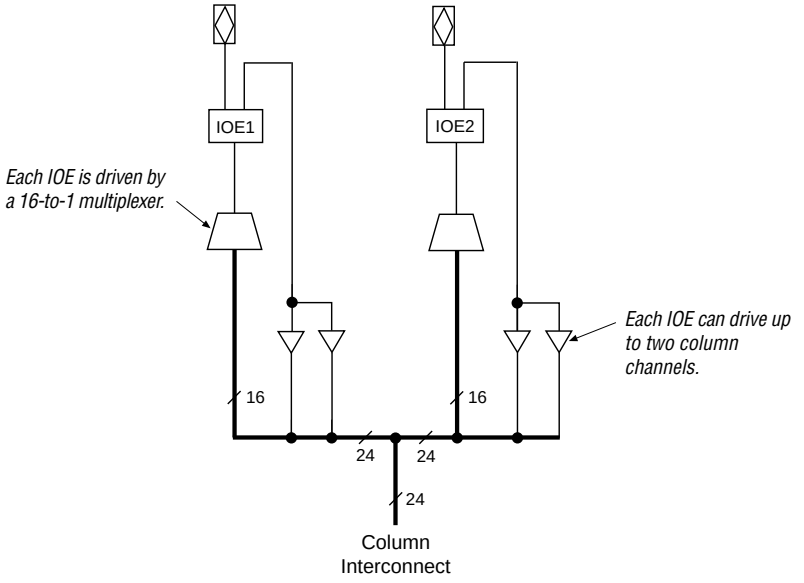
Table 6. FLEX 10K Row-to-IOE Interconnect Resources

Device	Channels per Row (*n*)	Row Channel per Pin (*m*)
EPF10K10	144	18
EPF10K20	144	18
EPF10K30	216	27
EPF10K40	216	27
EPF10K50	216	27
EPF10K70	312	39
EPF10K100	312	39

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be connected to 16 of the 24 column channels via a 16-to-1 multiplexer. The set of 16 column channels that each IOE can access is different for each IOE. See Figure 15.

Figure 15. FLEX 10K Column-to-IOE Connections



ClockLock & ClockBoost

To support high-speed designs, specially marked FLEX 10K devices offer optional ClockLock and ClockBoost circuitry. These circuits are phase-locked loops (PLLs) and can be used to increase design speed and reduce resource usage. The ClockLock circuitry is a synchronizing PLL that reduces the clock delay and skew within a device, improving setup and clock-to-output times. With the ClockBoost circuitry, which provides a clock multiplier, designers can easily implement time-domain-multiplexed logic to reduce resource usage in a design.

3.3- or 5.0-V I/O Pin Operation

Some FLEX 10K devices can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCINT} pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs. The V_{CCIO} pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the V_{CCIO} pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}.

Open-Drain Output Option

FLEX 10K devices provide an optional open-drain (electrically equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

JTAG Operation

All FLEX 10K devices provide JTAG BST circuits that comply with the IEEE Std. 1149.1-1990 specification. All FLEX 10K devices can also be configured using the JTAG PROGRAM instruction.

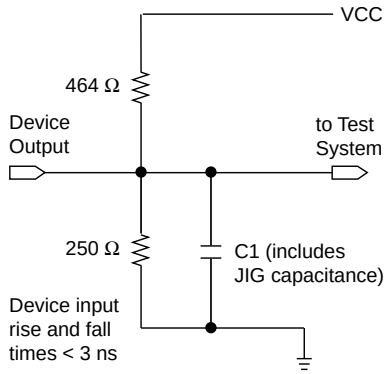
Go to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)* for more information.

Generic Testing

Each FLEX 10K device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 10K devices are made under conditions equivalent to those shown in Figure 16. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 16. FLEX 10K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



FLEX 10K Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		Plastic and power quad flat pack packages, under bias		135	° C

FLEX 10K Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	*Note (4)*	3.00	3.60	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

FLEX 10K Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V, *Note (7)*	2.4			V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V, *Note (7)*	2.4			V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V, *Note (8)*			0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V, *Note (8)*			0.45	V
I_I	Input pin leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load		500		µA

FLEX 10K Device Capacitance *Note (9)*

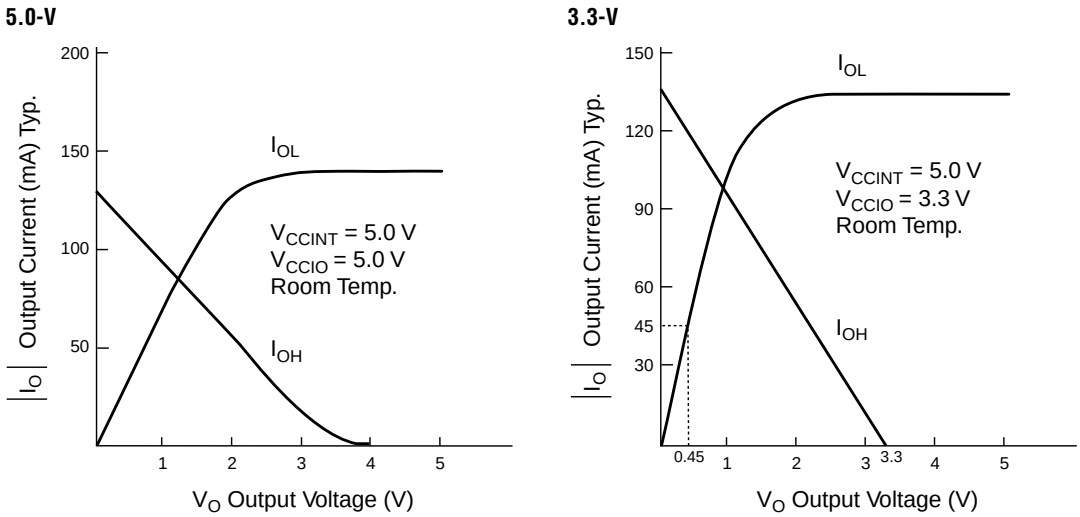
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for industrial-temperature-range versions.
(4) Maximum V_{CC} rise time is 100 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) Operating conditions: V_{CCINT} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(7) The I_{OH} parameter refers to high-level TTL output current.
(8) The I_{OL} parameter refers to low-level TTL output current.
(9) Capacitance is sample-tested only.

Figure 17 shows the typical output drive characteristics of FLEX 10K devices with 5.0-V and 3.3V V_{CCIO}. The output driver is compatible with the ***PCI Local Bus Specification,*** version 2.0.

Figure 17. Output Drive Characteristics for Devices with 5.0-V V_{CCIO}



Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row could be calculated by adding the following parameters:

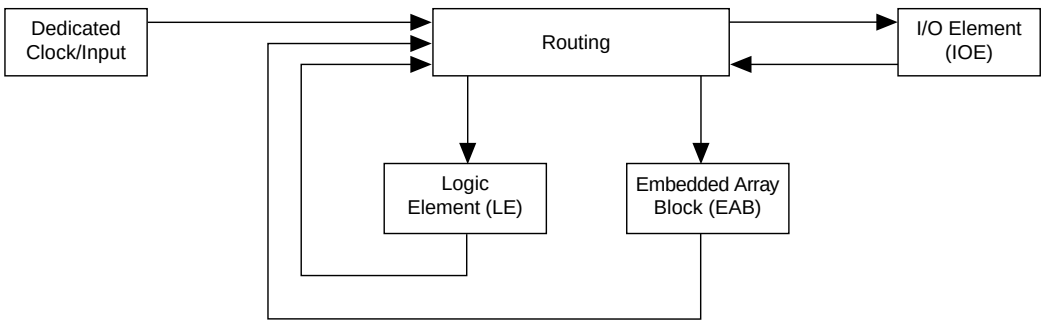
- LE register clock-to-output delay (t_{CO})
- Routing delay ($t_{SAMEROW}$)
- LE look-up table delay (t_{LUT})
- LE register setup time (t_{SU})

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 18 shows the overall timing model, which maps the possible routing paths to and from the various elements of the FLEX 10K device.

Figure 18. FLEX 10K Device Timing Model



Figures 19 through 21 show the delays that correspond to various paths and functions within the LE, IOE, and EAB timing models.

Figure 19. FLEX 10K Device LE Timing Model

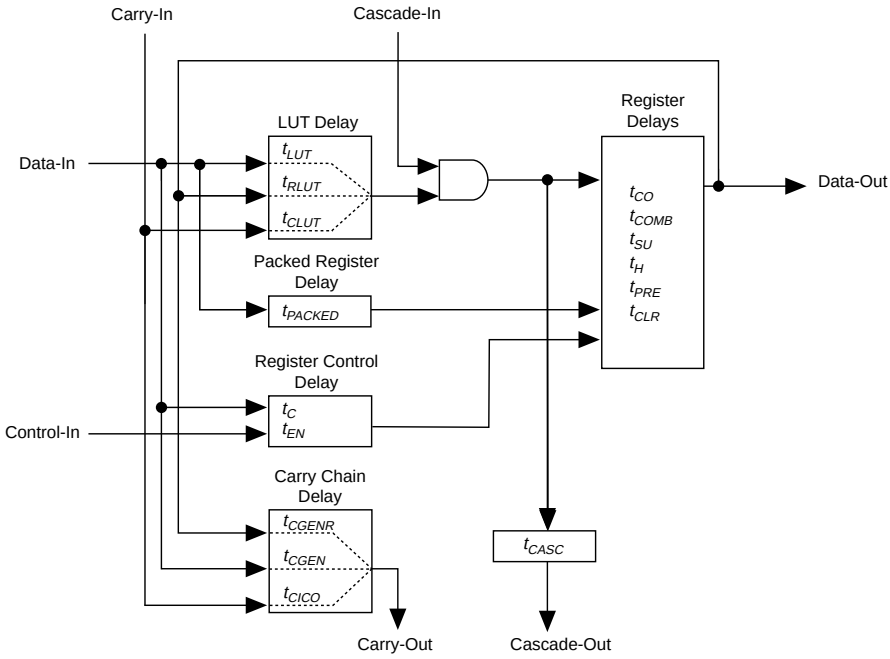


Figure 20. FLEX 10K Device IOE Timing Model

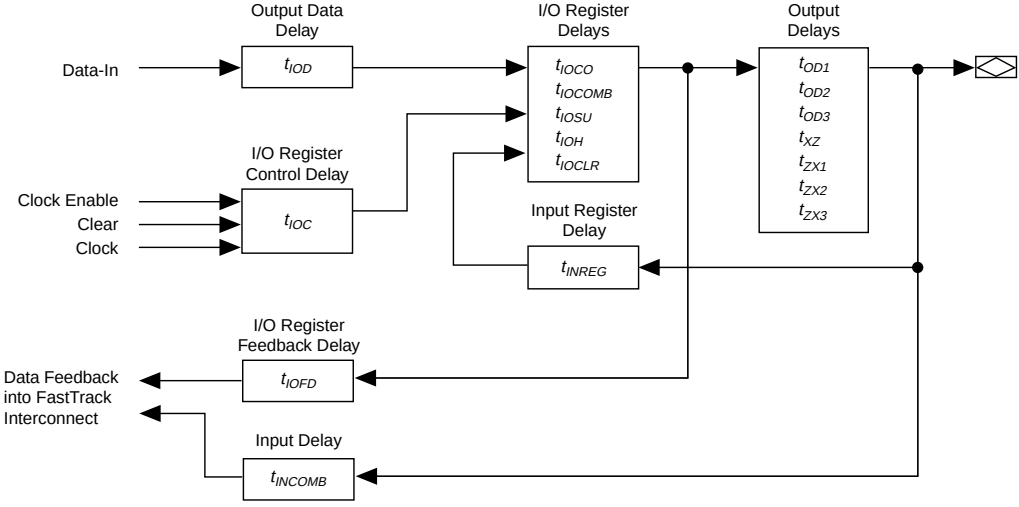
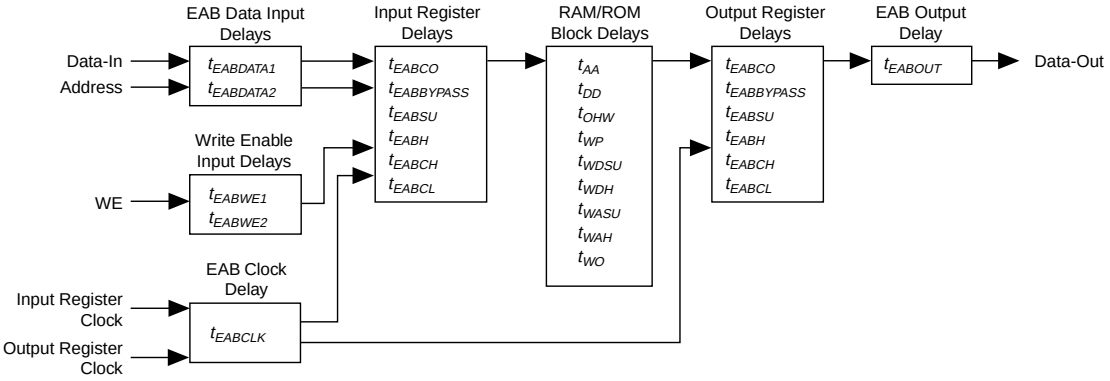


Figure 21. FLEX 10K Device EAB Timing Model



Tables 7 through 11 describe the FLEX 10K internal timing parameters. These internal timing parameters are expressed as worst-case values. Using hand calculations, these parameters can be used to estimate design performance. However, before committing designs to silicon, actual worst-case performance should be modeled using timing simulation and timing analysis. Tables 12 and 13 describe FLEX 10K external timing parameters.

Table 7. LE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{LUT}	LUT delay for data-in	
t_{CLUT}	LUT delay for carry-in	
t_{RLUT}	LUT delay for LE register feedback	
t_{PACKED}	Data-in to packed register delay	
t_{EN}	LE register enable delay	
t_{CICO}	Carry-in to carry-out delay	
t_{CGEN}	Data-in to carry-out delay	
t_{CGENR}	LE register feedback to carry-out delay	
t_{CASC}	Cascade-in to cascade-out delay	
t_{C}	LE register control signal delay	
t_{CO}	LE register clock-to-output delay	
t_{COMB}	Combinatorial delay	
t_{SU}	LE register setup time before clock	
t_{H}	LE register hold time before clock	
t_{PRE}	LE register preset delay	
t_{CLR}	LE register clear delay	

Table 8. IOE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{IOD}	IOE data delay	
t_{IOC}	IOE register control signal delay	
t_{IOCO}	IOE register clock-to-output delay	
t_{IOCOMB}	IOE combinatorial delay	
t_{IOSU}	IOE register data setup time before clock	
t_{IOH}	IOE register data hold time after clock	
t_{IOCLR}	IOE register clear time	
t_{OD1}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF *Note (2)*
t_{OD2}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *Note (3)*
t_{OD3}	Output buffer and pad delay, Slow slew rate = on	C1 = 35 pF *Note (4)*
t_{XZ}	IOE output buffer disable delay	
t_{ZX1}	IOE output buffer enable delay, Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF *Note (2)*
t_{ZX2}	IOE output buffer enable delay, Slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *Note (3)*
t_{ZX3}	IOE output buffer enable delay, Slow slew rate = off	C1 = 35 pF *Note (4)*
t_{INREG}	IOE input pad and buffer to IOE register delay	
t_{IOFD}	IOE register feedback delay	
t_{INCOMB}	IOE input pad and buffer to FastTrack Interconnect delay	

Table 9. EAB Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
t_{EABWE1}	Write enable delay to EAB for combinatorial input	
t_{EABWE2}	Write enable delay to EAB for registered input	
t_{EABCLK}	EAB register clock delay	
t_{EABCO}	EAB register clock-to-output delay	
$t_{EABBYPASS}$	Bypass register delay	
t_{EABSU}	EAB register setup time before clock	
t_{EABH}	EAB register hold time after clock	
t_{EABCH}	Clock high time	
t_{EABCL}	Clock low time	
t_{AA}	Address access delay	
t_{WP}	Write pulse width	
t_{WDSU}	Data setup time before falling edge of write pulse	*Note (5)*
t_{WDH}	Data hold time after falling edge of write pulse	*Note (5)*
t_{WASU}	Address setup time before rising edge of write pulse	*Note (5)*
t_{WAH}	Address hold time after falling edge of write pulse	*Note (5)*
t_{WO}	Write enable to data output valid delay	
t_{DD}	Data-in to data-out valid delay	
t_{EABOUT}	Data-out delay	

Table 10. EAB Timing Macroparameters (Part 1 of 2) *Note (6)*

Symbol	Parameter	Equation	Conditions
t_{EABAA}	EAB address access delay	$t_{EABDATA1} + t_{EABBYPASS} + t_{AA} + t_{EABBYPASS} + t_{EABOUT}$	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	$t_{EABDATA1} + t_{EABBYPASS} + t_{AA} + t_{EABBYPASS} + t_{EABOUT}$	
$t_{EABRCREG}$	EAB synchronous read cycle time	$t_{EABCO} + t_{AA} + t_{EABSU}$	
t_{EABWP}	EAB write pulse width	t_{WP}	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	$t_{WASU} + t_{WP} + t_{WAH}$	
$t_{EABWCREG}$	EAB synchronous write cycle time	$t_{EABCO} + t_{DD} + t_{EABSU}$	
t_{EABDD}	EAB data-in to data-out valid delay	$t_{EABDATA1} + t_{EABBYPASS} + t_{DD} + t_{EABBYPASS} + t_{EABOUT}$	

Table 10. EAB Timing Macroparameters (Part 2 of 2) *Note (6)*			
Symbol	**Parameter**	**Equation**	**Conditions**
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	$t_{EABCLK} + t_{EABCO} + t_{EABOUT}$	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	$t_{EABSU} + t_{EABDATA2} - t_{EABCLK}$	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	$t_{EABH} + t_{EABCLK} - t_{EABDATA2}$	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	$t_{EABSU} + t_{EABWE2} - t_{EABCLK}$	
t_{EABWEH}	EAB WE hold time after clock when using input register	$t_{EABH} + t_{EABCLK} - t_{EABWE2}$	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	$t_{WDSU} + (t_{EABDATA1} + t_{EABBYPASS}) - (t_{EABWE1} + t_{EABBYPASS})$	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	$t_{WDH} + (t_{EABWE1} + t_{EABBYPASS}) - (t_{EABDATA1} + t_{EABBYPASS})$	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	$t_{WASU} + (t_{EABDATA1} + t_{EABBYPASS}) - (t_{EABWE1} + t_{EABBYPASS})$	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	$t_{WAH} + (t_{EABWE1} + t_{EABBYPASS}) - (t_{EABDATA1} + t_{EABBYPASS})$	
t_{EABWO}	EAB write enable to data output valid delay	$t_{EABWE1} + t_{EABBYPASS} + t_{WO} + t_{EABBYPASS} + t_{EABOUT}$	

Table 11. Routing Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	*Note (7)*
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	*Note (7)*
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	*Note (7)*
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	*Note (7)*
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	*Note (7)*
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	*Note (7)*
t_{DIN2LE}	Delay from dedicated input pin to LE control input	*Note (7)*
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	*Note (7)*
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE clock	*Note (7)*

Table 12. External Reference Timing Parameters *Note (8)*

Symbol	Parameter	Conditions
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects	*Note (9)*

Table 13. External Timing Parameters *Note (10)*

Symbol	Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (11)*

Notes to tables:

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
(2) Operating conditions: V_{CCIO} = 5.0 V ± 5% for commercial use.
V_{CCIO} = 5.0 V ± 10% for industrial use.
(3) Operating conditions: V_{CCIO} = 3.3 V ± 5% for commercial use.
V_{CCIO} = 3.3 V ± 10% for industrial use.
(4) Operating conditions: V_{CCIO} = 3.3 V or 5.0 V.
(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
(8) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(9) Contact Altera Applications at (800) 800-EPLD for test circuit specifications and test conditions.
(10) These timing parameters are sample tested only.
(11) This parameter is a guideline that is sample-tested only and based on extensive device characterization. This parameter applies for both global and non-global clocking and for LE, EAB, and IOE registers.

Figures 22 and 23 show the asynchronous and synchronous timing waveforms, respectively, for the EAB macroparameters in Table 10.

Figure 22. EAB Asynchronous Timing Waveforms

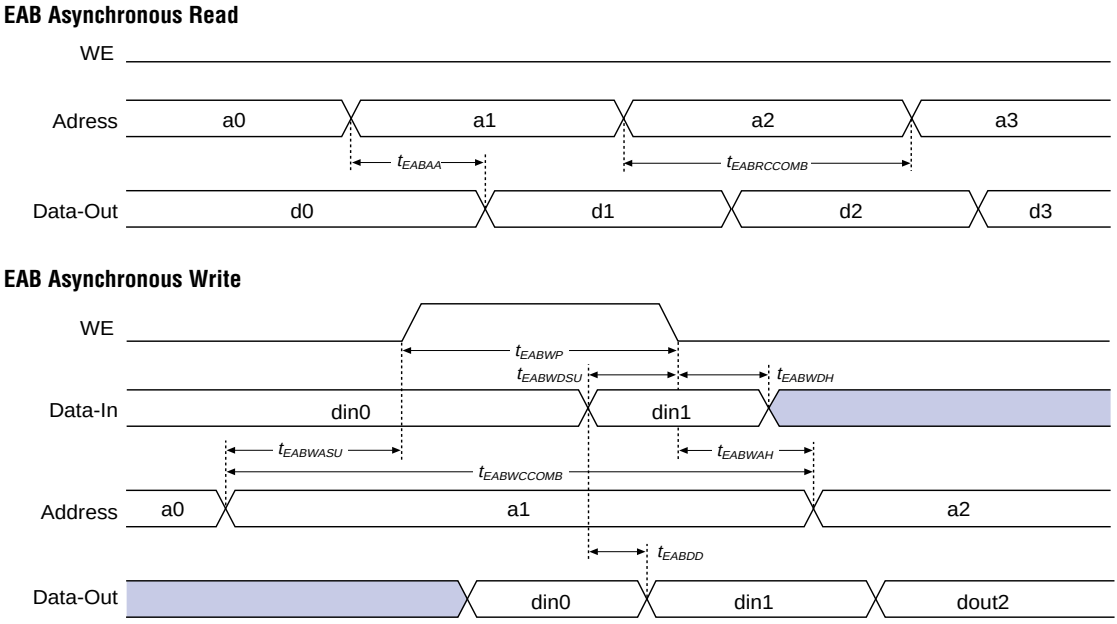
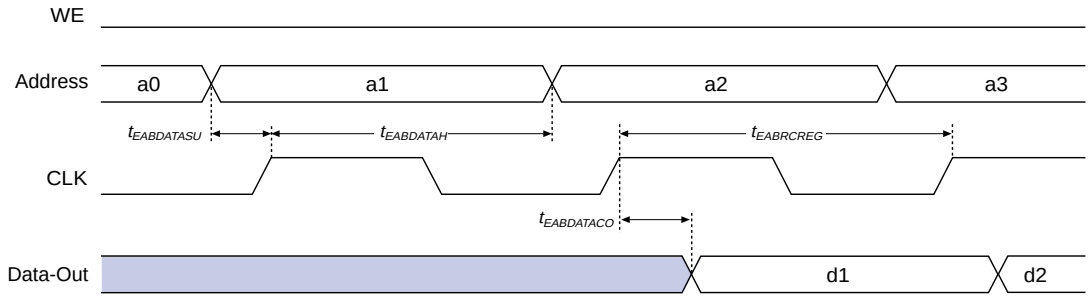
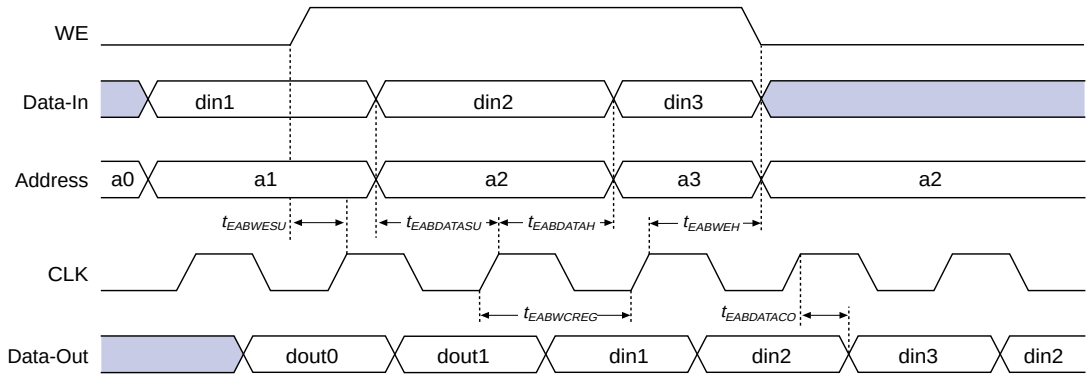


Figure 23. EAB Synchronous Timing Waveforms

EAB Synchronous Read



EAB Synchronous Write



FLEX 10K Device Internal Timing Parameters

LE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.5		1.9		2.5	ns
t_{CLUT}		0.8		1.0		1.4	ns
t_{RLUT}		1.3		1.5		2.2	ns
t_{PACKED}		0.7		0.8		1.1	ns
t_{EN}		0.7		0.8		1.1	ns
t_{CICO}		0.3		0.3		0.5	ns
t_{CGEN}		1.2		1.5		2.0	ns
t_{CGENR}		0.2		0.2		0.3	ns
t_{CASC}		1.1		1.2		1.5	ns
t_{C}		1.1		1.4		1.9	ns
t_{CO}		0.2		0.2		0.3	ns
t_{COMB}		0.6		0.7		0.9	ns
t_{SU}	2.2		2.7		3.7		ns
t_{H}	0.0		0.0		0.0		ns
t_{PRE}		1.2		1.4		1.9	ns
t_{CLR}		0.9		1.1		1.4	ns

FLEX 10K Device IOE Timing Microparameters *Note (1)* Updates							
Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		1.3		1.6		2.0	ns
t_{IOC}		1.2		1.4		1.8	ns
t_{IOCO}		0.2		0.2		0.3	ns
t_{IOCOMB}		0.2		0.3		0.3	ns
t_{IOSU}	3.8		4.6		5.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.1		1.3		1.7	ns
t_{OD1}		6.1		6.2		6.4	ns
t_{OD2}		6.4		6.6		7.0	ns
t_{OD3}		8.7		9.5		10.5	ns
t_{XZ}		1.4		1.7		2.1	ns
t_{ZX1}		1.4		1.7		2.1	ns
t_{ZX2}		1.7		2.1		2.7	ns
t_{ZX3}		4.0		5.0		6.2	ns
t_{INREG}		4.9		5.9		7.4	ns
t_{IOFD}		1.0		1.1		1.2	ns
t_{INCOMB}		1.0		1.1		1.1	ns

FLEX 10K Device EAB Internal Microparameters							
Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		2.4		3.0		3.9	ns
$t_{EABDATA2}$		4.7		5.8		7.5	ns
t_{EABWE1}		2.4		3.0		3.9	ns
t_{EABWE2}		4.7		5.8		7.5	ns
t_{EABCLK}		0.9		1.1		1.4	ns
t_{EABCO}		0.6		0.7		0.9	ns
$t_{EABBYPASS}$		0.8		1.0		1.3	ns
t_{EABSU}	1.8		2.2		2.9		ns
t_{EABH}	0.0		0.0		0.0		ns
t_{EABCH}	4.3		5.3		6.9		ns
t_{EABCL}	1.6		1.9		2.5		ns
t_{AA}		7.1		8.7		11.3	ns
t_{WP}	4.7		5.8		7.5		ns
t_{WDSU}	5.9		7.3		9.5		ns
t_{WDH}	0.0		0.0		0.0		ns
t_{WASU}	2.4		3.0		3.8		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		7.1		8.7		11.3	ns
t_{DD}		7.1		8.7		11.3	ns
t_{EABOUT}		3.1		3.9		5.0	ns

FLEX 10K Device EAB Internal Timing Macroparameters *Note (2)*							
Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		14.2		17.6		22.8	ns
$t_{EABRCCOMB}$		14.2		17.6		22.8	ns
$t_{EABRCREG}$		9.5		11.6		15.1	ns
t_{EABWP}	4.7		5.8		7.5		ns
$t_{EABWCCOMB}$		7.1		8.8		11.3	ns
$t_{EABWCREG}$		9.5		11.6		15.1	ns
t_{EABDD}		14.2		17.6		22.8	ns
$t_{EABDATACO}$		4.6		5.7		7.3	ns
$t_{EABDATASU}$	5.6		6.9		9.0		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	5.6		6.9		9.0		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	5.9		7.3		9.5		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	2.4		3.0		3.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		14.2		17.6		22.8	ns

EPF10K10 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		5.2		5.7	ns
t_{DIN2LE}		3.1		3.2	ns
$t_{DCLK2IOE}$		2.0		2.2	ns
$t_{DCLK2LE}$		3.1		3.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		2.6		2.9	ns
$t_{SAMECOLUMN}$		3.5		3.9	ns
$t_{DIFFROW}$		6.1		6.7	ns
$t_{TWOROWS}$		8.7		9.6	ns
$t_{LEPERIPH}$		5.6		6.2	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

EPF10K20 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		5.2		5.7	ns
t_{DIN2LE}		3.1		3.2	ns
$t_{DCLK2IOE}$		2.0		2.2	ns
$t_{DCLK2LE}$		3.1		3.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		2.6		2.9	ns
$t_{SAMECOLUMN}$		4.0		4.4	ns
$t_{DIFFROW}$		6.6		7.3	ns
$t_{TWOROWS}$		9.2		10.1	ns
$t_{LEPERIPH}$		5.6		6.2	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

EPF10K30 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		6.0		6.6	ns
t_{DIN2LE}		3.1		3.2	ns
$t_{DCLK2IOE}$		2.5		2.7	ns
$t_{DCLK2LE}$		3.1		3.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		3.7		4.1	ns
$t_{SAMECOLUMN}$		5.5		6.1	ns
$t_{DIFFROW}$		9.2		10.1	ns
$t_{TWOROWS}$		12.9		14.2	ns
$t_{LEPERIPH}$		6.7		7.4	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

EPF10K40 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		6.0		6.6	ns
t_{DIN2LE}		3.1		3.2	ns
$t_{DCLK2IOE}$		2.5		2.7	ns
$t_{DCLK2LE}$		3.1		3.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		3.7		4.1	ns
$t_{SAMECOLUMN}$		6.0		6.6	ns
$t_{DIFFROW}$		9.7		10.7	ns
$t_{TWOROWS}$		13.4		14.7	ns
$t_{LEPERIPH}$		6.7		7.4	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

EPF10K50 Routing Timing Microparameters *Note (1)*							
Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		6.0		6.7		10.6	ns
t_{DIN2LE}		3.1		3.2		3.3	ns
$t_{DCLK2IOE}$		2.5		2.7		4.5	ns
$t_{DCLK2LE}$		3.1		3.2		3.3	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		3.7		4.1		5.4	ns
$t_{SAMECOLUMN}$		6.5		7.2		8.1	ns
$t_{DIFFROW}$		10.2		11.2		13.5	ns
$t_{TWOROWS}$		13.9		15.3		18.9	ns
$t_{LEPERIPH}$		6.7		7.4		8.0	ns
$t_{LABCARRY}$		2.0		2.0		2.3	ns
$t_{LABCASC}$		2.6		2.6		2.9	ns

EPF10K70 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		9.0		9.9	ns
t_{DIN2LE}		6.1		6.2	ns
$t_{DCLK2IOE}$		4.0		4.9	ns
$t_{DCLK2LE}$		6.1		6.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		5.0		5.5	ns
$t_{SAMECOLUMN}$		8.5		9.4	ns
$t_{DIFFROW}$		13.5		14.9	ns
$t_{TWOROWS}$		18.5		20.4	ns
$t_{LEPERIPH}$		8.0		8.8	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

EPF10K100 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		9.4		10.3	ns
t_{DIN2LE}		6.1		6.2	ns
$t_{DCLK2IOE}$		4.0		4.9	ns
$t_{DCLK2LE}$		6.1		6.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		5.0		5.5	ns
$t_{SAMECOLUMN}$		9.0		9.9	ns
$t_{DIFFROW}$		14.0		15.4	ns
$t_{TWOROWS}$		19.0		20.9	ns
$t_{LEPERIPH}$		8.0		8.8	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

External Timing Parameters

EPF10K10 & EPF10K20 Device External Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{DRR}		16.1		20.0	ns
t_{INSU}, *Notes (2), (3)*	5.5		6.0		ns
t_{INH}, *Note (3)*	0.0		0.0		ns
t_{OUTCO}, *Note (3)*		8.5		8.9	ns
t_{ODH}, *Note (3)*	1.0		1.0		ns

EPF10K30 & EPF10K40 Device External Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{DRR}		17.2		21.1	ns
t_{INSU}, *Notes (2), (3)*	6.5		7.0		ns
t_{INH}, *Note (3)*	0.0		0.0		ns
t_{OUTCO}, *Note (3)*		8.5		8.9	ns
t_{ODH}, *Note (3)*	1.0		1.0		ns

EPF10K50 Device External Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		17.2		21.1		27.0	ns
t_{INSU}, *Notes (2), (3)*	6.5		7.0		7.7		ns
t_{INH}, *Note (3)*	0.0		0.0		0.0		ns
t_{OUTCO}, *Note (3)*		8.5		8.9		9.6	ns
t_{ODH}, *Note (3)*	1.0		1.0		1.0		ns

EPF10K70 & EPF10K100 Device External Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{DRR}		19.1		24.2	ns
t_{INSU}, *Notes (2), (3)*	7.0		7.7		ns
t_{INH}, *Note (3)*	0.0		0.0		ns
t_{OUTCO}, *Note (3)*		11.5		12.7	ns
t_{ODH}, *Note (3)*	1.0		1.0		ns

Notes to tables:
(1) All timing parameters are described in Tables 7 through 13 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is guaranteed by characterization.

Power Consumption

The supply power for FLEX 10K devices, P, can be calculated with the following equation:

$$P = P_{INT} + P_{IO}$$

$$= (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the "FLEX 10K Device DC Operating Conditions" table on page 61 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)* in this data book.

Relative to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CC_{ACTIVE}} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are as follows:

$\mathbf{f_{MAX}}$	=	Maximum operating frequency in MHz
N	=	Total number of logic cells used in the device
$\mathbf{tog_{LC}}$	=	Average percent of logic cells toggling at each clock (typically 12.5%)
K	=	Constant, shown in Table 14

Table 14. Values for Constant K

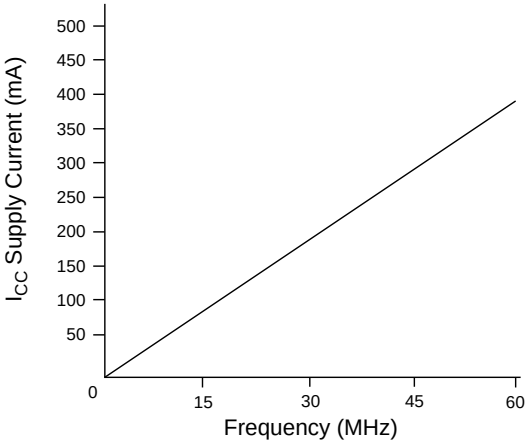
Device	K
EPF10K10	90
EPF10K20	98
EPF10K30	97
EPF10K40	101
EPF10K50	104
EPF10K70	93
EPF10K100	97

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

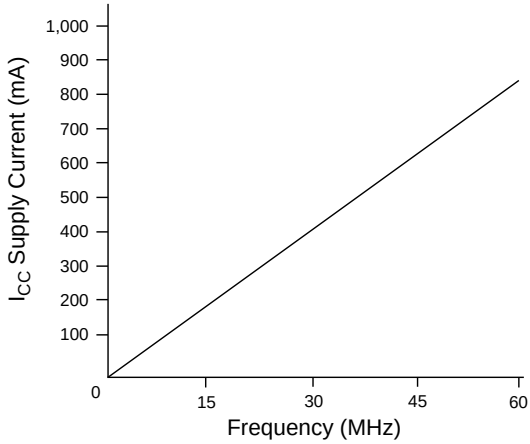
Figure 24 shows the relationship between the current and operating frequency of FLEX 10K devices.

Figure 24. $I_{CCACTIVE}$ vs. Operating Frequency (Part 1 of 2)

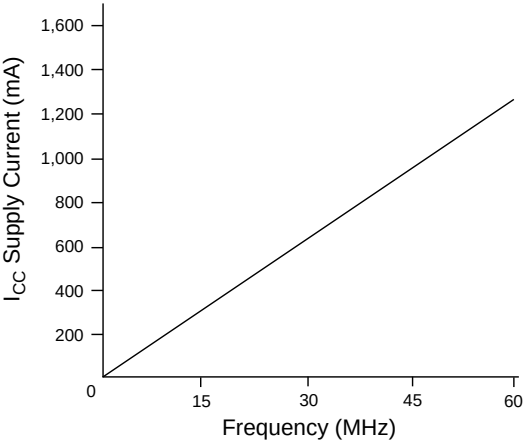
EPF10K10



EPF10K20



EPF10K30



EPF10K40

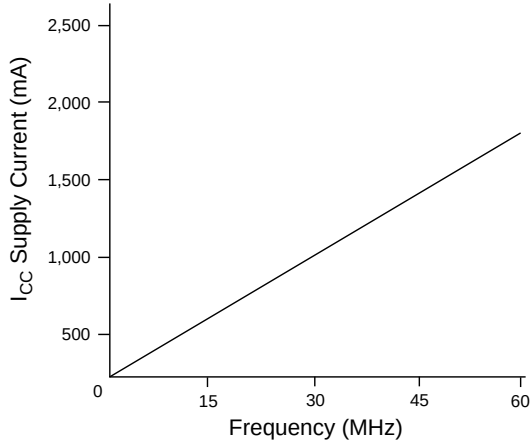
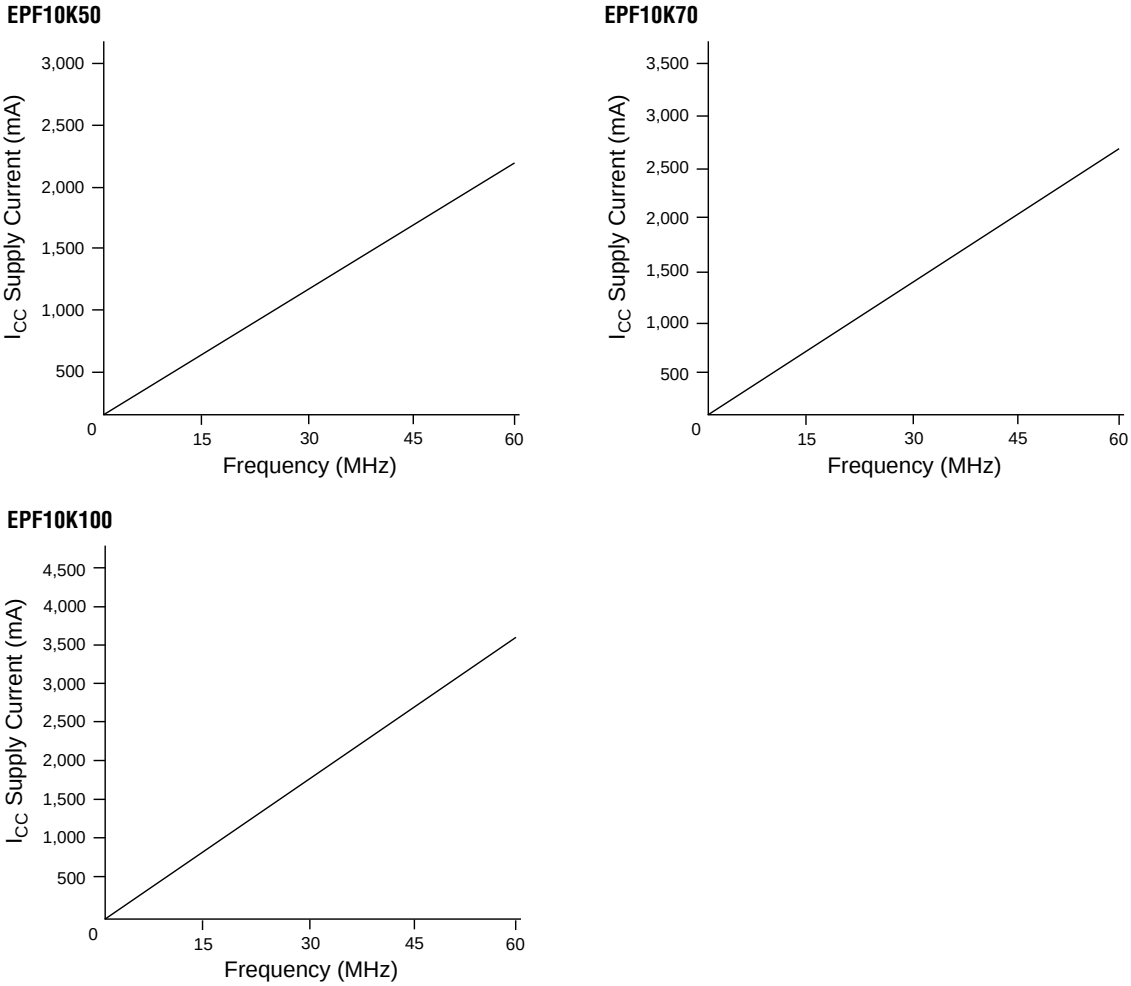


Figure 24. $I_{CCACTIVE}$ vs. Operating Frequency (Part 2 of 2)



Configuration & Operation

The FLEX 10K architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

Go to *Application Note 59 (Configuring FLEX 10K Devices)* for detailed descriptions of device configuration options; device configuration pins; and information on configuring FLEX 10K devices, including sample schematics, timing diagrams, and configuration parameters.

Operating Modes

The FLEX 10K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 10K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 200 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 10K device can be loaded with one of five configuration schemes (see Table 15), chosen on the basis of the target application. An EPC1 Configuration EPROM, intelligent controller, or JTAG port can be used to control the configuration of a FLEX 10K device, allowing automatic configuration on system power-up.

Multiple FLEX 10K devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 15. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration EPROM	EPC1 Configuration EPROM
Passive serial (PS)	BitBlaster, serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	JTAG controller, BitBlaster

Device Pin-Outs

Tables 16 through 18 show the pin names and numbers for the dedicated pins in each FLEX 10K device package.

Table 16. FLEX 10K Device Pin-Outs (Part 1 of 2) *Note (1)* Updates

Pin Name	84-Pin PLCC EPF10K10	208-Pin PQFP EPF10K10	208-Pin RQFP EPF10K20 EPF10K30 EPF10K40	240-Pin RQFP EPF10K20 EPF10K30 EPF10K40 EPF10K50 EPF10K70
MSEL0 *(2)*	20	108	108	124
MSEL1 *(2)*	21	107	107	123
nSTATUS *(2)*	44	52	52	60
nCONFIG *(2)*	23	105	105	121
DCLK *(2)*	2	155	155	179
CONF_DONE *(2)*	65	2	2	2
INIT_DONE *(4)*	58	19	19	26
nCE *(2)*	3	154	154	178
nCEO *(2)*	64	3	3	3
nWS *(3)*	69	206	206	238
nRS *(3)*	70	204	204	236
nCS *(3)*	67	208	208	240
CS *(3)*	68	207	207	239
RDYnBSY *(3)*	59	16	16	23
CLKUSR *(3)*	62	10	10	11
DATA7 *(3)*	78	166	166	190
DATA6 *(3)*	79	164	164	188
DATA5 *(3)*	80	162	162	186
DATA4 *(3)*	81	161	161	185
DATA3 *(3)*	82	159	159	183
DATA2 *(3)*	83	158	158	182
DATA1 *(3)*	84	157	157	181
DATA0 *(2)*	1	156	156	180
TDI *(2)*	4	153	153	177
TDO *(2)*	63	4	4	4
TCK *(2)*	66	1	1	1
TMS *(2)*	46	50	50	58
nTRST *(2)*	45	51	51	59

Table 16. FLEX 10K Device Pin-Outs (Part 2 of 2) *Note (1)* Updates

Pin Name	84-Pin PLCC EPF10K10	208-Pin PQFP EPF10K10	208-Pin RQFP EPF10K20 EPF10K30 EPF10K40	240-Pin RQFP EPF10K20 EPF10K30 EPF10K40 EPF10K50 EPF10K70
Dedicated Inputs	31, 33, 73, 75	78, 80, 182, 184	78, 80, 182, 184	90, 92, 210, 212
Dedicated Clock Pins	32,74	79, 183	79, 183	91, 211
DEV_CLRn *(4)*	76	180	180	209
DEV_OE *(4)*	72	186	186	213
VCCINT (5.0 V)	9, 22, 29, 34, 52, 77	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	5, 16, 27, 37, 47, 57, 77, 89, 96, 112, 122, 130, 140, 150, 160, 170, 189, 205, 224
VCCIO (5.0 V or 3.3 V)	–	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	–
GNDINT	15, 30, 35, 57, 71	21, 33, 49, 81, 82, 123, 129, 151, 185	21, 33, 49, 81, 82, 123, 129, 151, 185	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232
GNDIO	–	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	–
No Connect (N.C.) *Note (5)*	–	7, 8, 9, 14, 15, 36, 37, 113, 114, 125, 126, 139, 140	–	–
Total User I/O Pins	59	134	147	189

Table 17. EPF10K30 & EPF10K50 Pin-Outs (Part 1 of 2) *Note (1)*

Pin Name	356-Pin BGA EPF10K30	356-Pin BGA EPF10K50
MSEL0 *(2)*	D4	D4
MSEL1 *(2)*	D3	D3
nSTATUS *(2)*	D24	D24
nCONFIG *(2)*	D2	D2
DCLK *(2)*	AC5	AC5
CONF_DONE *(2)*	AC24	AC24
INIT_DONE *(4)*	T24	T24
nCE *(2)*	AC2	AC2
nCEO *(2)*	AC22	AC22
nWS *(3)*	AE24	AE24
nRS *(3)*	AE23	AE23
nCS *(3)*	AD24	AD24
CS *(3)*	AD23	AD23
RDYnBSY *(3)*	U22	U22
CLKUSR *(3)*	AA24	AA24
DATA7 *(3)*	AF4	AF4
DATA6 *(3)*	AD8	AD8
DATA5 *(3)*	AE5	AE5
DATA4 *(3)*	AD6	AD6
DATA3 *(3)*	AF2	AF2
DATA2 *(3)*	AD5	AD5
DATA1 *(3)*	AD4	AD4
DATA0 *(2)*	AD3	AD3
TDI *(2)*	AC3	AC3
TDO *(2)*	AC23	AC23
TCK *(2)*	AD25	AD25
TMS *(2)*	D22	D22
nTRST *(2)*	D23	D23
Dedicated Inputs	A13, B14, AF14, AE13,	A13, B14, AF14, AE13
Dedicated Clock Pins	A14, AF13	A14, AF13
DEV_CLRn *(4)*	AD13	AD13
DEV_OE *(4)*	AE14	AE14
VCCINT (5.0 V)	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26

Table 17. EPF10K30 & EPF10K50 Pin-Outs (Part 2 of 2) *Note (1)*

Pin Name	356-Pin BGA EPF10K30	356-Pin BGA EPF10K50
VCCIO (5.0 V or 3.3 V)	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16
GNDINT	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25
GNDIO	–	–
No Connect (N.C.) *Note (6)*	C1, D1, D26, E1, E2, G1, G5, G23, G26, H1, H25, H26, J25, K25, P24, R24, T23, U25, V1, V3, V4, V26, W2, W3, Y1, Y2, Y23, AC26	–
Total User I/O Pins	246	274

Table 18. EPF10K50, EPF10K70 & EPF10K100 Pin-Outs (Part 1 of 2)

Pin Name	403-Pin PGA EPF10K50	503-Pin PGA EPF10K70	503-Pin PGA EPF10K100
MSEL0 *(2)*	AN1	AT40	AT40
MSEL1 *(2)*	AR1	AV40	AV40
nSTATUS *(2)*	AU37	AY4	AY4
nCONFIG *(2)*	AU1	AY40	AY40
DCLK *(2)*	E1	H40	H40
CONF_DONE *(2)*	C37	F4	F4
INIT_DONE *(4)*	R35	V6	V6
nCE *(2)*	G1	K40	K40
nCEO *(2)*	E37	H4	H4
nWS *(3)*	E31	A3	A3
nRS *(3)*	A33	C5	C5
nCS *(3)*	A35	C1	C1
CS *(3)*	C33	C3	C3
RDYnBSY *(3)*	N35	T6	T6
CLKUSR *(3)*	G35	H6	H6
DATA7 *(3)*	C9	E29	E29
DATA6 *(3)*	A7	D30	D30
DATA5 *(3)*	E9	C31	C31
DATA4 *(3)*	C7	B32	B32
DATA3 *(3)*	A5	D32	D32
DATA2 *(3)*	E7	B34	B34
DATA1 *(3)*	C5	E33	E33
DATA0 *(2)*	C1	F40	F40
TDI *(2)*	J1	M40	M40
TDO *(2)*	G37	K4	K4
TCK *(2)*	A37	D4	D4
TMS *(2)*	AN37	AT4	AT4
nTRST *(2)*	AR37	AV4	AV4
Dedicated Inputs	A17, A21, AU17, AU21	D20, D24, AY24, AY20	D20, D24, AY24, AY20
Dedicated Clock Pins	A19, AU19	D22, AY22	D22, AY22
DEV_CLRn *(4)*	C17	F22	F22
DEV_OE *(4)*	C19	G21	G21

Table 18. EPF10K50, EPF10K70 & EPF10K100 Pin-Outs (Part 2 of 2)

Pin Name	403-Pin PGA EPF10K50	503-Pin PGA EPF10K70	503-Pin PGA EPF10K100
VCCINT (5.0 V)	B2, D14, E25, F22, K36, T2, T32, V6, AD34, AE5, AL5, AM6, AM20, AN25, AN29, AP4, AT16, AT36	C11, E39, G27, N5, N41, W39, AC3, AG7, AR3, AR41, AU37, AW5, AW25, AW41, BA17, BA19	C11, E39, G27, N5, N41, W39, AC3, AG7, AR3, AR41, AU37, AW5, AW25, AW41, BA17, BA19
VCCIO (5.0 V or 3.3 V)	B22, D34, E11, E27, F16, L5, L33, P4, T6, T36, V32, AB36, AG5, AG33, AH2, AM18, AM32, AN11, AN27, AP24, AT22	C9, C15, C25, C33, C37, E19, E41, G7, L3, R41, U3, U37, W5, AC41, AE5, AJ41, AL39, AU3, AU17, AW3, AW19, BA9, BA27, BA29, BA37	C9, C15, C25, C33, C37, E19, E41, G7, L3, R41, U3, U37, W5, AC41, AE5, AJ41, AL39, AU3, AU17, AW3, AW19, BA9, BA27, BA29, BA37
GNDINT	B16, B36, D4, E21, F18, F32, G33, P34, U5, Y32, AA33, AB2, AB6, AH36, AM16, AN17, AN21, AP14, AT2	C17, E3, E5, E25, G37, J3, J41, U7, AA3, AE39, AL5, AL41, AU27, AW39, BA7, BA13, BA25	C17, E3, E5, E25, G37, J3, J41, U7, AA3, AE39, AL5, AL41, AU27, AW39, BA7, BA13, BA25
GNDIO	B10, B28, D24, E5, E19, E33, F6, F20, K2, W5, W33, Y6, AB32, AD4, AM22, AN5, AN19, AN33, AP34, AT10, AT28	C21, C23, C39, C41, E13, E31, G3, G17, N3, N39, R3, W41, W3, AA41, AG37, AJ3, AN3, AN41, AU7, AU41, AW13, AW31, BA11, BA21, BA23	C21, C23, C39, C41, E13, E31, G3, G17, N3, N39, R3, W3, W41, AA41, AG37, AJ3, AN3, AN41, AU7, AU41, AW13, AW31, BA11, BA23, BA21,
No Connect (N.C.) *Note (7)*	–	A19, A21, A23, A31, A33, A35, A39, A41, B16, B18, B22, B24, B30, B40, C29, C35, D18, D26, D28, D38, E27, E37, F18, F2, F26, F30, F32, G23, G25, G29, G31, G33, G35, K6, K42, L39, L43, M2, N7, P38, P4, P42, R37, T40, V42, AC5, AD2, AE3	–
Total User I/O Pins	310	358	406

Notes to tables:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin after configuration.
(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(5) To maintain pin compatibility when migrating from the EPF10K30 to the EPF10K10 in the 208-pin RQFP package, do not use these pins as user I/O pins.
(6) To maintain pin compatibility when migrating from the EPF10K50 to the EPF10K30 in the 356-pin BGA package, do not use these pins as user I/O pins.
(7) To maintain pin compatibility when migrating from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.

FLEX 10K

Embedded Programmable Logic Family

August 1996, ver. 2.1 Data Sheet Supplement

Preliminary Information

This data sheet supplement provides package outline and pin-out information for the FLEX 10K devices listed in Table 1. This supplement should be used together with the *FLEX 10K Embedded Programmable Logic Family Data Sheet* in the Altera ***1996 Data Book***.

Table 1. FLEX 10K Devices

Device	Package
EPF10K10	144-pin thin quad flat pack (TQFP)
EPF10K20	144-pin TQFP
EPF10K30	356-pin ball-grid array (BGA)
EPF10K50	356-pin BGA

Device Pin-Outs

Table 2 shows the pin names and numbers for the packages shown in Table 1.

Table 2. FLEX 10K Package Pin-Outs (Part 1 of 2) *Note (1)*

Pin Name	144-pin TQFP EPF10K10 EPF10K20	356-Pin BGA EPF10K30	356-Pin BGA EPF10K50
MSEL0 *(2)*	77	D4	D4
MSEL1 *(2)*	76	D3	D3
nSTATUS *(2)*	35	D24	D24
nCONFIG *(2)*	74	D2	D2
DCLK *(2)*	107	AC5	AC5
CONF_DONE *(2)*	2	AC24	AC24
INIT_DONE *(3)*	14	T24	T24
nCE *(2)*	106	AC2	AC2
nCEO *(2)*	3	AC22	AC22
nWS *(4)*	142	AE24	AE24
nRS *(4)*	141	AE23	AE23
nCS *(4)*	144	AD24	AD24
CS *(4)*	143	AD23	AD23
RDYnBSY *(4)*	11	U22	U22
CLKUSR *(4)*	7	AA24	AA24
DATA7 *(4)*	116	AF4	AF4
DATA6 *(4)*	114	AD8	AD8
DATA5 *(4)*	113	AE5	AE5
DATA4 *(4)*	112	AD6	AD6
DATA3 *(4)*	111	AF2	AF2
DATA2 *(4)*	110	AD5	AD5
DATA1 *(4)*	109	AD4	AD4
DATA0 *(2)*	108	AD3	AD3
TDI *(2)*	105	AC3	AC3
TDO *(2)*	4	AC23	AC23
TCLK *(2)*	1	AD25	AD25
TMS *(2)*	34	D22	D22
nTRST *(2)*	*Note (5)*	D23	D23
Dedicated Inputs	54, 56, 124, 126	AF14, AE13, B14, A13	AF14, AE13, B14, A13
GCLK0	125	AF13	AF13
GCLK1	55	A14	A14
DEV_CLRn *(3)*	122	AD13	AD13
DEV_OE *(3)*	128	AE14	AE14

Table 2. FLEX 10K Package Pin-Outs (Part 2 of 2) *Note (1)*

Pin Name	144-pin TQFP EPF10K10 EPF10K20	356-Pin BGA EPF10K30	356-Pin BGA EPF10K50
VCCINT (5.0 V)	6, 25, 52, 53, 75, 93, 123	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	A1, A26,Ci4, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26
VCCIO (5.0 V or 3.3 V)	5, 24, 45, 61, 71, 94, 115, 134	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16
GNDINT	16, 58, 84, 103, 127	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25
GNDIO	15, 40, 50, 57, 66, 85, 104, 129, 139	–	–
No Connect (N.C.) *(6)*	–	C1, D1, D26, E1, E2, G1, G5, G23, G26, H1, H25, H26, J25, K25, P24, R24, T23, U25, V1, V3, V4, V26, W2, W3, Y1, Y2, Y23, AC26	–
Total User I/O Pins	102	246	274

Notes to Table:

(1) Unlisted pins are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) If it is not used for its device-wide or configuration functions, this pin can be used as a user I/O pin.
(4) After configuration, this pin can be used as a user I/O pin.
(5) The optional JTAG pin nTRST is not used in the 144-pin TQFP package.
(6) To maintain pin compatibility when migrating from the EPF10K50 to the EPF10K30 in the 356-pin BGA package, do not use these pins as user I/O pins.

Package Outlines

Figure 1 and Figure 2 show the package outlines for the 356-pin BGA and 144-pin TQFP packages, respectively.

Package outline dimensions are shown in the following formats:

min. inches (min. millimeters)
max. inches (max. millimeters)

or:

nominal inches ± tolerance
(nominal millimeters ± tolerance)

or:

inches
(millimeters) BSC, Min., Max., Ref., Typ., R, Dia., Sq.

Table 3 shows the units used to describe package outline dimensions.

Table 3. Package Outline Units

Unit	Description
BSC	Basic. Represents theoretical exact dimension or dimension target.
Min.	Minimum dimension specified.
Max.	Maximum dimension specified.
Ref.	Reference. Represents dimension for reference use only. This value is not a device specification.
Typ.	Typical. Provided as a general value. This value is not a device specification.
R	Radius. Represents curve dimension.
Dia.	Diameter. Represents curve dimension.
Sq.	Square. Indicates a square feature for a package with equal length and width dimensions.

Figure 1. 356-Pin Ball-Grid Array (BGA)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only.

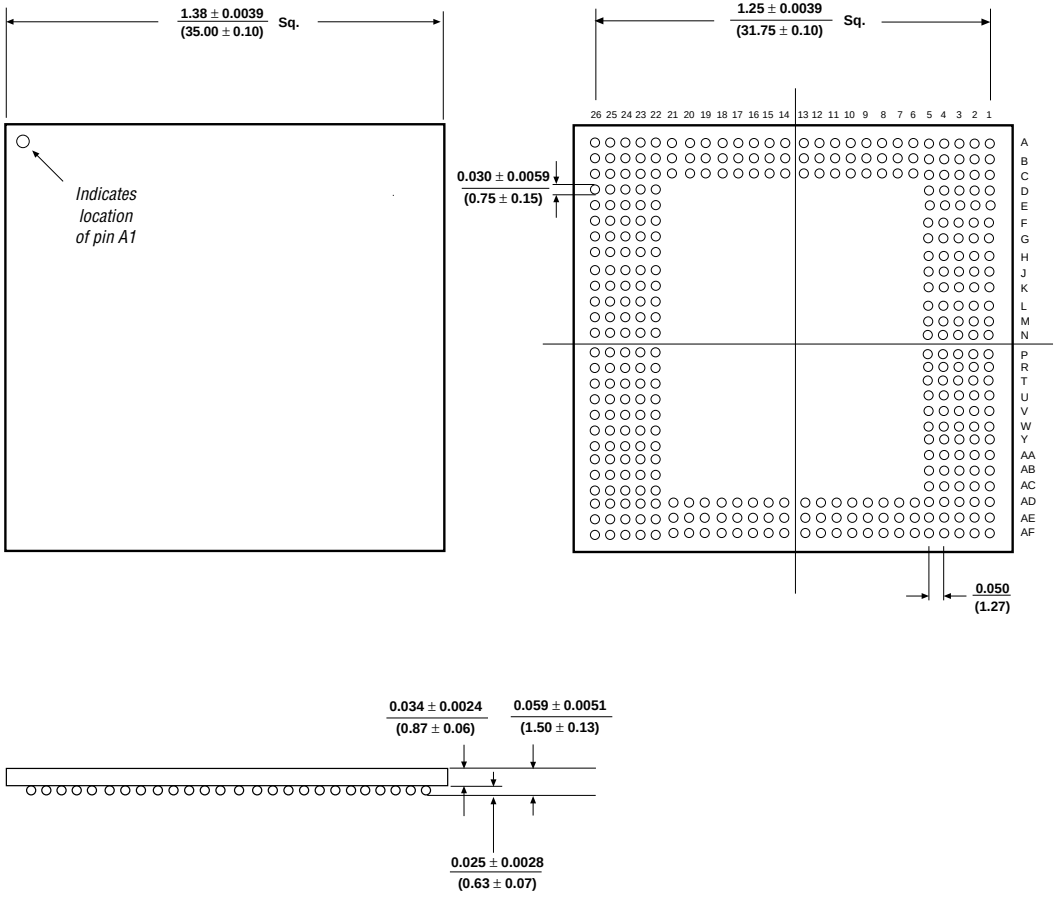
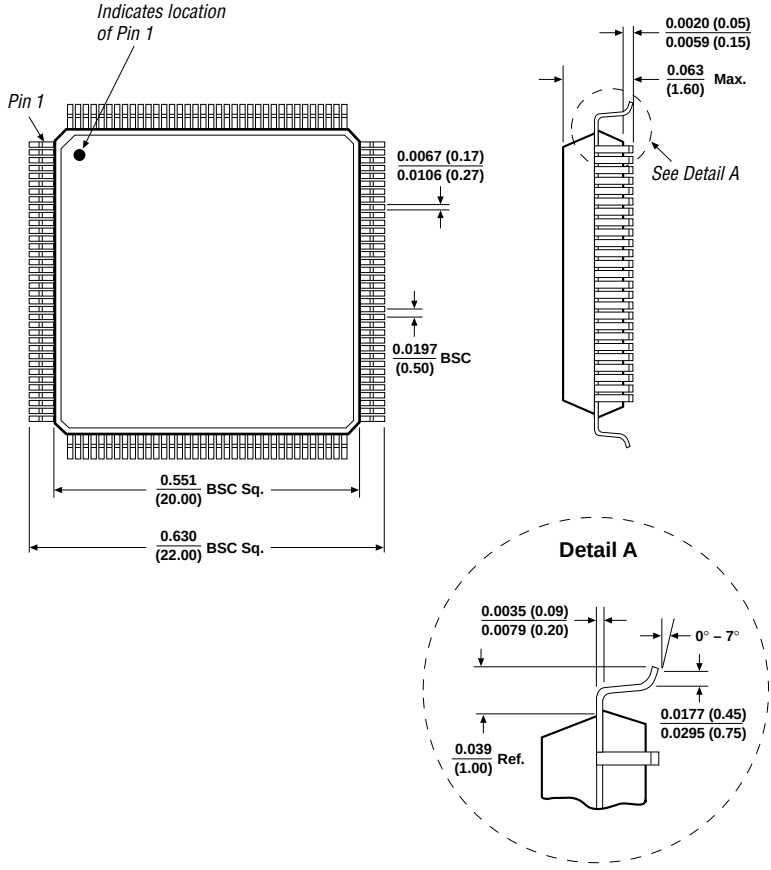


Figure 2. 144-Pin Plastic Thin Quad Flat Pack (TQFP)

This information is preliminary. Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only.



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EPF10K50V

Embedded Programmable Logic Device

December 1996, ver. 2.2 Data Sheet Supplement

Preliminary Information

This data sheet supplement provides operation and configuration information for EPF10K50V devices. This supplement should be used together with the *FLEX 10K Embedded Programmable Logic Family Data Sheet* in the Altera® ***1996 Data Book***.

Features

- 3.3-V operating voltage reduces power consumption
- 3.3 and 5.0-V TTL-compatible I/O levels
- Fabricated on a 0.35-micron process
- Pin-, function-, and programming-file compatible with other FLEX 10K devices in the same package
- Available in 240-pin power quad flat pack (RQFP) and 356-pin ball-grid array (BGA) packages

3.3-V or 5.0-V I/O Pin Operation

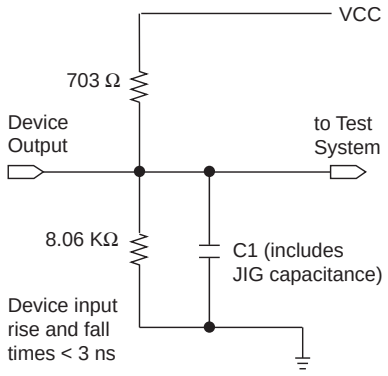
All EPF10K50V device inputs can be driven with 3.3-V or 5.0-V signals without damaging the device. Also, when driving a high signal, the output voltage is high enough to drive 5.0-V devices. The high-level output voltage (V_{OH}) specification is V_{CC} – 0.2 V, and the minimum V_{CC} is 3.0 V. Therefore, the minimum V_{OH} is 2.8 V, which exceeds the high-level input voltage (V_{IH}) requirement of 2.0 V for 5.0-V devices. This capability enables the EPF10K50V device to interface with both 3.3-V and 5.0-V devices without level shifters.

Generic Testing

Each EPF10K50V device is functionally tested and specified by Altera. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for EPF10K50V devices are made under conditions equivalent to those shown in Figure 1. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 1. FLEX 10K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Operating Conditions

The following tables provide absolute maximum ratings, recommended operating conditions, and DC operating conditions for EPF10K50V devices.

EPF10K50V 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Notes (2), (3)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Power quad flat pack (RQFP) packages, under bias		135	° C

EPF10K50V 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Note (3)*	3.0	3.6	V
V_I	Input voltage		0	5.55	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

EPF10K50V 3.3-V Device DC Operating Conditions *Note (4)*

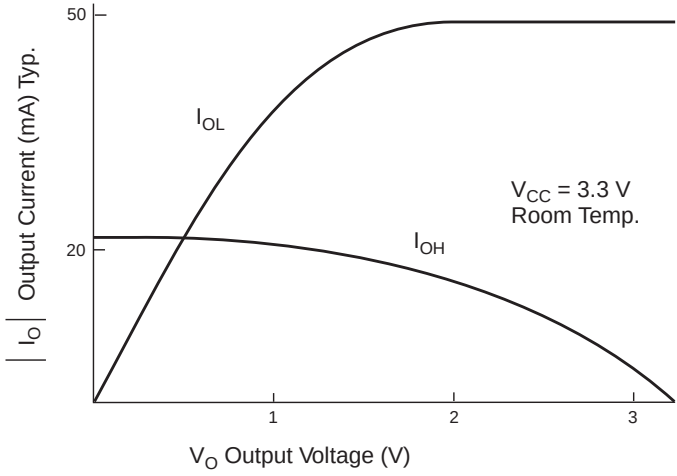
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		5.55	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA DC, *Note (5)*	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (5)*			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load, *Note (6)*		500		µA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in the Altera ***1996 Data Book***.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) The maximum V_{CC} rise time is 100 ms.
(4) Operating conditions: V_{CC} = 3.3 V ± 10% for commercial use.
(5) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.
(6) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.

Figure 2 shows the output drive characteristics of 3.3-V EPF10K50V devices.

Figure 2. Output Drive Characteristics



Timing Parameters

The following tables provide internal and external timing parameters for EPF10K50V devices. These tables should be used together with the timing models in the *FLEX 10K Embedded Programmable Logic Family Data Sheet*.

EPF10K50V Device Internal Timing Parameters

LE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{LUT}		1.8		2.3	ns
t_{CLUT}		1.3		1.7	ns
t_{RLUT}		1.6		2.1	ns
t_{PACKED}		0.8		1.0	ns
t_{EN}		0.8		1.0	ns
t_{CICO}		0.3		0.4	ns
t_{CGEN}		0.8		1.0	ns
t_{CGENR}		0.7		0.9	ns
t_{CASC}		0.4		0.5	ns
t_{C}		2.4		3.0	ns
t_{CO}		0.9		1.1	ns
t_{COMB}		0.5		0.6	ns
t_{SU}	0.2		0.3		ns
t_{H}	0.0		0.0		ns
t_{PRE}		3.0		3.8	ns
t_{CLR}		3.1		3.9	ns

EPF10K50V Device IOE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{IOD}		0.8		1.0	ns
t_{IOC}		0.5		0.7	ns
t_{IOCO}		0.4		0.5	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	1.9		2.4		ns
t_{IOH}	0.0		0.0		ns
t_{IOCLR}		1.7		2.2	ns
t_{OD1}		4.4		5.0	ns
t_{OD3}		8.1		9.7	ns
t_{XZ}		6.3		7.4	ns
t_{ZX1}		6.3		7.4	ns
t_{ZX3}		10.0		12.1	ns
t_{INREG}		10.0		12.6	ns
t_{IOFD}		3.6		4.5	ns
t_{INCOMB}		1.8		2.3	ns

EPF10K50V Device EAB Internal Microparameters					
Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{EABDATA1}$		2.4		3.0	ns
$t_{EABDATA2}$		4.7		5.8	ns
t_{EABWE1}		2.4		3.0	ns
t_{EABWE2}		4.7		5.8	ns
t_{EABCLK}		0.9		1.1	ns
t_{EABCO}		0.6		0.7	ns
$t_{EABBYPASS}$		0.8		1.0	ns
t_{EABSU}	1.8		2.2		ns
t_{EABH}	0.0		0.0		ns
t_{EABCH}	4.3		5.3		ns
t_{EABCL}	1.6		1.9		ns
t_{AA}		7.1		8.7	ns
t_{WP}	4.7		5.8		ns
t_{WDSU}	5.9		7.3		ns
t_{WDH}	0.0		0.0		ns
t_{WASU}	3.4		4.0		ns
t_{WAH}	0.0		0.0		ns
t_{WO}		7.1		8.7	ns
t_{DD}		7.1		8.7	ns
t_{EABOUT}		0.6		0.7	ns

EPF10K50V Device EAB Internal Timing Macroparameters (Part 1 of 2)					
Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{EABAA}		11.7		14.4	ns
$t_{EABRCCOMB}$		11.7		14.4	ns
$t_{EABRCREG}$		9.5		11.6	ns
t_{EABWP}	4.7		5.8		ns
$t_{EABWCCOMB}$		8.1		9.8	ns
$t_{EABWCREG}$		9.5		11.6	ns
t_{EABDD}		11.7		14.4	ns
$t_{EABDATACO}$		2.1		2.5	ns
$t_{EABDATASU}$	5.6		6.9		ns
$t_{EABDATAH}$	0.0		0.0		ns
$t_{EABWESU}$	5.6		6.9		ns
t_{EABWEH}	0.0		0.0		ns
$t_{EABWDSU}$	5.9		7.3		ns

EPF10K50V Device EAB Internal Timing Macroparameters (Part 2 of 2)					
Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{EABWDH}	0.0		0.0		ns
$t_{EABWASU}$	3.4		4.0		ns
t_{EABWAH}	0.0		0.0		ns
t_{EABWO}		11.7		14.4	ns

EPF10K50V Routing Timing Microparameters Note (1)					
Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{DIN2IOE}$		7.5		8.0	ns
t_{DIN2LE}		2.2		2.3	ns
$t_{DCLK2IOE}$		3.2		3.7	ns
$t_{DCLK2LE}$		2.2		2.3	ns
$t_{SAMELAB}$		0.3		0.4	ns
$t_{SAMEROW}$		4.5		4.9	ns
$t_{SAMECOLUMN}$		5.6		6.0	ns
$t_{DIFFROW}$		10.1		10.9	ns
$t_{TWOROWS}$		14.3		15.4	ns
$t_{LEPERIPH}$		4.7		5.2	ns
$t_{LABCARRY}$		0.8		1.0	ns
$t_{LABCASC}$		0.8		1.0	ns

EPF10K50V External Timing Parameters

EPF10K50V Device External Timing Parameters Note (1)					
Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{DRR}		17.2		21.1	ns
t_{INSU}, Notes (2), (3)	8.6		11.0		ns
t_{INH}, Note (3)	0.0		0.0		ns
t_{OUTCO}, Note (3)		8.5		9.9	ns
t_{ODH}, Note (3)	1.0		1.0		ns

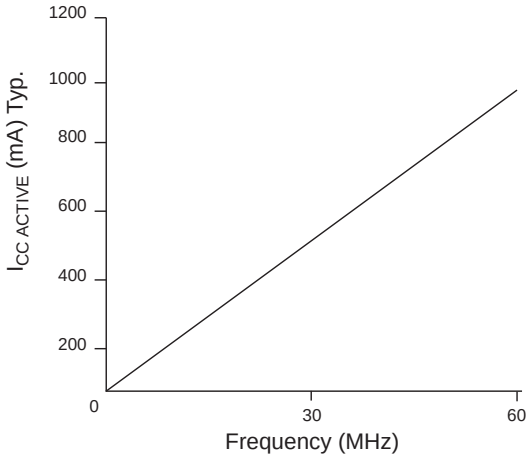
Notes to tables:

(1) All timing parameters are described in the *FLEX 10K Embedded Programmable Logic Family Data Sheet*.
(2) Using a logic element (LE) to register the signal may provide a lower setup time.
(3) This parameter is guaranteed by characterization.

Power Consumption

For details on computing power consumption for the EPF10K50V device, see the *FLEX 10K Embedded Programmable Logic Family Data Sheet* and *Application Note 74 (Evaluating Power for Altera Devices)* in the Altera ***1996 Data Book***. The required device-specific parameter for power computations is the constant *K*. The *K* value for the EPF10K50V device is 45. Figure 3 shows the relationship between the current and the operating frequency for a EPF10K50V device filled with 180 16-bit counters.

Figure 3. EPF10K50V $I_{CCACTIVE}$ vs. Operating Frequency



Device Configuration

FLEX 10K devices can be configured with EPC1 Configuration EPROMs, or with any passive configuration scheme using an intelligent host. EPC1 devices can operate with 3.3 or 5.0 V; the voltage level depends on the Programmer Object File (**.pof**) that is used to program the EPC1 device. When compiling a EPF10K50V design, MAX+PLUS® II will automatically create the POF to set the EPC1 Configuration EPROM for 3.3-V operation.

For more information on configuring EPF1050V devices, refer to *Application Note 59 (Configuring FLEX 10K Devices)*.

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ClockLock & ClockBoost in FLEX 10K Devices

March 1997, ver. 2.3 Data Sheet Supplement

Preliminary Information

This data sheet supplement provides information on the ClockLock™ and ClockBoost™ features available in FLEX® 10K devices. FLEX 10K devices with ClockLock and ClockBoost circuitry have "DX" in the ordering code (e.g., EPF10K100GC503-3DX). This data sheet supplement should be used together with the *FLEX 10K Embedded Programmable Logic Family Data Sheet* in the Altera® ***1996 Data Book***.

ClockLock & ClockBoost

The ClockLock and ClockBoost circuits contain a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by resource sharing within the device. ClockBoost allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, ClockLock and ClockBoost provide significant improvements in system performance and bandwidth.

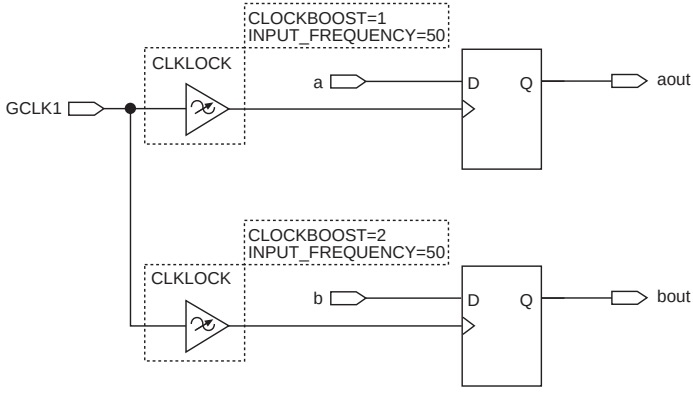
The ClockLock and ClockBoost features in FLEX 10K devices are enabled through the MAX+PLUS® II software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can only drive the clock inputs of registers; the generated clock cannot be gated or inverted.

The dedicated clock pin (`GCLK1`) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

In designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to GCLK1. With MAX+PLUS II version 7.2 and higher, GCLK1 can feed both the ClockLock and ClockBoost circuitry in the FLEX 10K device. However, when both circuits are used, the other clock pin (GCLK0) cannot be used. Figure 1 shows a block diagram of how to enable both the ClockLock and ClockBoost circuits in MAX+PLUS II version 7.2 and higher. The example shown is a schematic, but a similar approach applies for designs created in the Altera Hardware Description Language (AHDL™), VHDL, and Verilog HDL. When the ClockLock and ClockBoost circuits are used simultaneously, the input frequency parameter must be the same for both circuits. In this case, the input frequency must meet the requirements specified when the ClockBoost multiplication factor is two.

Figure 1. Enabling ClockLock & ClockBoost in the Same Design



To use both the ClockLock and ClockBoost circuits in the same design, designers must use Revision C EPF10K100GC503-3DX devices and MAX+PLUS II version 7.2 or higher. The revision is identified by the first digit of the date code stamped on top of the device (e.g., date code C9715 identifies a Revision C device). All designs previously created in MAX+PLUS II versions 7.0 and 7.1 will function properly in Revision C devices. However, programming files using only ClockLock or only ClockBoost circuitry that are designed in MAX+PLUS II version 7.2 will function in Revision B devices. Designs created in MAX+PLUS II version 7.2 that use both ClockLock and ClockBoost circuitry will configure Revision B devices, but will not function properly.

For more information on using the ClockLock and ClockBoost features, see the *Clock Management with ClockLock and ClockBoost Features White Paper*, which is available from Altera Literature Services.

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, generating an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 2 illustrates the incoming and generated clock specifications.

Figure 2. Specifications for the Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.

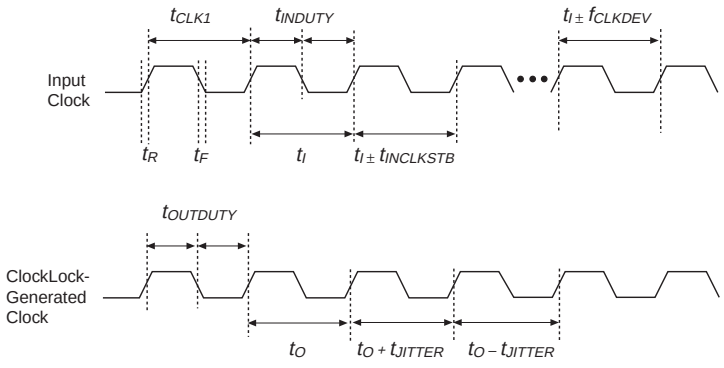


Table 1 summarizes the ClockLock and ClockBoost parameters.

Table 1. ClockLock & ClockBoost Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_R	Input rise time			2	ns
t_F	Input fall time			2	ns
t_{INDUTY}	Input duty cycle	45		55	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	30		80	MHz
t_{CLK1}	Input clock period (ClockBoost clock multiplication factor equals 1)	12.5		33.3	ns
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16		50	MHz
t_{CLK2}	Input clock period (ClockBoost clock multiplication factor equals 2)	20		62.5	ns
$f_{CLKDEV1}$	Input deviation from user specification in MAX+PLUS II, (ClockBoost clock multiplication factor equals 1), *Note (1)*			±1	MHz
$f_{CLKDEV2}$	Input deviation from user specification in MAX+PLUS II, (ClockBoost clock multiplication factor equals 2), *Note (1)*			±0.5	MHz
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)			100	ps
t_{LOCK}	Time required for ClockLock/ClockBoost to acquire lock, *Note (2)*			10	µs
t_{JITTER}	Jitter on ClockLock/ClockBoost-generated clock, *Note (3)*			1	ns
$t_{OUTDUTY}$	Duty cycle for ClockLock/ClockBoost-generated clock	40	50	60	%

Notes:

(1) To implement the ClockLock and ClockBoost circuitry with MAX+PLUS II, designers must specify the input frequency. MAX+PLUS II tunes the PLL in the ClockLock and ClockBoost circuitry to this entered frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the t_{LOCK} value is less than the time required for configuration.

(3) The t_{JITTER} specification is measured under long-term observation.

Delay Reduction

Using the ClockLock and ClockBoost features reduces delays from the clock pin to the logic element (LE) or I/O element (IOE). Table 2 shows the delays with and without the ClockLock and ClockBoost features. All parameters include t_{JITTER}, which affects the delay.

Table 2. EPF10K100 Routing Timing Parameters — -3DX Speed Grade

Symbol	Parameter	Condition	Min	Max	Unit
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE clock	Without ClockLock/ClockBoost		2.6	ns
		With ClockLock/ClockBoost		0.0	ns
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	Without ClockLock/ClockBoost		4.3	ns
		With ClockLock/ClockBoost		1.8	ns

Timing Improvements

Using the ClockLock or ClockBoost features improves setup, hold, and clock-to-output times. Table 3 shows these timing parameters with and without the ClockLock and ClockBoost features.

Table 3. EPF10K100 Device External Timing Parameters

Symbol	Parameter	Condition	-3DX Speed Grade Min	Max	Unit
t_{INSU} (1), (2)	Setup time with dedicated clock at IOE register	Without ClockLock/ClockBoost	8.9		ns
		With ClockLock/ClockBoost	4.2		ns
t_{INH} (1), (2)	Hold time with dedicated clock at IOE register	Without ClockLock/ClockBoost	0.0		ns
		With ClockLock/ClockBoost	0.0		ns
t_{OUTCO} (1), (2)	Clock-to-output delay with dedicated clock at IOE register	Without ClockLock/ClockBoost		9.6	ns
		With ClockLock/ClockBoost		8.3	ns
t_{ODH} (3)	Output data hold time after clock	Without ClockLock/ClockBoost for IOE registers	2.0		ns
		With ClockLock/ClockBoost for IOE registers	2.0		ns
		Without ClockLock/ClockBoost for LE registers	2.0		ns
		With ClockLock/ClockBoost for LE registers	2.0		ns

Notes:
(1) This parameter is guaranteed by production testing.
(2) When using ClockBoost, this parameter is specified relative to the rising edge of the incoming clock.
(3) This parameter is guaranteed by design and characterization.

Pins & Package Pin-Outs

The ClockLock and ClockBoost features are implemented with the pins listed in Table 4.

Table 4. ClockLock & ClockBoost Dedicated Pins

Pin Name	Description
GCLK1	Drives the ClockLock and ClockBoost circuitry.
LOCK	Shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. It is driven low if the clock violates the parameters in Table 1. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
VCC_CKLK GND_CKLK	Power and ground pins for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.

Table 5 describes the FLEX 10K package pin-outs.

Table 5. FLEX 10K Package Pin-Outs

Pin Name	503-Pin PGA EPF10K100
GCLK1	AY22
LOCK	AV14
VCC_CKLK	BA19
GND_CKLK	BA25

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EPF10K130V

Embedded Programmable Logic Device

April 1997, ver. 2.3 Data Sheet Supplement

Preliminary Information

This data sheet supplement provides operation and configuration information for EPF10K130V devices. This supplement should be used together with the *FLEX 10K Embedded Programmable Logic Family Data Sheet* in the Altera® ***1996 Data Book***.

Features

- 3.3-V operation
- Reduced power consumption
- Fabricated on a 0.35-micron process
- MultiVolt™ I/O interface enabling device core to run at 3.3 V, while I/O pins are compatible with 5.0-V and 3.3-V logic levels
- Pin compatible with other FLEX® 10K devices in the same package
- Designed for 599-pin pin-grid array (PGA) and 596-pin ball-grid array (BGA) packages
- Contains 6,656 FLEX logic elements (LEs)

3.3-V or 5.0-V I/O Pin Operation

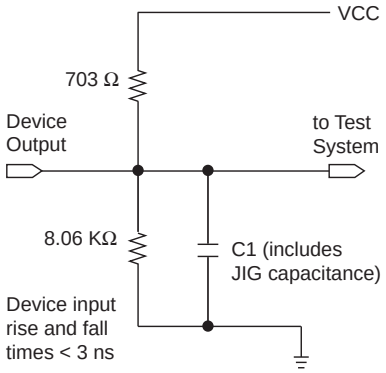
All EPF10K130V device inputs can be driven with 3.3-V or 5.0-V signals without damaging the device. Also, when driving a high signal, the output voltage is high enough to drive 5.0-V devices. The high-level output voltage (V_{OH}) specification is V_{CC} – 0.2 V, and the minimum V_{CC} is 3.0 V. Therefore, the minimum V_{OH} is 2.8 V, which exceeds the high-level input voltage (V_{IH}) requirement of 2.0 V for 5.0-V devices. This capability enables the EPF10K130V device to interface with both 3.3-V and 5.0-V devices without level shifters.

Generic Testing

Each EPF10K130V device is functionally tested and specified by Altera. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for EPF10K130V devices are made under conditions equivalent to those shown in Figure 1. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 1. FLEX 10K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Operating Conditions

The following tables provide absolute maximum ratings, recommended operating conditions, and DC operating conditions for EPF10K130V devices.

EPF10K130V 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Notes (2), (3)*	–0.5	4.6	V
V_I	DC input voltage		–0.5	5.7	V
I_{OUT}	DC output current per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Pin-grid array (PGA) packages, under bias		150	° C

EPF10K130V 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Note (3)*	3.0	3.6	V
V_I	Input voltage		0	5.3	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

EPF10K130V 3.3-V Device DC Operating Conditions *Note (4)*

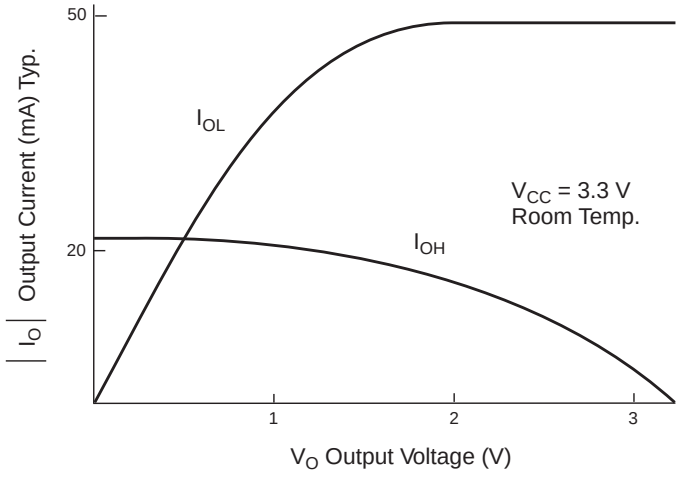
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		5.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA DC, *Note (5)*	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (5)*			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load, *Note (6)*		0.3	10	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in the Altera ***1996 Data Book***.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –0.5 V or overshoot to 5.7 V for periods shorter than 20 ns under no-load conditions.
(3) The maximum V_{CC} rise time is 100 ms.
(4) Operating conditions: V_{CC} = 3.3 V ± 10% for commercial use.
(5) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.
(6) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.

Figure 2 shows the output drive characteristics of 3.3-V EPF10K130V devices.

Figure 2. Output Drive Characteristics



Timing Parameters

The following tables provide internal and external timing parameters for EPF10K130V devices. This information should be used together with the timing models in the *FLEX 10K Embedded Programmable Logic Family Data Sheet*.

EPF10K130V Device Internal Timing Parameters

EPF10K130V LE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{LUT}		1.8		2.3	ns
t_{CLUT}		1.3		1.7	ns
t_{RLUT}		1.6		2.1	ns
t_{PACKED}		0.8		1.0	ns
t_{EN}		0.8		1.0	ns
t_{CICO}		0.3		0.4	ns
t_{CGEN}		1.1		1.3	ns
t_{CGENR}		0.7		0.9	ns
t_{CASC}		1.2		1.5	ns
t_{C}		2.4		3.0	ns
t_{CO}		0.9		1.1	ns
t_{COMB}		0.5		0.6	ns
t_{SU}	0.2		0.3		ns
t_{H}	0.0		0.0		ns
t_{PRE}		3.0		3.8	ns
t_{CLR}		3.1		3.9	ns

EPF10K130V Device IOE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{IOD}		1.6		2.0	ns
t_{IOC}		0.5		0.7	ns
t_{IOCO}		0.4		0.5	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	3.3		3.8		ns
t_{IOH}	0.0		0.0		ns
t_{IOCLR}		2.2		2.7	ns
t_{OD1}		4.4		5.0	ns
t_{OD3}		8.1		9.7	ns
t_{XZ}		6.3		7.4	ns
t_{ZX1}		6.3		7.4	ns
t_{ZX3}		10.0		12.1	ns
t_{INREG}		10.0		12.6	ns
t_{IOFD}		7.9		9.9	ns
t_{INCOMB}		1.8		2.3	ns

EPF10K130V Device EAB Internal Microparameters					
Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{EABDATA1}$		2.4		2.4	ns
$t_{EABDATA2}$		4.7		4.7	ns
t_{EABWE1}		2.4		2.4	ns
t_{EABWE2}		4.7		4.7	ns
t_{EABCLK}		0.9		0.9	ns
t_{EABCO}		0.6		0.6	ns
$t_{EABBYPASS}$		0.8		0.8	ns
t_{EABSU}	1.8		2.2		ns
t_{EABH}	0.0		0.0		ns
t_{EABCH}	4.3		4.3		ns
t_{EABCL}	1.6		1.6		ns
t_{AA}		7.1		7.1	ns
t_{WP}	4.7		4.7		ns
t_{WDSU}	5.9		5.9		ns
t_{WDH}	0.0		0.0		ns
t_{WASU}	5.0		5.0		ns
t_{WAH}	0.0		0.0		ns
t_{WO}		7.1		7.1	ns
t_{DD}		7.1		7.1	ns
t_{EABOUT}		0.6		0.6	ns

EPF10K130V Device EAB Internal Timing Macroparameters (Part 1 of 2)					
Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{EABAA}		11.7		11.7	ns
$t_{EABRCCOMB}$		11.7		11.7	ns
$t_{EABRCREG}$		9.5		9.9	ns
t_{EABWP}	4.7		4.7		ns
$t_{EABWCCOMB}$		9.7		9.7	ns
$t_{EABWCREG}$		9.5		9.9	ns
t_{EABDD}		11.7		11.7	ns
$t_{EABDATACO}$		2.1		2.1	ns
$t_{EABDATASU}$	5.6		6.0		ns
$t_{EABDATAH}$	0.0		0.0		ns
$t_{EABWESU}$	5.6		6.0		ns
t_{EABWEH}	0.0		0.0		ns
$t_{EABWDSU}$	5.9		5.9		ns

EPF10K130V Device EAB Internal Timing Macroparameters (Part 2 of 2)					
Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{EABWDH}	0.0		0.0		ns
$t_{EABWASU}$	5.0		5.0		ns
t_{EABWAH}	0.0		0.0		ns
t_{EABWO}		11.7		11.7	ns

EPF10K130V Routing Timing Microparameters Note (1)					
Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{DIN2IOE}$		9.0		9.5	ns
t_{DIN2LE}		3.0		3.1	ns
$t_{DCLK2IOE}$		4.6		5.1	ns
$t_{DCLK2LE}$		3.0		3.1	ns
$t_{SAMELAB}$		0.6		0.8	ns
$t_{SAMEROW}$		6.5		7.4	ns
$t_{SAMECOLUMN}$		12.5		13.5	ns
$t_{DIFFROW}$		19.0		20.9	ns
$t_{TWOROWS}$		24.9		27.5	ns
$t_{LEPERIPH}$		8.1		9.0	ns
$t_{LABCARRY}$		0.8		1.0	ns
$t_{LABCASC}$		1.0		1.2	ns

EPF10K130V External Timing Parameters

EPF10K130V Device External Timing Parameters Note (1)					
Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{DRR}		19.1		24.2	ns
t_{INSU}, Notes (2), (3)	8.6		11.0		ns
t_{INH}, Note (3)	0.0		0.0		ns
t_{OUTCO}, Note (3)		9.9		11.3	ns
t_{ODH}, Note (3)	2.0		2.0		ns

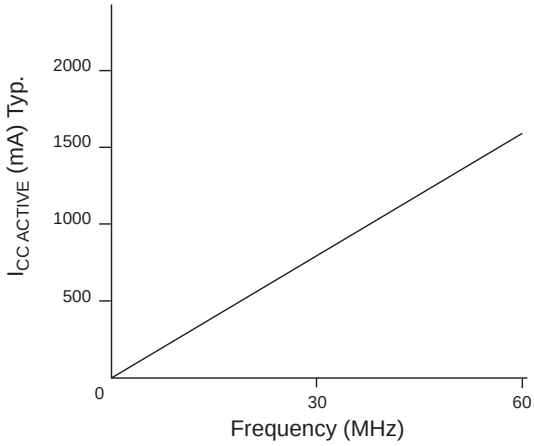
Notes to tables:

(1) All timing parameters are described in the *FLEX 10K Embedded Programmable Logic Family Data Sheet*.
(2) Using a logic element (LE) to register the signal may provide a lower setup time.
(3) This parameter is guaranteed by characterization.

Power Consumption

For details on computing power consumption for the EPF10K130V device, see the *FLEX 10K Embedded Programmable Logic Family Data Sheet* and *Application Note 74 (Evaluating Power for Altera Devices)* in the Altera ***1996 Data Book***. The required device-specific parameter for power computations is the constant K. The K value for the EPF10K130V device is 32. Figure 3 shows the relationship between the current and the operating frequency for an EPF10K130V device filled with 416 16-bit counters.

Figure 3. EPF10K130V $I_{CCACTIVE}$ vs. Operating Frequency



Device Configuration

FLEX 10K devices can be configured with 5.0-V EPC1 Configuration EPROMs, or with any passive configuration scheme using an intelligent host. EPC1 devices can operate with 3.3 or 5.0 V; the voltage level depends on the Programmer Object File (**.pof**) that is used to program the EPC1 device. When compiling an EPF10K130V design, MAX+PLUS® II automatically creates the POF to set the EPC1 Configuration EPROM for 3.3-V operation.

For more information on configuring EPF10K130V devices, refer to *Application Note 59 (Configuring FLEX 10K Devices)*.

Device Pin-Outs

Table 1 shows the pin names and numbers of the EPF10K130VGC599 device package.

Table 1. EPF10K130VGC599 Device Package Pin-Outs (Part 1 of 2) *Note (1)*

Pin Name	599-Pin PGA
MSEL0 *(2)*	F6
MSEL1 *(2)*	C3
nSTATUS *(2)*	E43
nCONFIG *(2)*	B4
DCLK *(2)*	BE5
CONF_DONE *(2)*	BC43
INIT_DONE *(4)*	AM40
nCE *(2)*	BB6
nCEO *(2)*	BF44
nWS *(3)*	BB40
nRS *(3)*	BA37
nCS *(3)*	AY38
CS *(3)*	BA39
RDYnBSY *(3)*	AW47
CLKUSR *(3)*	AY42
DATA7 *(3)*	BD14
DATA6 *(3)*	BA17
DATA5 *(3)*	BB16
DATA4 *(3)*	BF12
DATA3 *(3)*	BG11
DATA2 *(3)*	BG9
DATA1 *(3)*	BF10
DATA0 *(2)*	BC5
TDI *(2)*	BF4
TDO *(2)*	BB42
TCK *(2)*	BE43
TMS *(2)*	F42
nTRST *(2)*	B46
Dedicated Inputs	B24, C25, BG25, BG23
GCLK0	BF24
GCLK1	A25
DEV_CLRn *(4)*	BE23
DEV_OE *(4)*	BC25

Table 1. EPF10K130VGC599 Device Package Pin-Outs (Part 2 of 2) Note (1)	
Pin Name	**599-Pin PGA**
VCCINT	E5, A3, A45, C1, C11, C19, C29, C37, C47, G25, L3, L45, W3, W45, AJ3, AJ45, AU3, AU45, BE1, BE11, BE19, BE29, BE37, BE47, BG3, BG45
VCCIO	D24, E9, E15, E21, E27, E33, E39, G7, G41, J5, J43, R5, R43, AA5, AA43, AD4, AD44, AG5, AG43, AN5, AN43, AW5, AW43, BA7, BA41, BC9, BC15, BC21, BC27, BC33, BC39, BD24
GNDINT	A47, B2, C13, C21, C27, C35, C45, D4, G23, N3, N45, AA3, AA45, AG3, AG45, AR3, AR45, BD44, BE3, BE13, BE21, BE27, BE35, BE45, BG1, BG47
GNDIO	E7, E13, E19, E29, E35, E41, F24, G5, G43, H40, N5, W5, W43, AD6, AD42, AJ5, AJ43, AR5, AR43, AY8, AY40, BA5, BA43, BB24, BC7, BC13, BC19, BC29, BC35, BC41, N43
Total User I/O Pins	470

Notes:
(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin after configuration.
(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

Package Outlines

Figure 4 shows the package outline for the 599-pin PGA package.

Package outline dimensions are shown in the following formats:

min. inches (min. millimeters)
max. inches (max. millimeters)

or:

nominal inches ± tolerance
(nominal millimeters ± tolerance)

or:

inches
(millimeters) BSC, Min., Max., Ref., Typ., R, Dia., Sq.

Table 2 shows the units used to describe package outline dimensions.

Table 2. Package Outline Units

Unit	Description
BSC	Basic. Represents theoretical exact dimension or dimension target.
Min.	Minimum dimension specified.
Max.	Maximum dimension specified.
Ref.	Reference. Represents dimension for reference use only. This value is not a device specification.
Typ.	Typical. Provided as a general value. This value is not a device specification.
R	Radius. Represents curve dimension.
Dia.	Diameter. Represents curve dimension.
Sq.	Square. Indicates a square feature for a package with equal length and width dimensions.

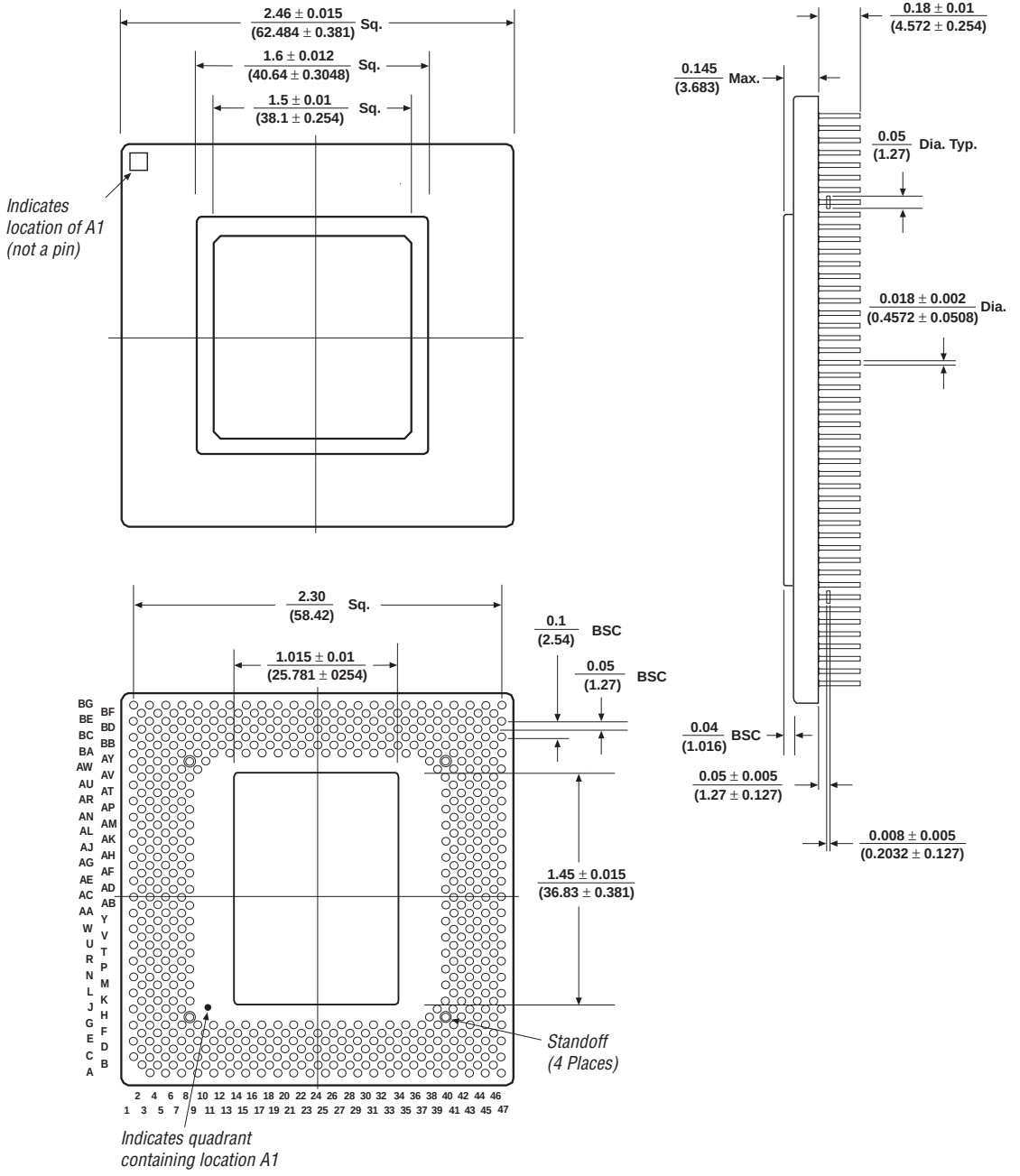
Table 3 lists the thermal resistance of EPF10K130V 599-pin PGA device packages.

Table 3. Thermal Resistance of EPF10K130V 599-Pin PGA Device Packages

Pin Count	Package	θ_{JC} (°C/W)	θ_{JA} (°C/W) Still Air	θ_{JA} (°C/W) 100 ft./min.	θ_{JA} (°C/W) 200 ft./min.	θ_{JA} (°C/W) 400 ft./min.
599	PGA	1	8	7	6	4

Figure 4. 599-Pin Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. Note: The EPF10K130V 599-pin PGA package weighs 69 grams.



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