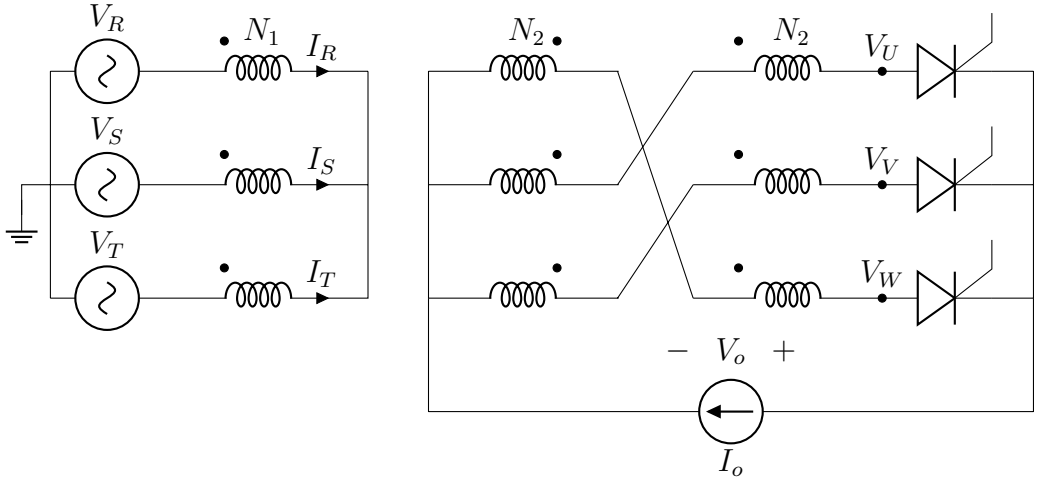
Examen de Electrónica de Potencia
8 de Diciembre de 2023

Problema 1 (50 puntos)

Sea el rectificador trifásico simple vía de la figura. Se asumirá que la corriente I_o es lisa. Para cada fase se cuenta con un transformador ideal de tres arrollamientos. Se controla el ángulo de disparo de tal forma que la potencia sobre la carga es P_o. La tensión de línea del sistema trifasico es U.

1) Calcular la relación de vueltas $\frac{N2}{N1}$ tal que las tensiones de fase RST y UVW tengan el mismo valor eficaz de tensión.
2) Dibujar el esquema fasorial de las tensiones de fase de los sistemas RST y UVW.
3) Dibujar la tensión V_o junto con las tensiones UVW.
4) Dibujar en el mismo referencial temporal de la parte anterior las corrientes de los sistemas trifásicos.
5) Suponiendo conocido el contenido armónico de la corriente I_U, calcular el contenido armónico de la corriente I_R.
6) Demostrar que las corrientes I_U o I_R no tienen terceros armónicos.

Datos: U= 230 V, P_o=10 kW y I_o= 84 A.



Problema 2 (50 puntos)

Se dispone de un convertidor Flyback que funciona con un control PWM a 100 kHz que admite un ciclo de trabajo δ máximo de 0,5. Ha sido diseñado para funcionar en modo de conducción discontinua para alimentar una carga máxima de 5 A en 24 V. La alimentación proviene de una batería cuya tensión puede variar entre 150 V y 250 V. La llave del convertidor es un MOSFET IRFPE50 y se ha montado sobre un disipador cuya resistencia térmica es 2 ºC/W. La temperatura ambiente máxima son 40 ºC.

1) Determine el valor de la inductancia del primario y del secundario para que el convertidor funcione según lo previsto.

   Por error, un usuario conecta una carga a la salida que consume el doble de la potencia para la que está diseñado el convertidor, cuando se tiene una tensión de baterías de 150 V.

2) Grafique la tensión y la corriente que circulará por el MOSFET en esa condición de funcionamiento. Indique valores de abscisas y ordenadas.

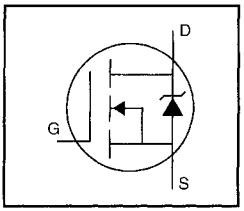
3) Determine si es posible que el MOSFET pueda soportar esa condición de funcionamiento en régimen permanente, asumiendo que el resto de los componentes del convertidor sí lo pueden hacer.

International IOR Rectifier

IRFPE50

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 800V

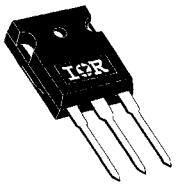
$R_{DS(on)}$ = 1.2Ω

I_D = 7.8A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial–industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.



TO-247AC

DATA SHEETS

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	7.8	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	4.9	
I_{DM}	Pulsed Drain Current ①	31	
P_D @ T_C = 25°C	Power Dissipation	190	W
	Linear Derating Factor	1.5	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	770	mJ
I_{AR}	Avalanche Current ①	7.8	A
E_{AR}	Repetitive Avalanche Energy ①	19	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.65	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	800	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.98	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.2	Ω	V_{GS}=10V, I_D=4.7A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	5.6	—	—	S	V_{DS}=100V, I_D=4.7A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	100	μA	V_{DS}=800V, V_{GS}=0V
		—	—	500		V_{DS}=640V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	200	nC	I_D=7.8A
Q_{gs}	Gate-to-Source Charge	—	—	24		V_{DS}=400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	110		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	19	—	ns	V_{DD}=400V
t_r	Rise Time	—	38	—		I_D=7.8A
$t_{d(off)}$	Turn-Off Delay Time	—	120	—		R_G=6.2Ω
t_f	Fall Time	—	39	—		R_D=52Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	3100	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	800	—		V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance	—	490	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	7.8	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	31		
V_{SD}	Diode Forward Voltage	—	—	1.8	V	T_J=25°C, I_S=7.8A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	650	980	ns	T_J=25°C, I_F=7.8A
Q_{rr}	Reverse Recovery Charge	—	3.8	5.7	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=50V, starting T_J=25°C, L=23mH R_G=25Ω, I_{AS}=7.8A (See Figure 12)

③ I_{SD}≤7.8A, di/dt≤140A/μs, V_{DD}≤600 , T_J≤150°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

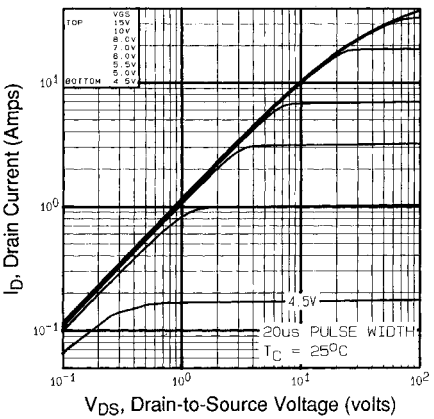


Fig 1. Typical Output Characteristics, T_C=25°C

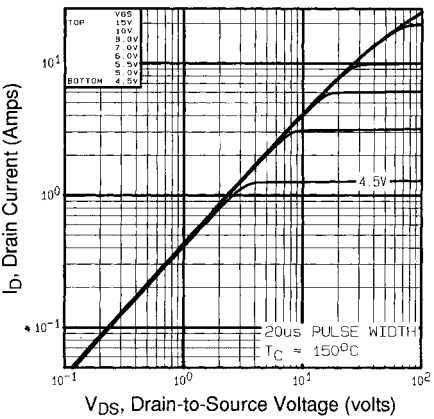


Fig 2. Typical Output Characteristics, T_C=150°C

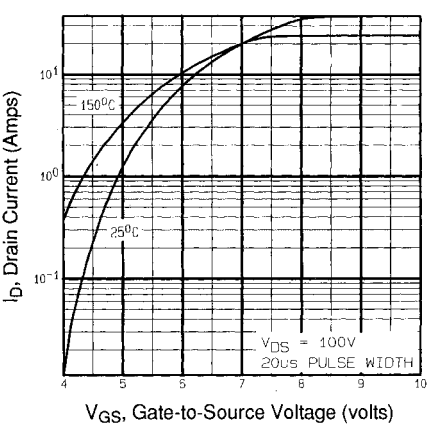


Fig 3. Typical Transfer Characteristics

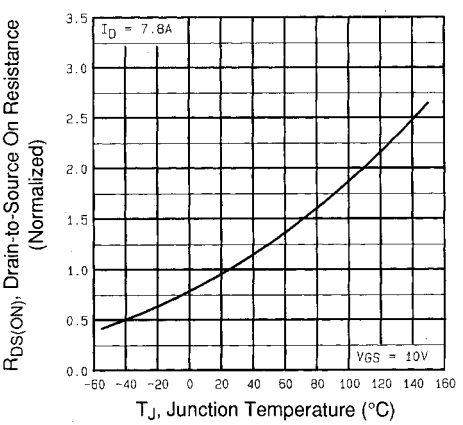


Fig 4. Normalized On-Resistance Vs. Temperature

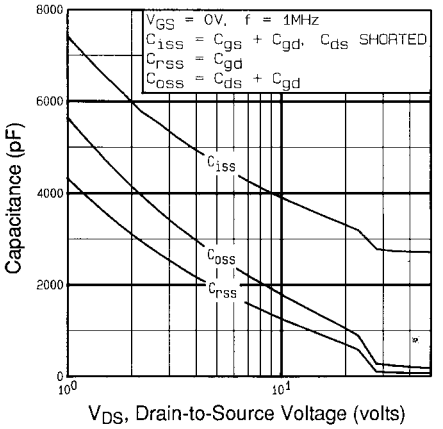


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

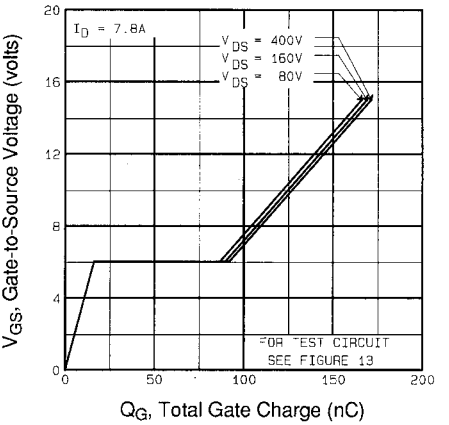


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

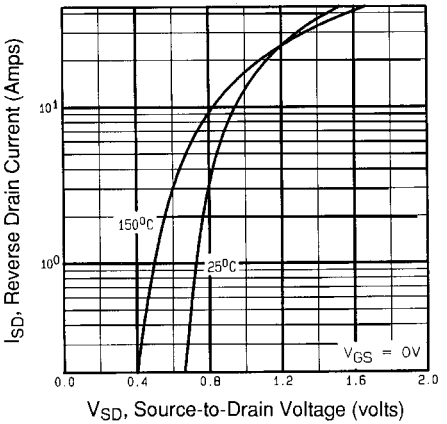


Fig 7. Typical Source-Drain Diode Forward Voltage

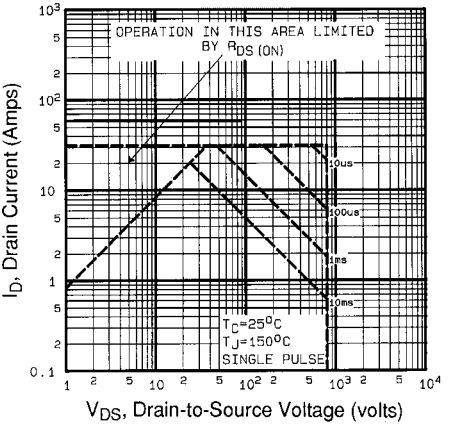


Fig 8. Maximum Safe Operating Area

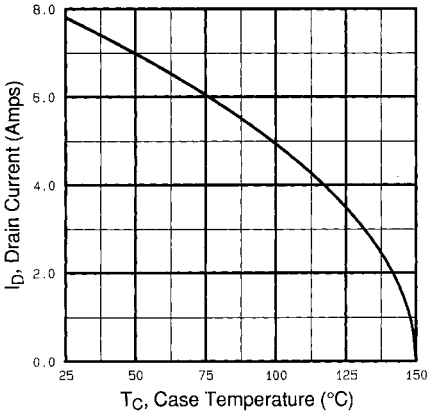


Fig 9. Maximum Drain Current Vs. Case Temperature

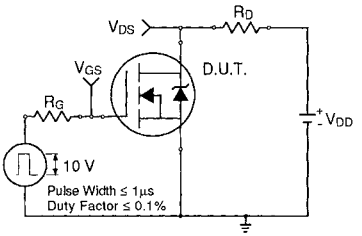


Fig 10a. Switching Time Test Circuit

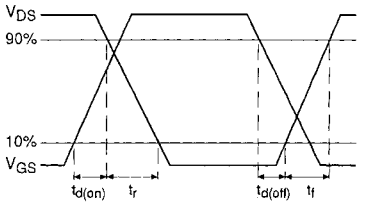


Fig 10b. Switching Time Waveforms

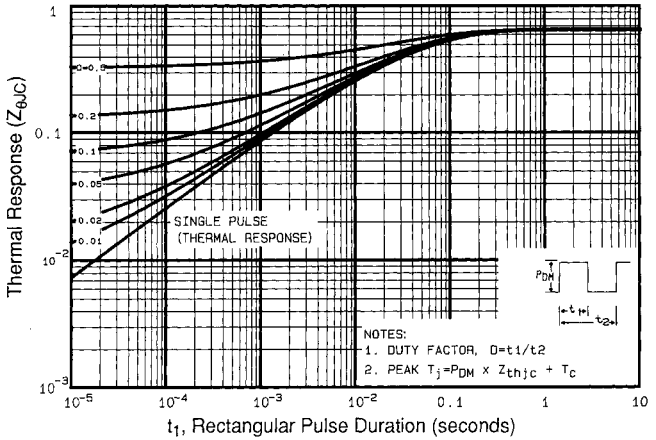


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

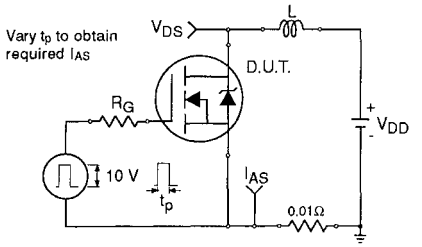


Fig 12a. Unclamped Inductive Test Circuit

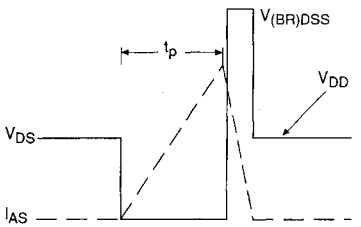


Fig 12b. Unclamped Inductive Waveforms

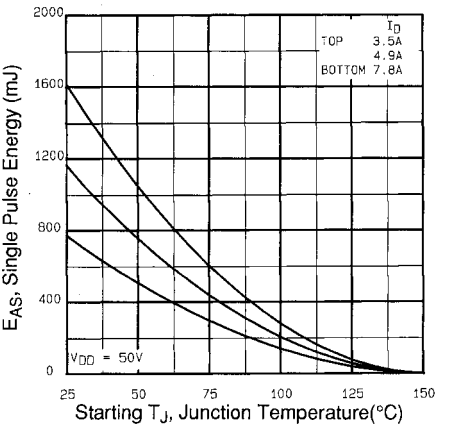


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

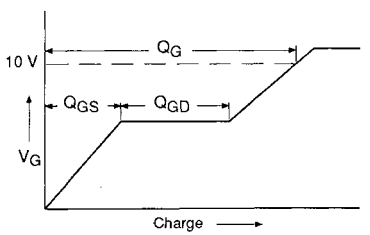


Fig 13a. Basic Gate Charge Waveform

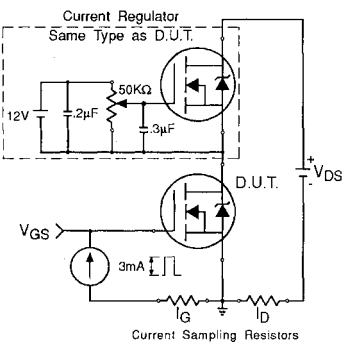


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1511

Appendix C: Part Marking Information – See page 1517

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