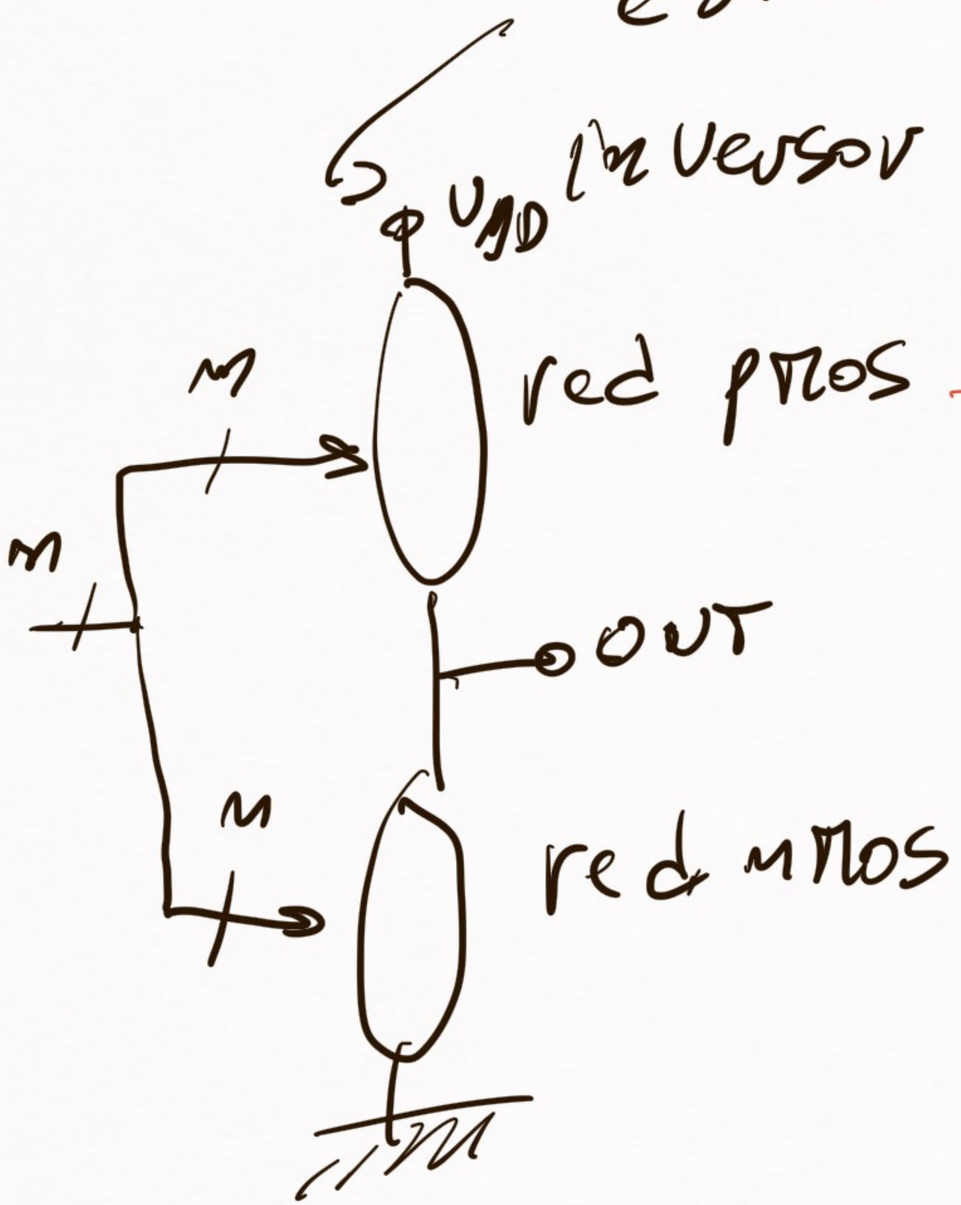
16/6/21

Puerta: Compuerta CMOS

estado lógico: "lógico estática"

Inversor generalizado:



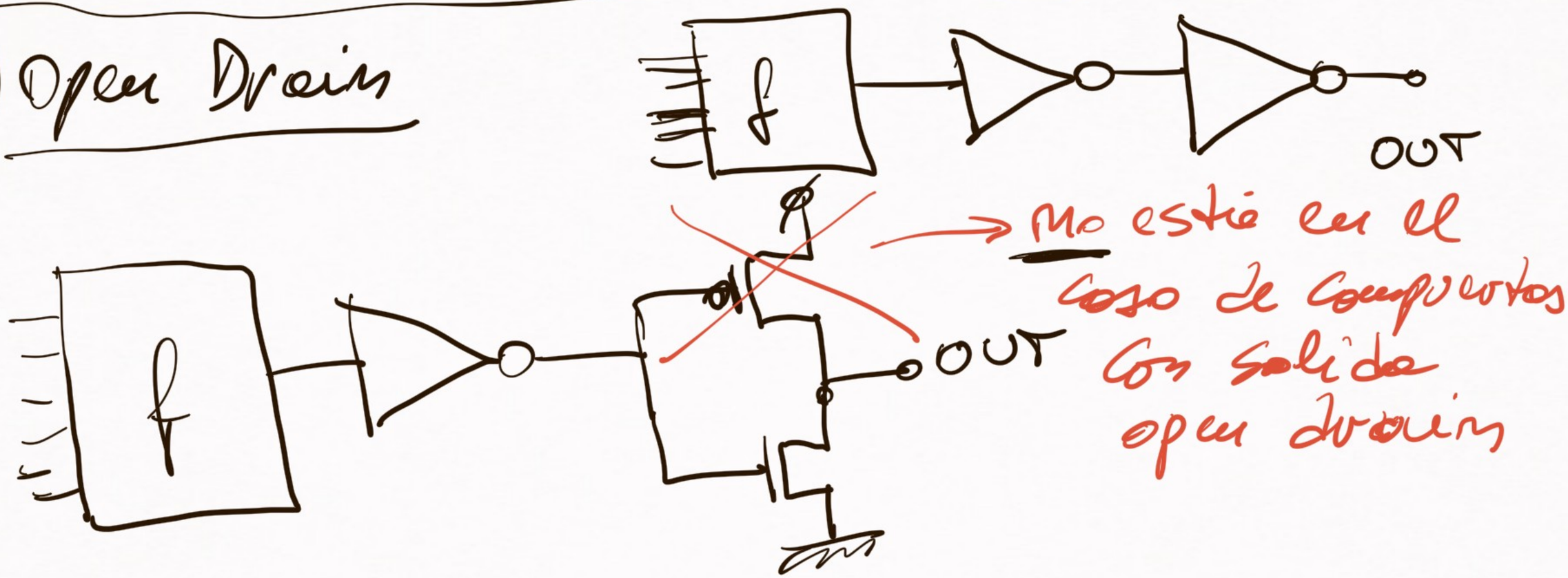
"duales":

paralelo ⟷ serie

Tipos especiales de compuertas

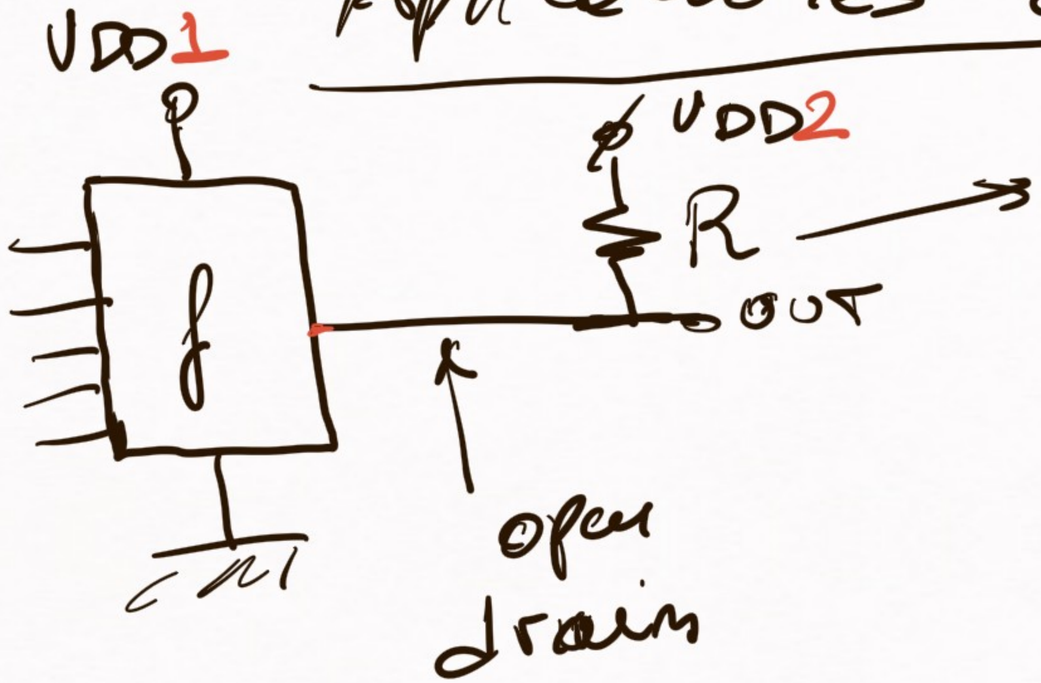
1) Open Drain (o open collector)
2) Tri-state (salida de 3er estado)

1) Open Drain



→ No está en el caso de compuertas con salida open drain

Aplicaciones de las salidas open drain

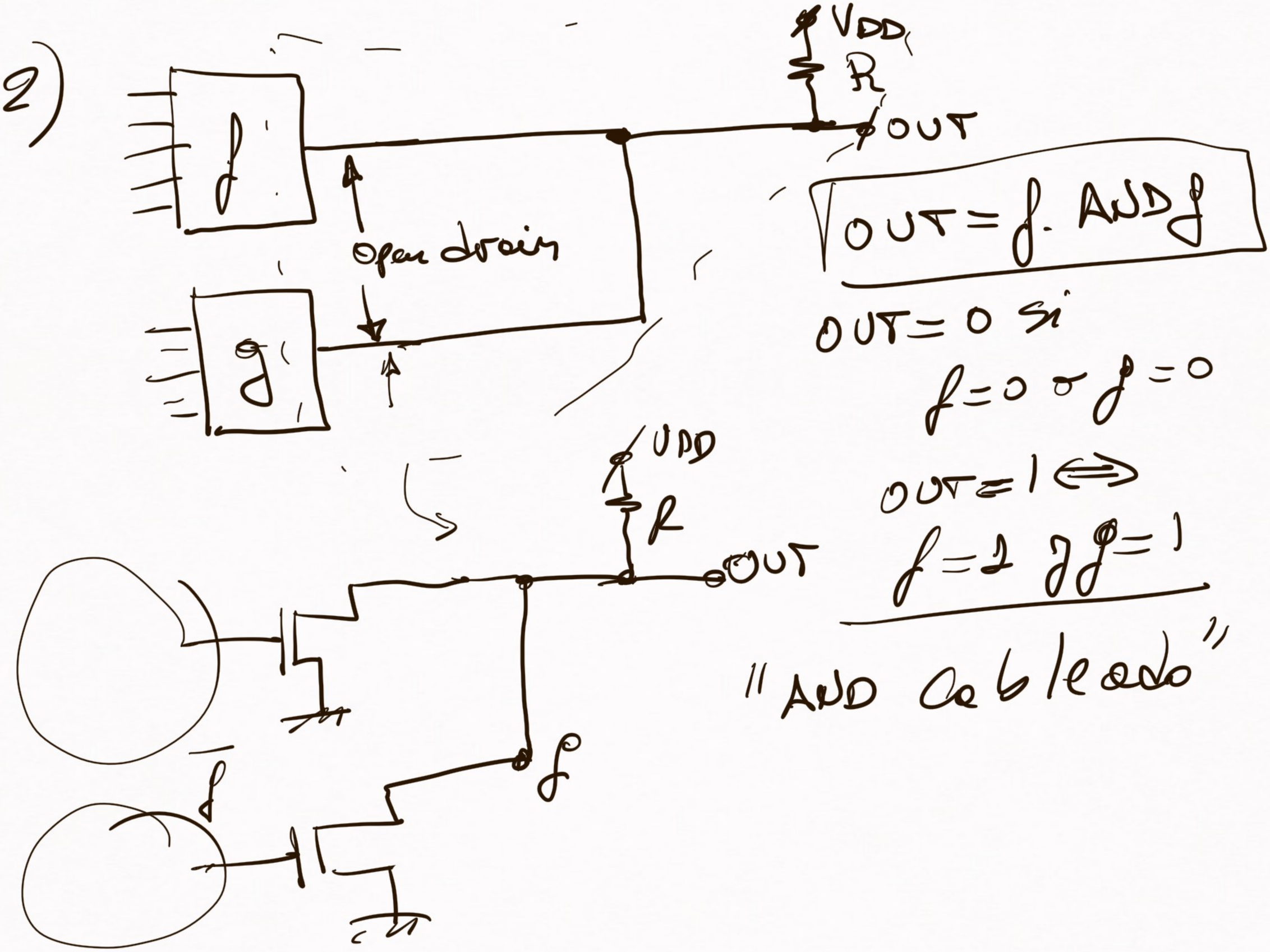


Resistencia de "pull up"

1) Conversión de niveles lógicos

Paso de $V_{OH} = V_{DD1}$ a $V_{OH} = V_{DD2}$

2)



$OUT = f \cdot AND\ g$

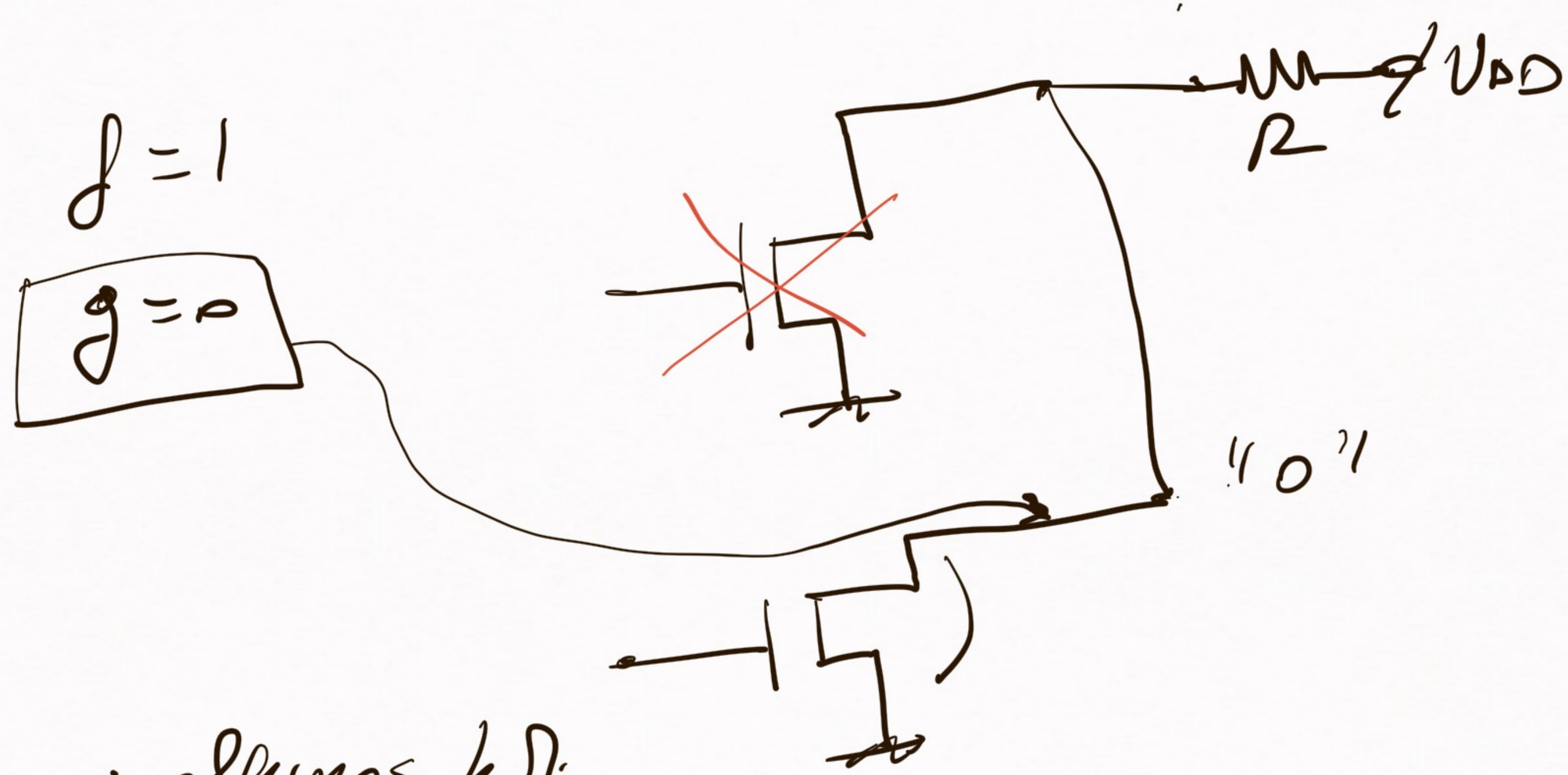
$OUT = 0$ Si

$f = 0$ o $g = 0$

$OUT = 1 \Leftrightarrow$

$f = 1$ y $g = 1$

"AND cableado"

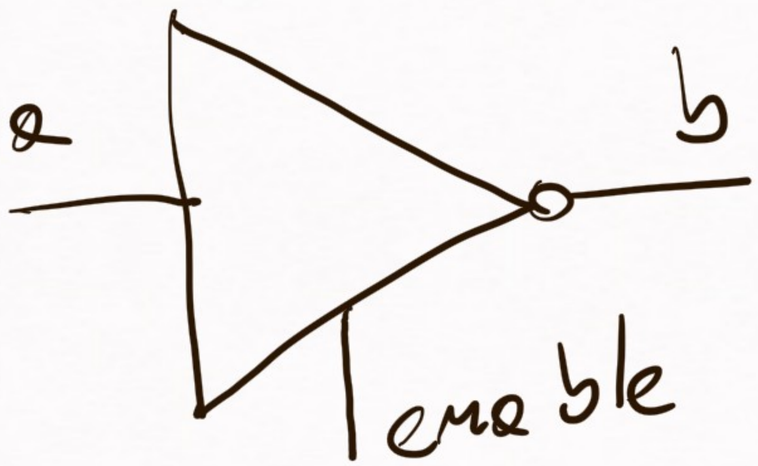


→ algunos kΩ.

R pull-up: → no ser demasiado chica para que el consumo con OUT = 0 no sea demasiado fuera de lo deseado.

→ R.C no sea demasiado alto.

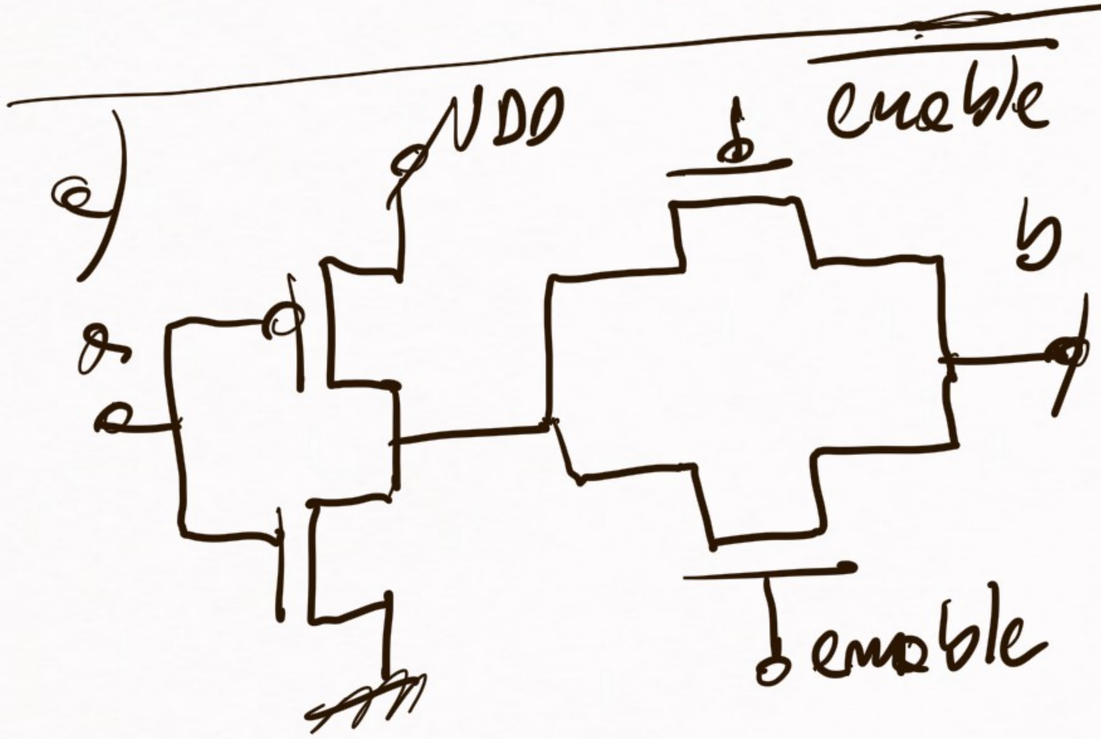
2) Componentes Tri-state
(salida en tercer estado)



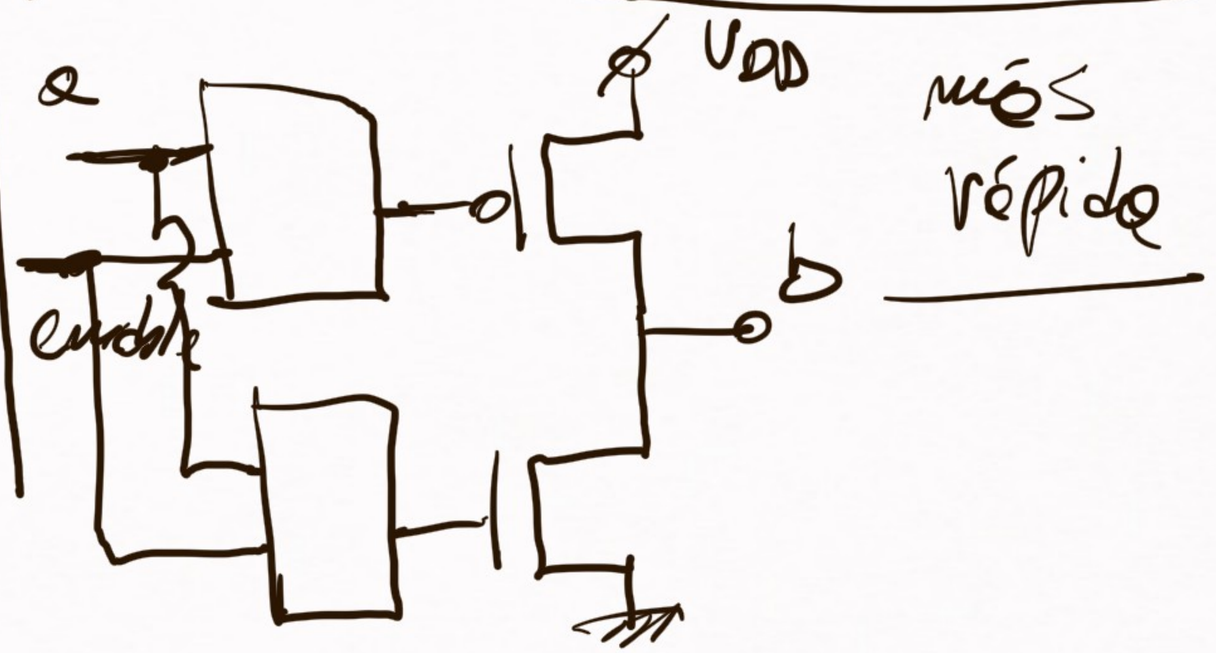
enable	
1	$b = \overline{a}$
0	b "alta impedancia" (High Z)

b: desconectado

a)

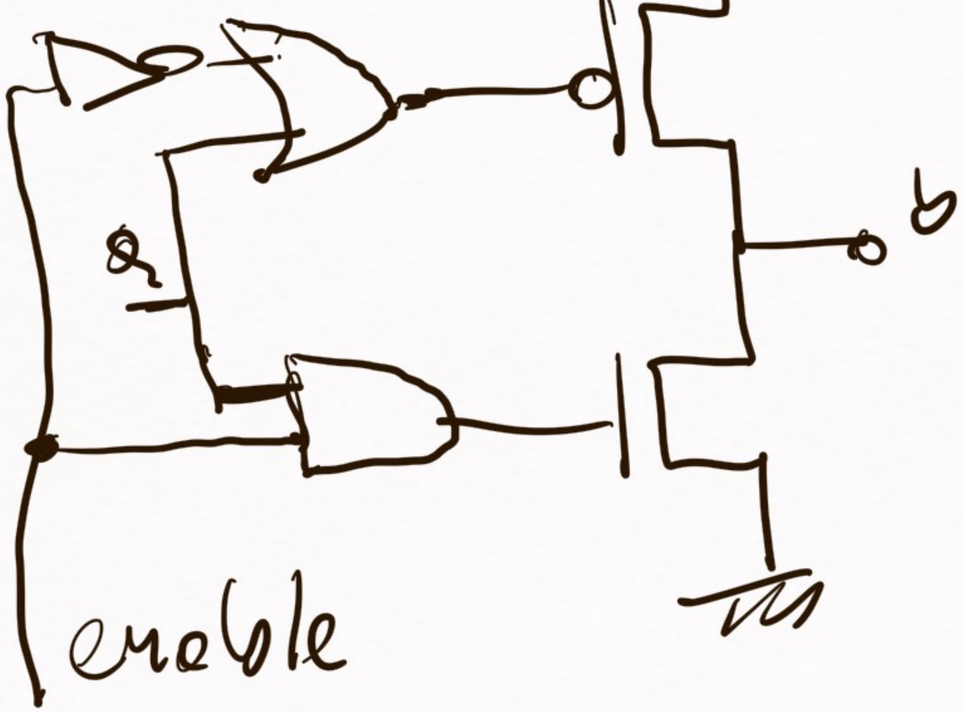


b)



más rápida

opção b):

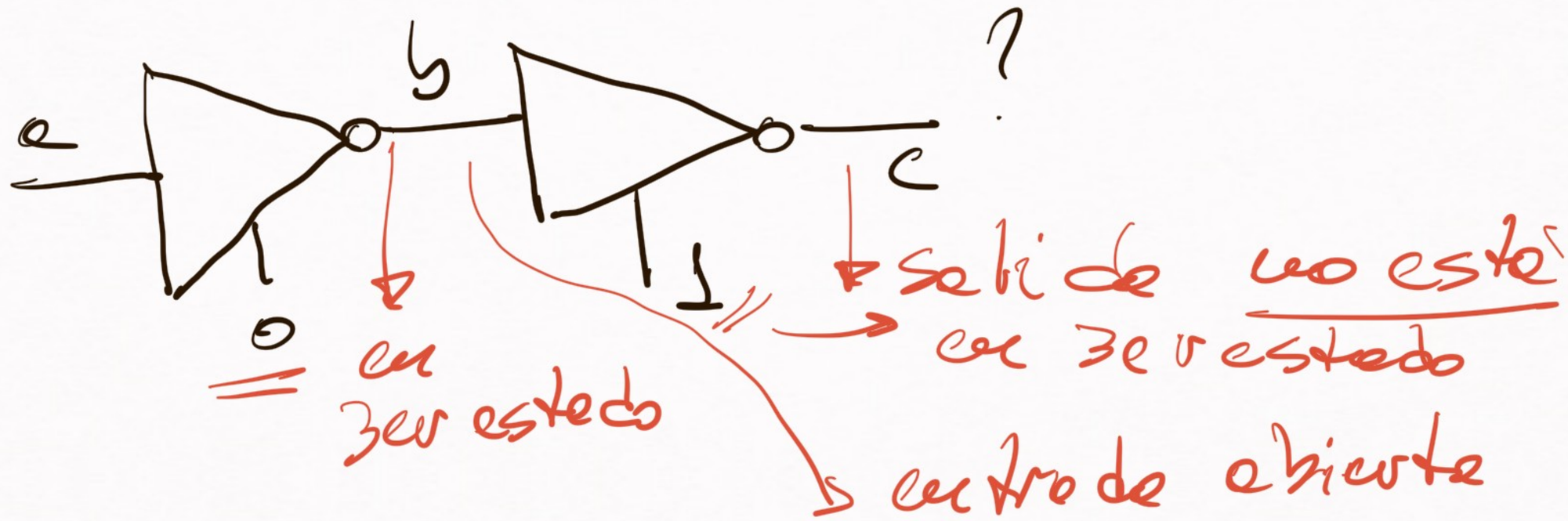


Gate p: $\begin{cases} a & enable = 1 \\ 1 & enable = 0 \end{cases}$

$Gate\ p = a + \overline{enable}$

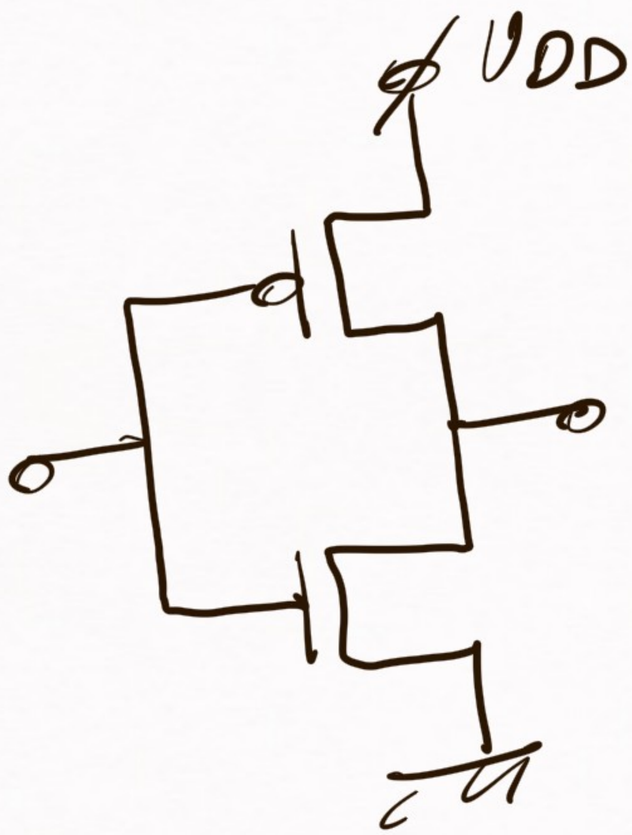
Gate M: $\begin{cases} a & enable = 1 \\ 0 & enable = 0 \end{cases}$

$Gate\ M = a . enable$



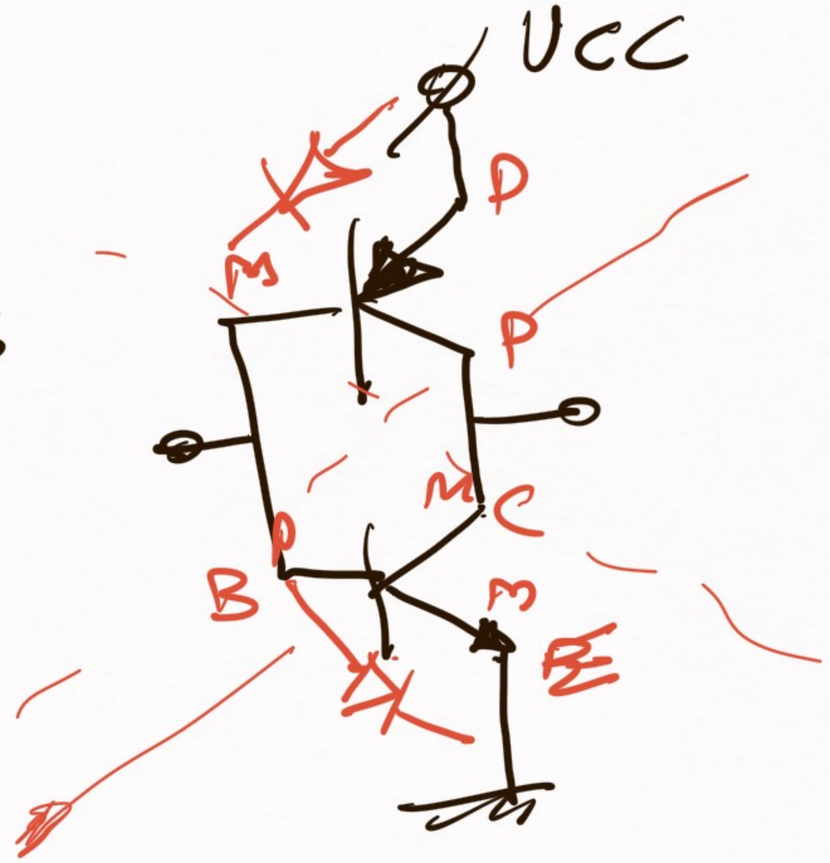
C: indeterminado, ruido, señal que varía entre 0 y 1 según que es lo que se capta a la entrada.

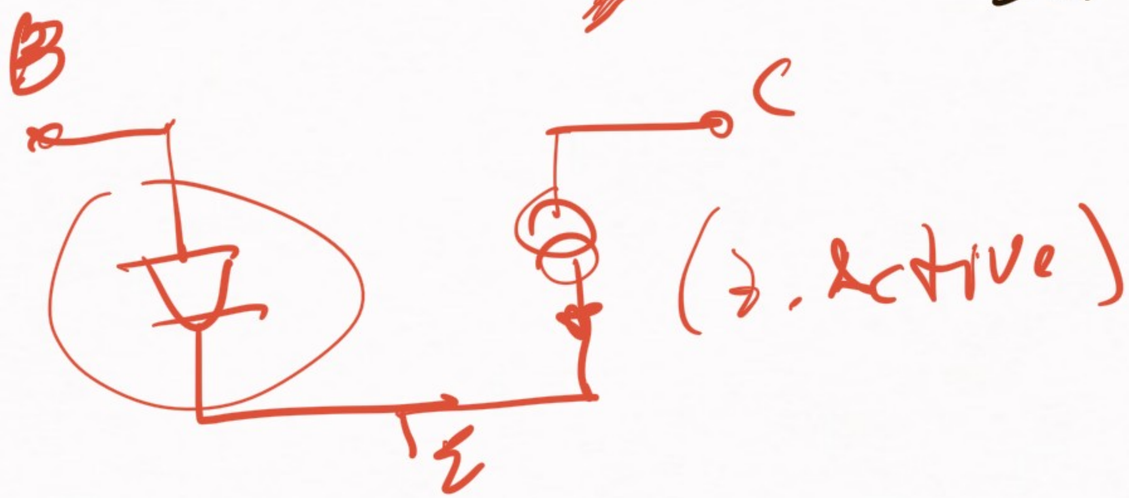
Lógica con transistores BJT



?

para lo demos
idea
a los BJT

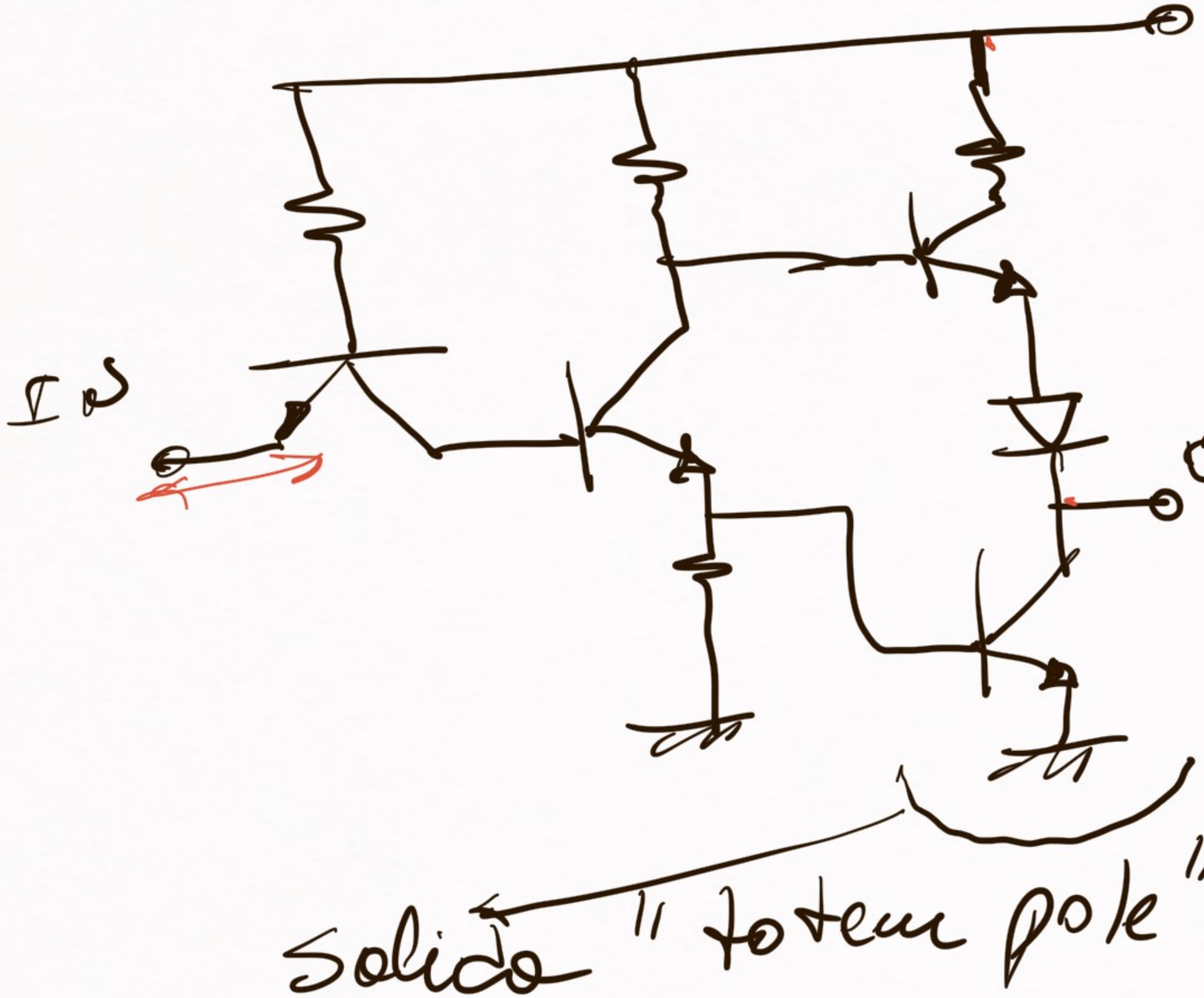




(→ Active)

⇒ lógica TTL: Transistor - Transistor

lógica: inversor TTL



	Min	Tip	Max	
V_{OL}		0.25	0.4	V
V_{OH}	2.7	3.5		
V_{IL}			0.8	
V_{IH}	2.0			