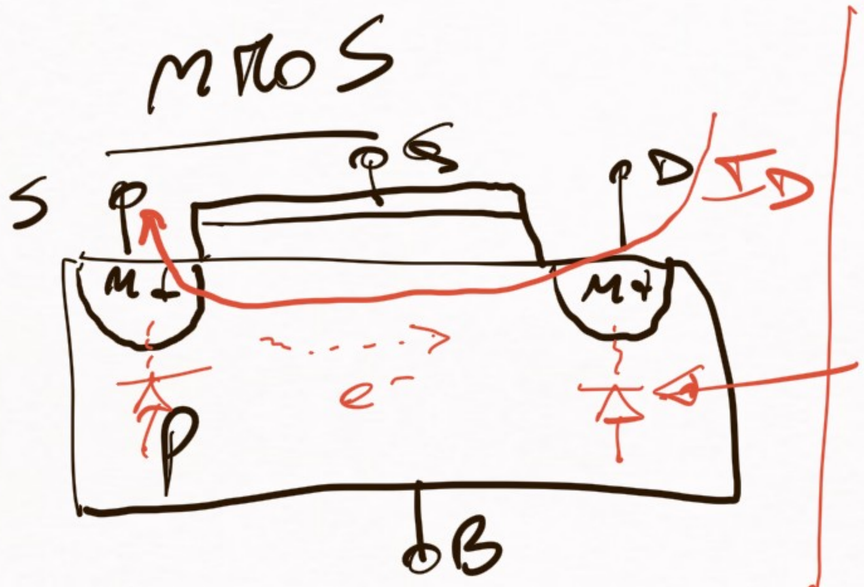
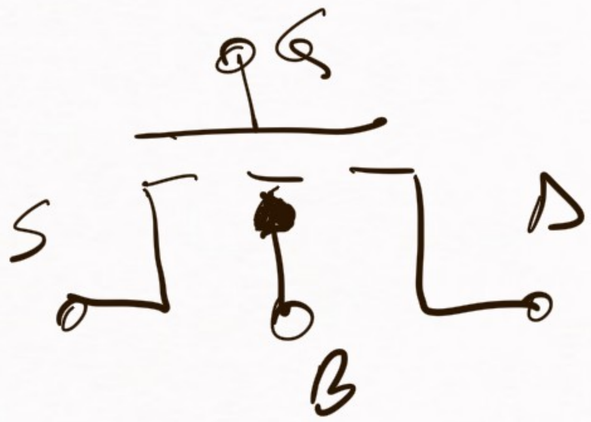
Transistor pMOS

nMOS

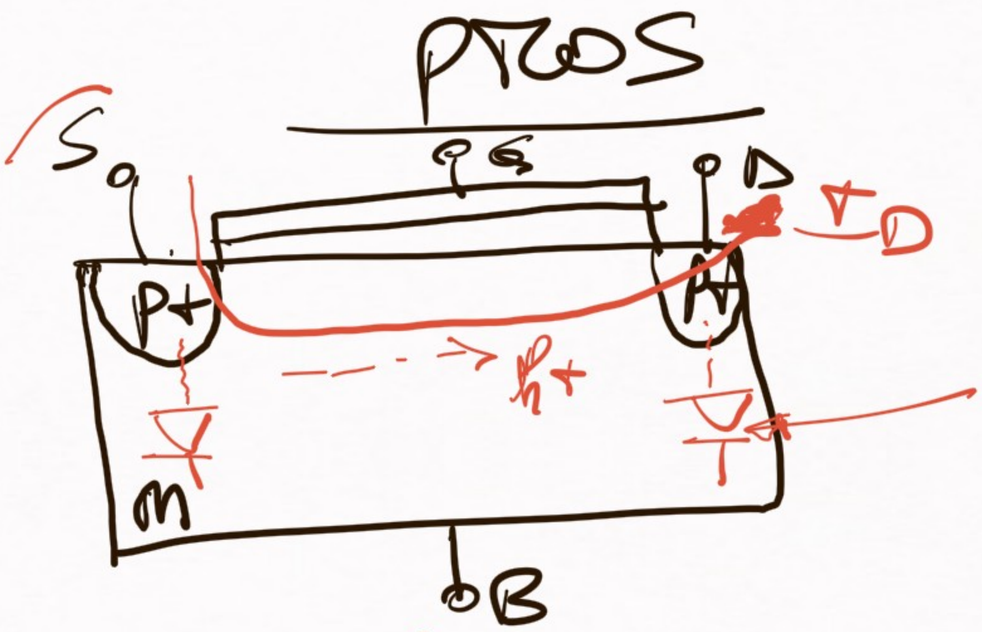


para que conduzca $V_{GB} > 0$

$V_{GB} > V_{to} + (1+\delta) V_{SB}$



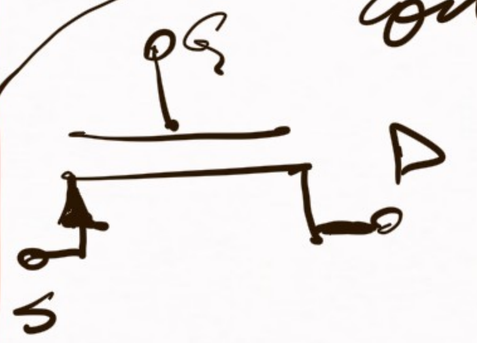
pMOS

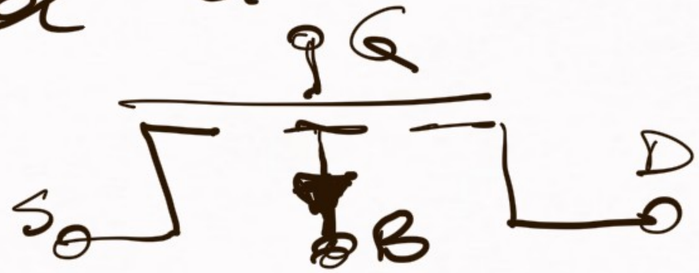


$V_{SB} \leq 0$ en operación normal

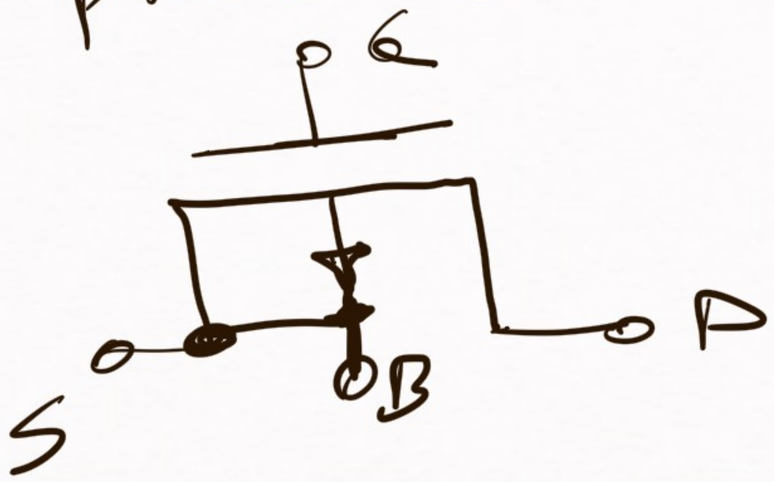
$V_{DB} \leq 0$

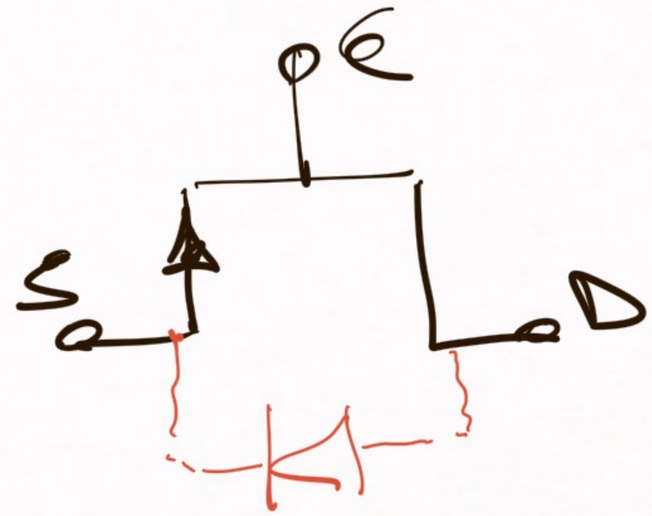
$V_{GB} < 0$ para formar el canal de inversión





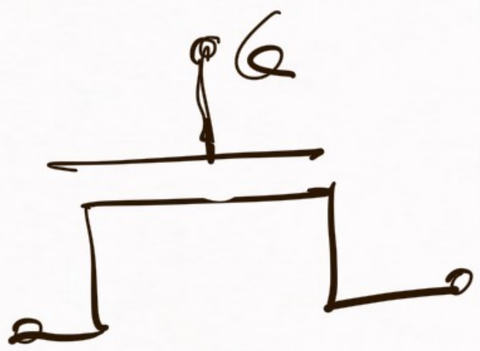
pMOS descubierto



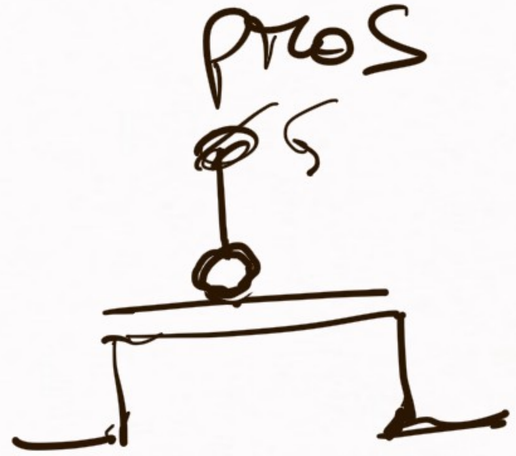


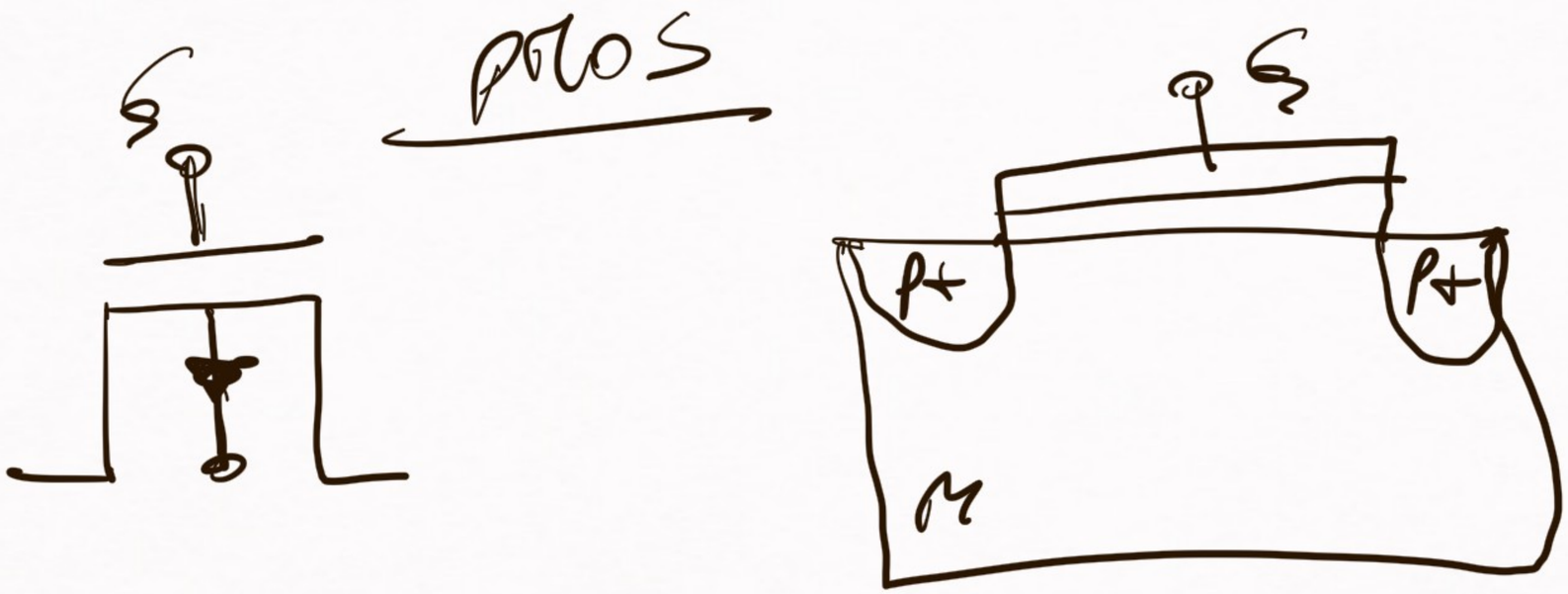
en contexto de circ. digitales

nMOS



pMOS





para p' conducir $V_{GB} < 0$, $V_{to} < 0$

$V_{SB}, V_{DB} \leq 0$

Ecs: Tomar las ecs del transistor nMOS

Conclusión: 1) Convierte Vo en sentido contrario (de S a D)

2) Variables son las opuestas:

$|V_{to}|, V_{BG}, V_{BS}, V_{BD} > 0$

Ej:

Ec. nMOS en saturación:

$$I_D = \frac{\beta}{2(1+\lambda)}\left(V_G - V_{to} - (1+\lambda)V_S\right)^2$$

V_S: V_{SB}

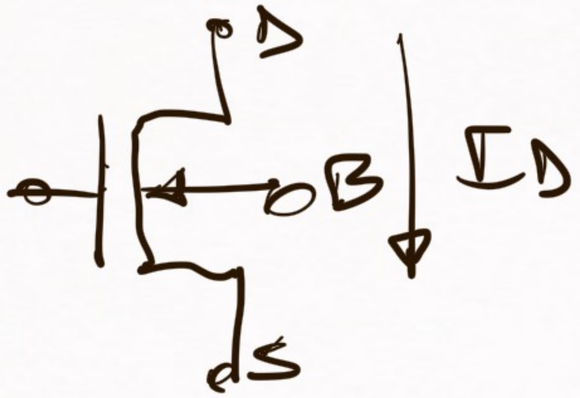
V_G: V_{GB}

$V_S < V_P$, $V_D > V_P$

V_D: V_{DB}

V_S: V_{SB}

$$V_P = \frac{V_G - V_{to}}{(1+\lambda)}$$



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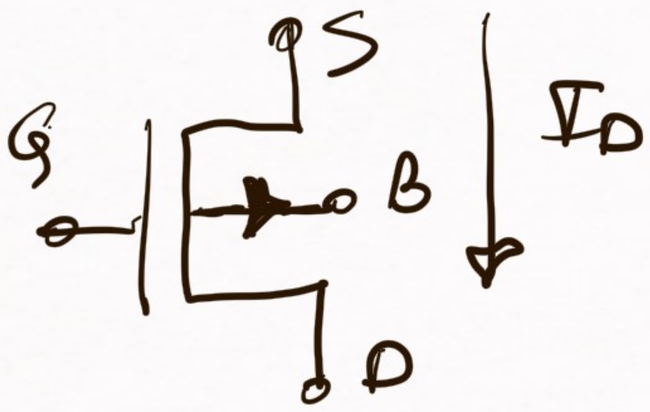
pMOS en saturación

$$I_D = \frac{\beta}{2(1+\lambda)}\left(V_{SG} - |V_{to}| - (1+\lambda)V_{SD}\right)^2$$



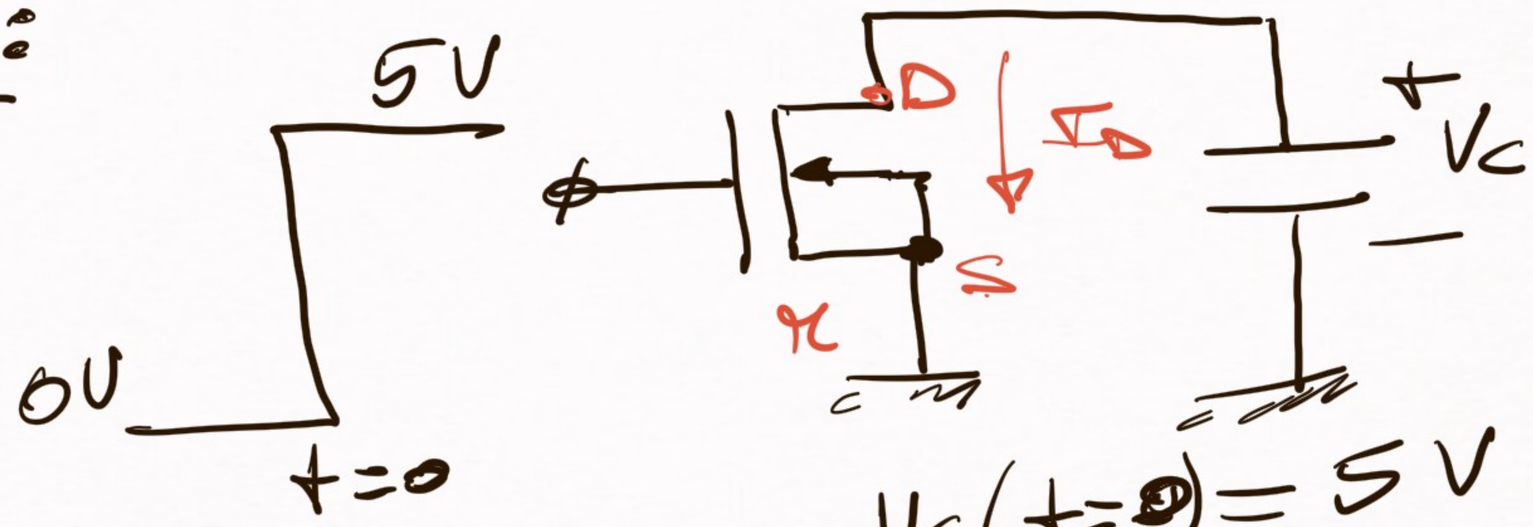
$V_{SD} < V_P$

$V_{SD} > V_P$

$$V_P = \frac{V_{SG} - |V_{to}|}{(1+\lambda)}$$

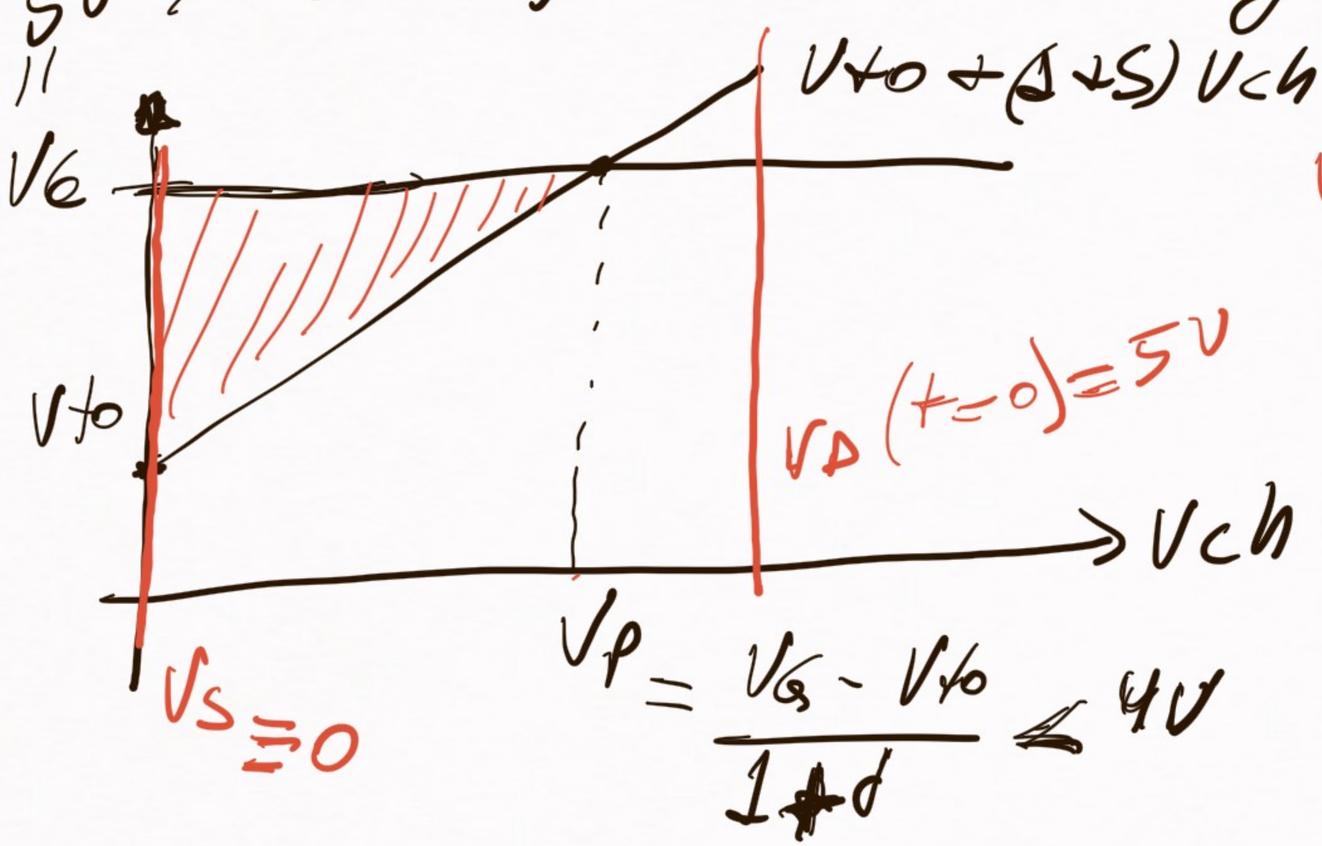
Ejercicio:

$V_{to} = 1V$



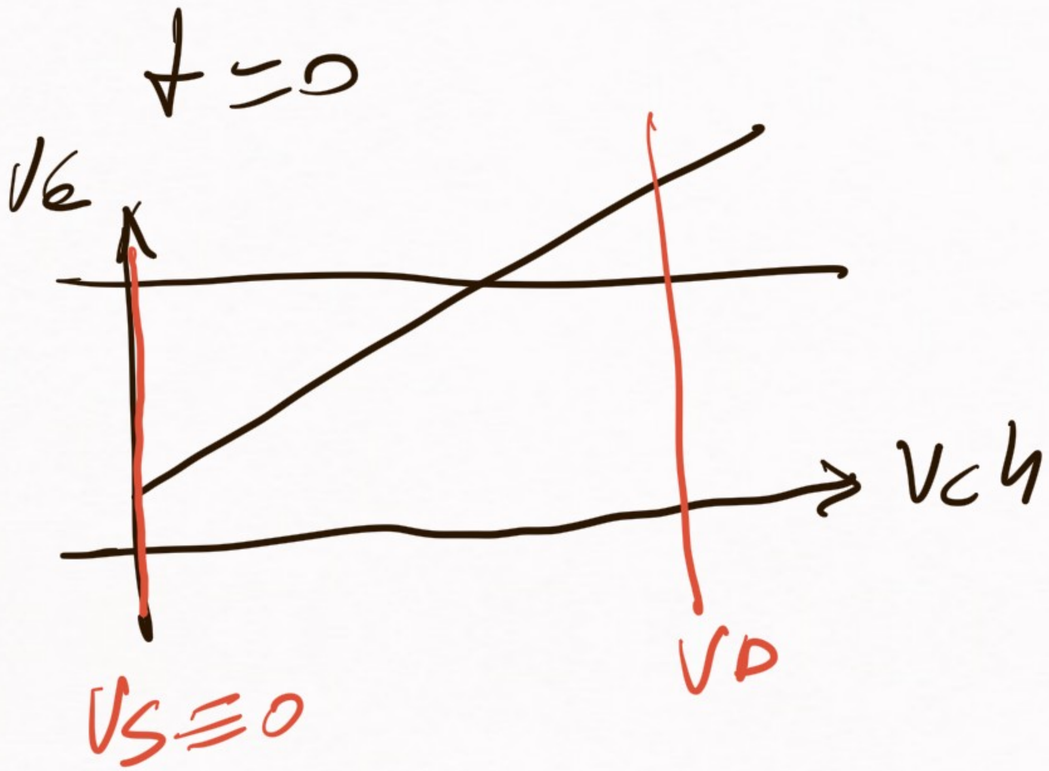
$V_C(t=0) = 5V$

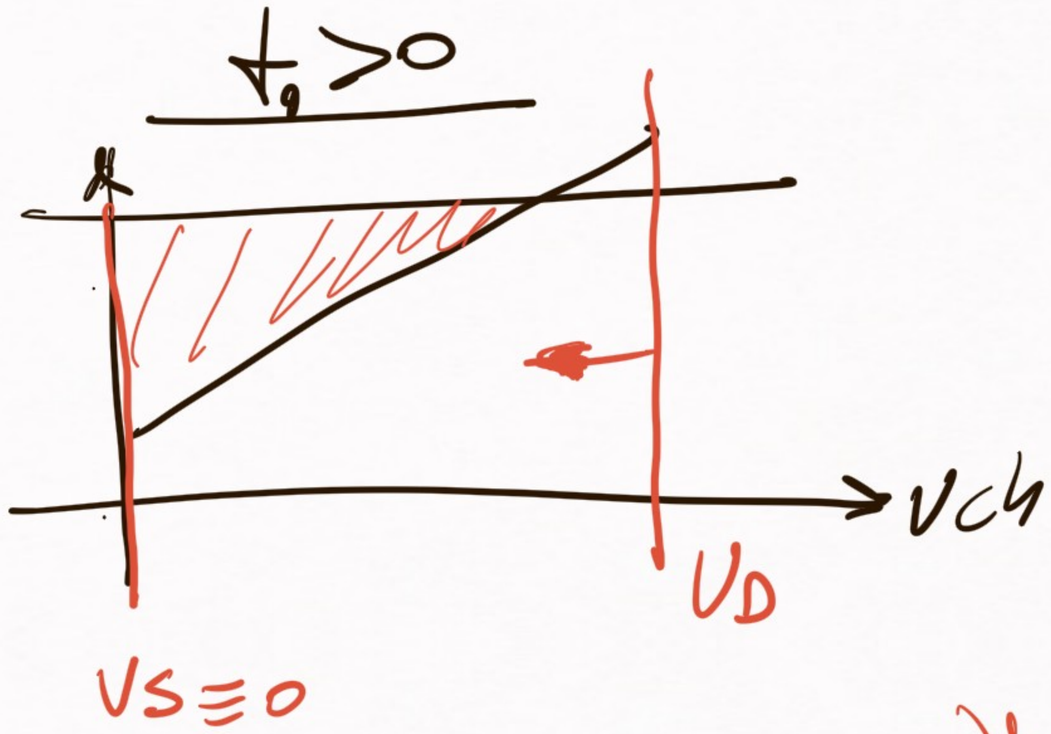
5V ¿cuál es la tensión final en el condensador?

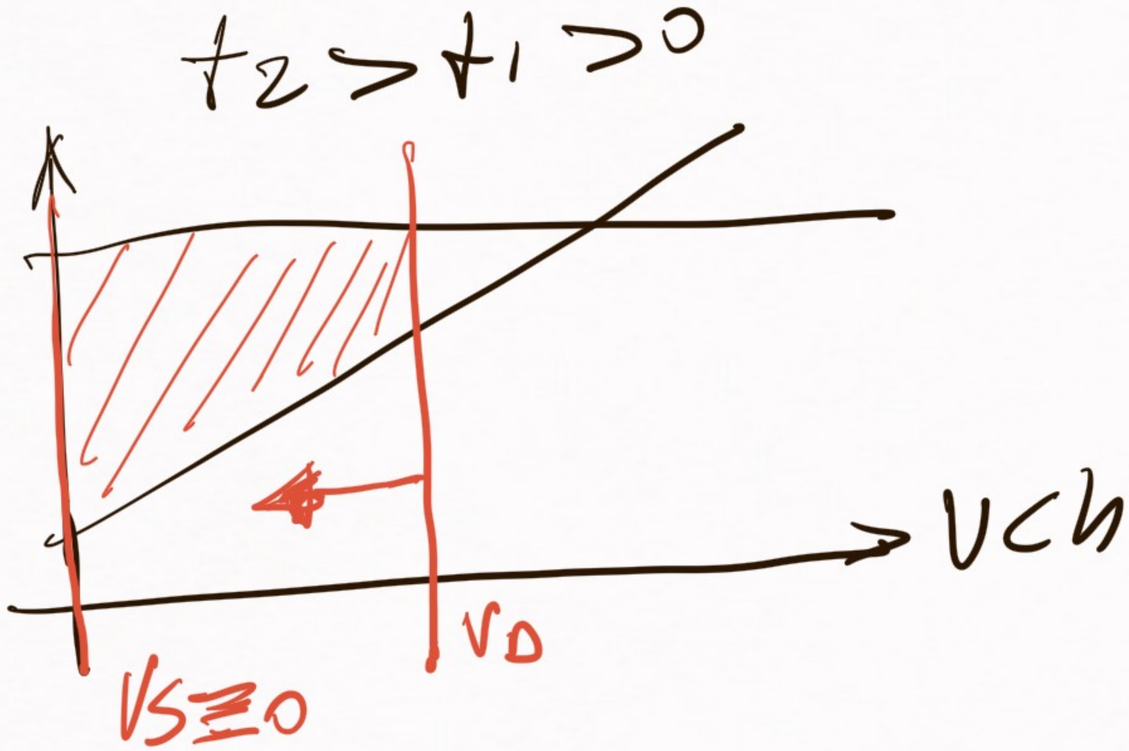


$V_D(t=0) > V_P$

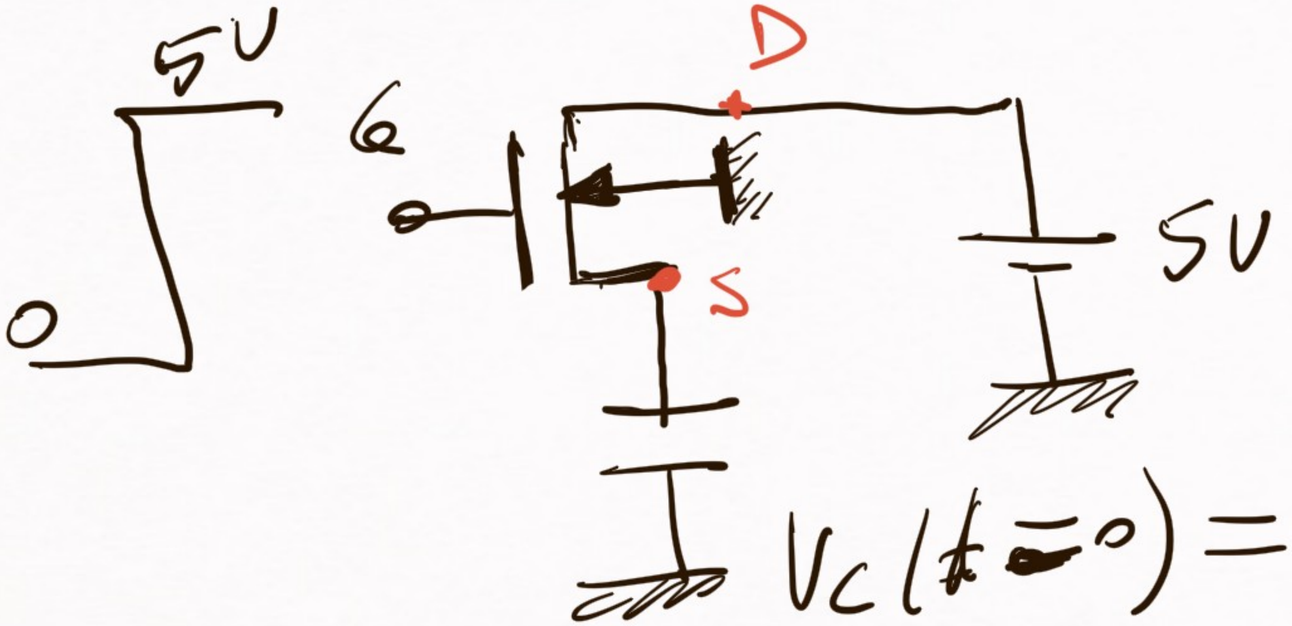
$\Rightarrow$ El setup no está en $t=0$


t = 0
VG
Vch
VD
VS ≡ 0


tg > 0
Vch
VD
VS ≡ 0

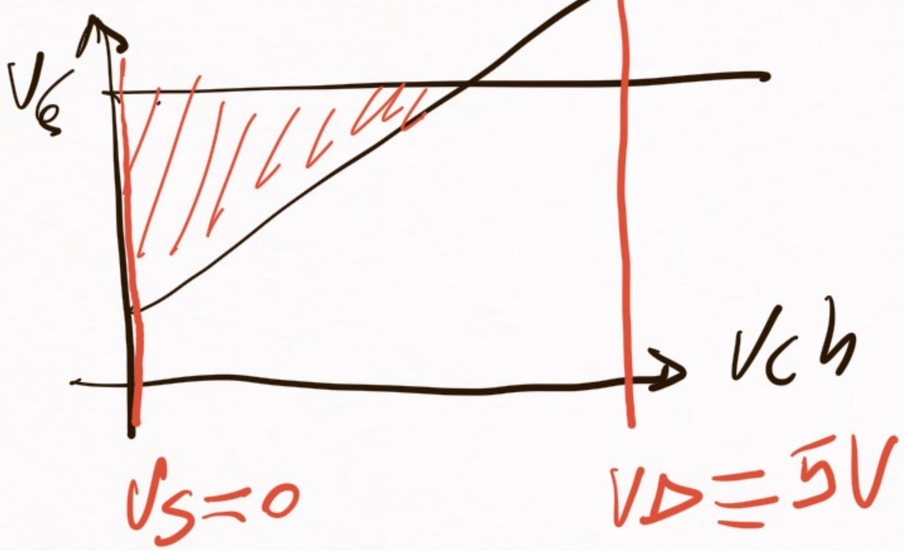

t2 > t1 > 0
Vch
VD
VS ≡ 0

VC → 0
t → ∞
descarga con I cte
VC
5V
VP
t

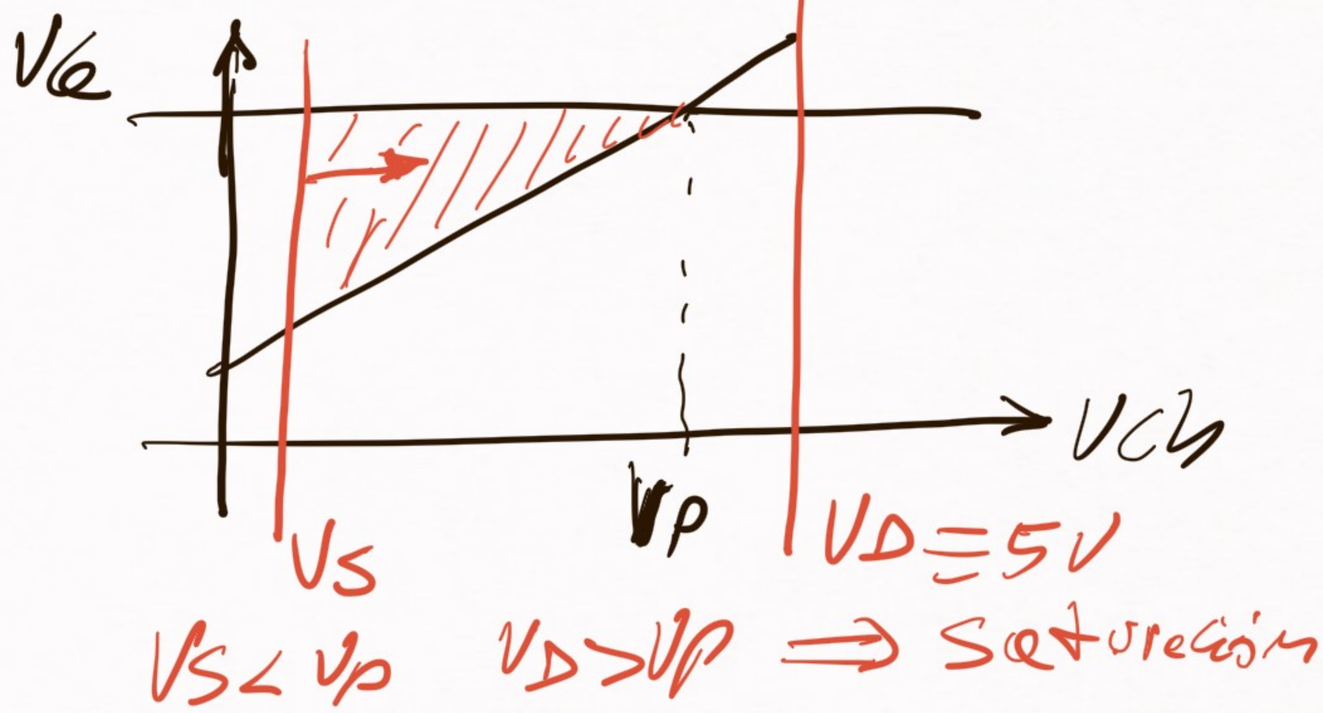


¿Cuánto vale la tensión final en el condensador?

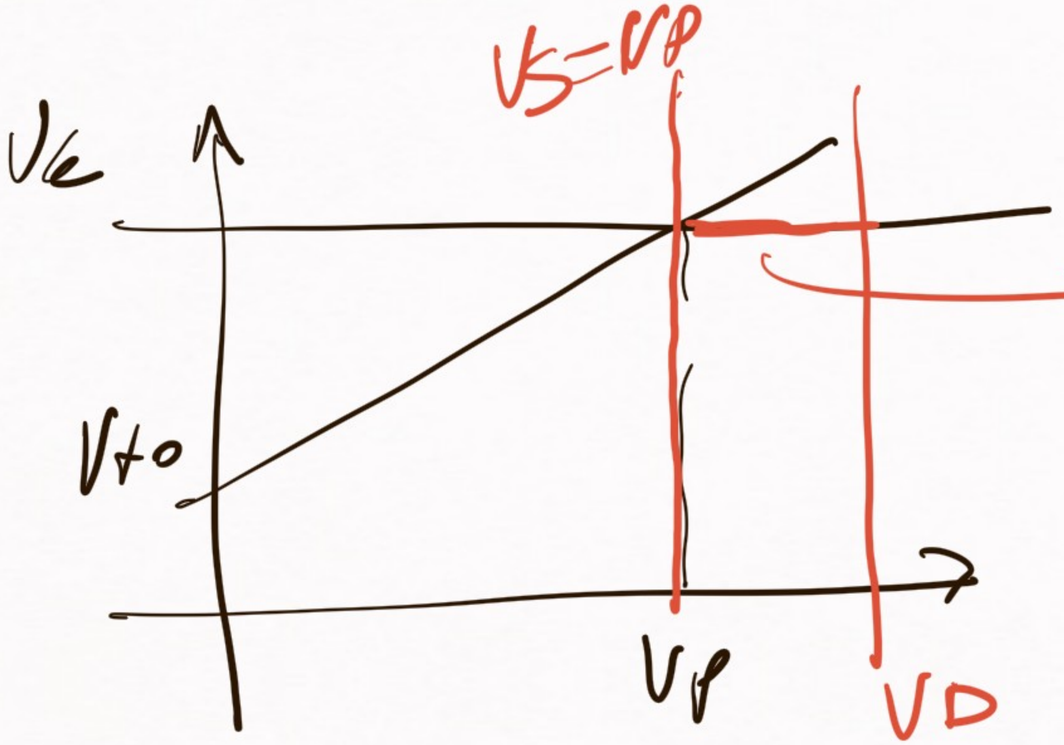
$t=0$



$t_1>0$



$V_S < V_P$ $V_D > V_P \Rightarrow$ Saturación



$I_D \cong 0$ (transistor cortado)

Modelo simplificado de cierre de EF:

$\Rightarrow$ Valor final de tensión de el $C = V_P$

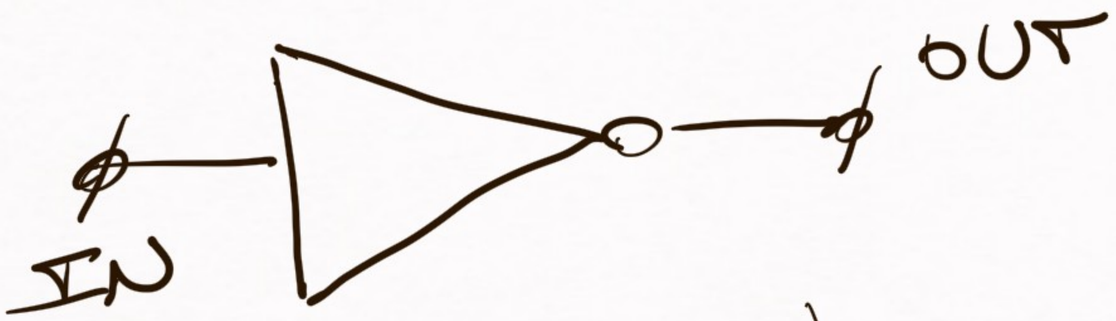
Inversely I_D muy pequeño pero $\neq 0 \Rightarrow C$ se fija cargando mucho más lentamente.

Moraleja: NMOS es bueno para descargar a tierra en C pero es malo para cargar a la fuente.

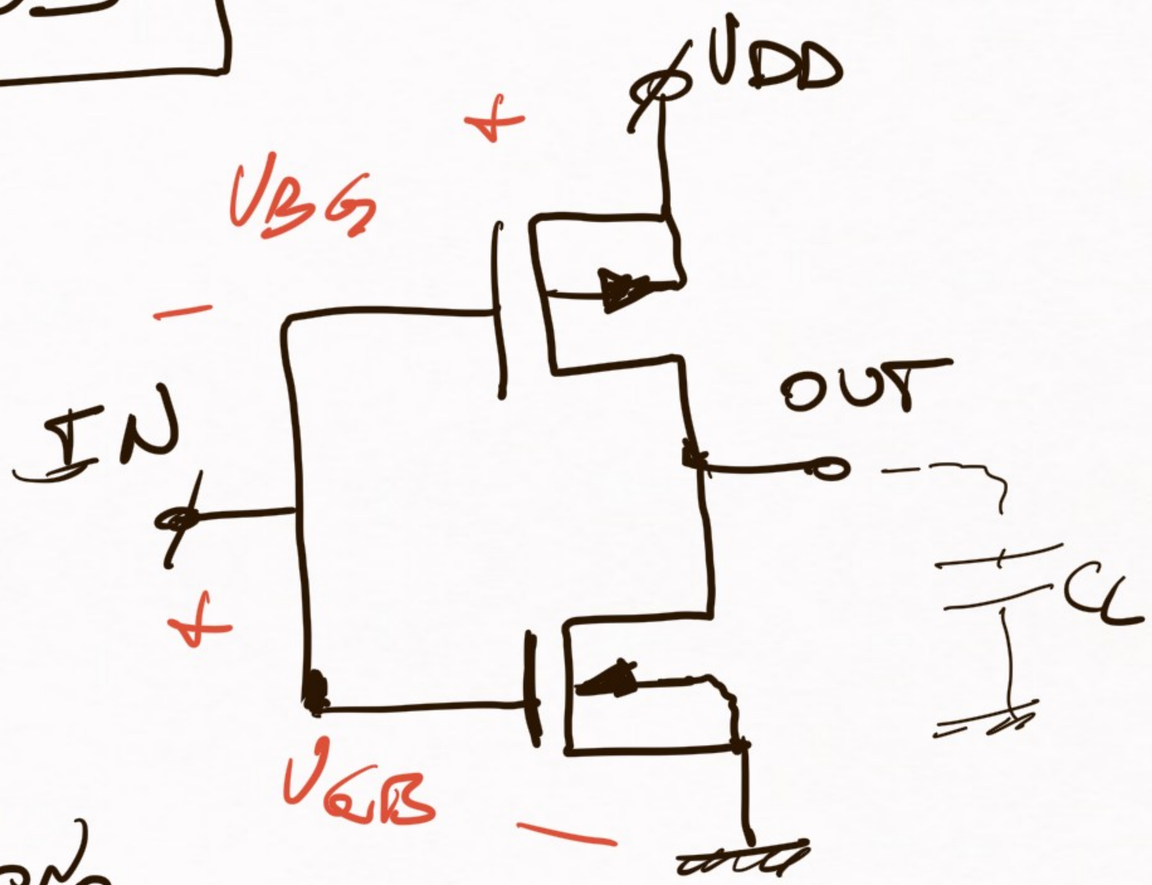
en PMOS ocurre lo inverso
es bueno para cargar a VDD y malo para descargar a tierra

⇒ en circ. digitales precisamos los dos ⇒ tecnología CMOS (complementary)

inversor CMOS



IN "alta" ($=V_{DD}$)

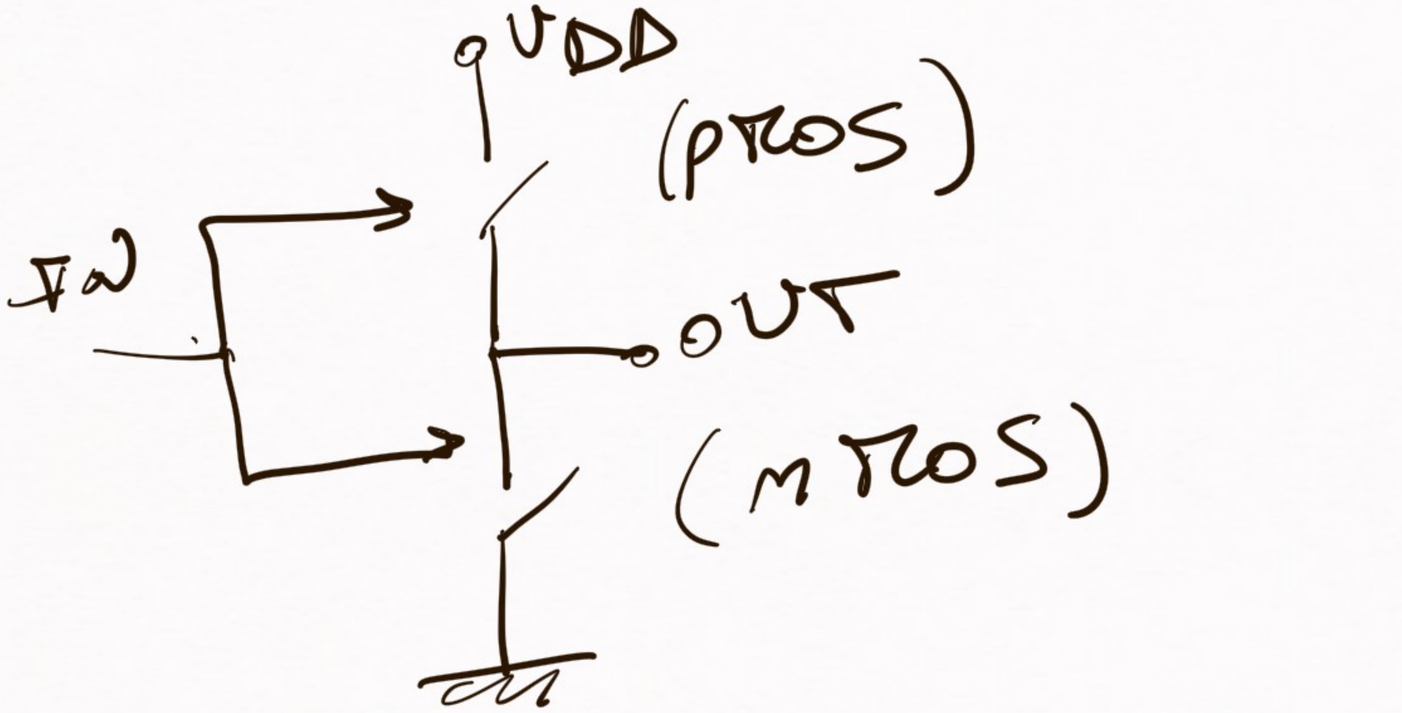


$V_{BG_{pmos}} = 0 \Rightarrow$ pMOS cortado

$V_{GB_{nmos}} = V_{DD} \Rightarrow$ nMOS conduce $\Rightarrow$ descarga OUT a ϕ

$\Rightarrow$ simetricamente para $\underline{IN = 0}$

Inversor CMOS



Prox. Nova aula

Ecs de transistor MOS: referidas al sustrato.

Variables: V_{GB}, V_{SB}, V_{DB} (nMOS)

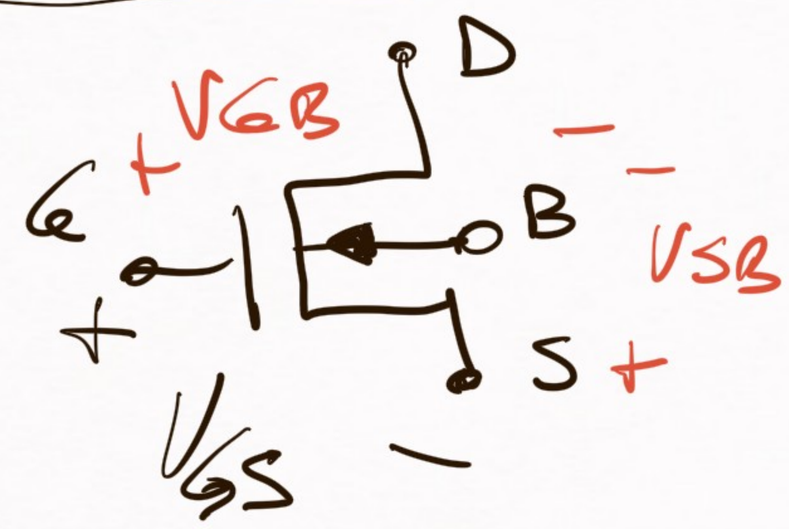
Alternativa:

Ecs. del transistor MOS referidas a la source:

Variables: (nMOS)

V_{GS}, V_{BS}, V_{DS}

V_{SB}

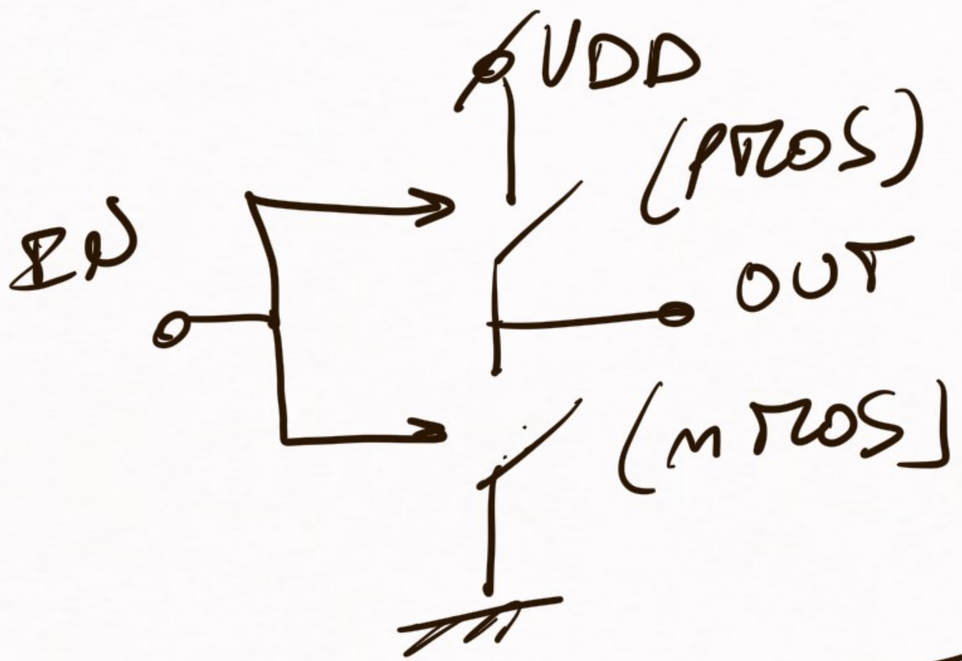


Malla

$\Rightarrow V_{GS} = V_{GB} - V_{SB}$

$V_{DS} = V_{DB} - V_{SB}$

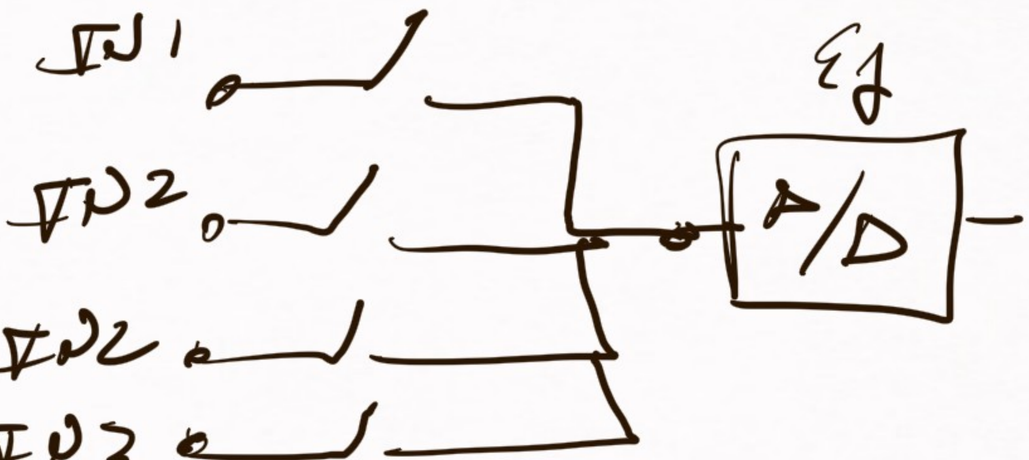
INVERSOR ("mundo digital")



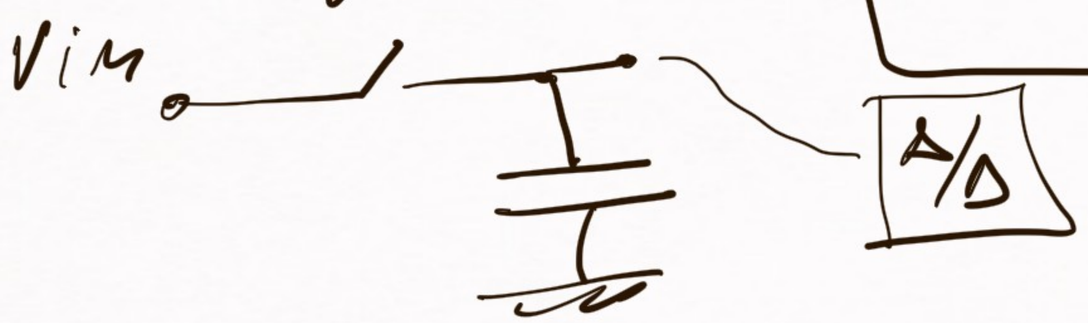
salida: 0 (tierra)
1 (VDD)

Mundo analógico:

Ej: Mux analógico:



Ej: sample and hold



VDD) PMOS

)?

0V) NMOS