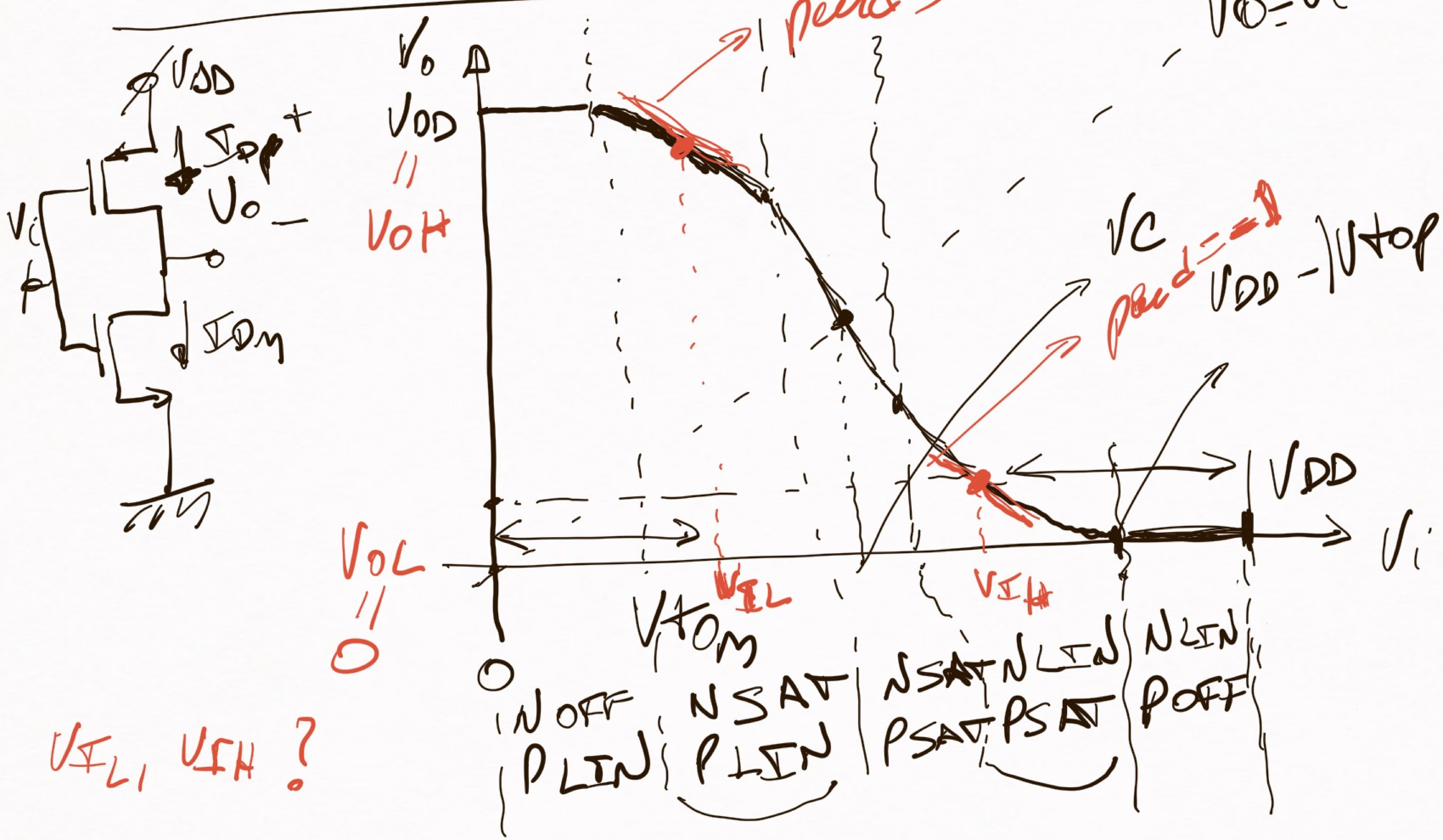
10/06/20

Inv. CMOS:

Caracteristica estática



VIL, VIH ?

$V_i = 0$: NMOS OFF $(V_i < V_{toN})$

$\rightarrow I_{D_N} = 0 \Rightarrow$ PLIN $\Rightarrow V_o = V_{DD}$

$\rightarrow I_{Dp} = 0 \Rightarrow V_{DSp} = 0$

Si transistores tienen características iguales: $V_{toN} = |V_{toP}|$, $\beta_N = \beta_P$, $\delta_N = \delta_P$

$$\Updownarrow$$

$$\mu_N \left(\frac{W}{L}\right)_N = \left(\frac{W}{L}\right)_P \mu_P$$

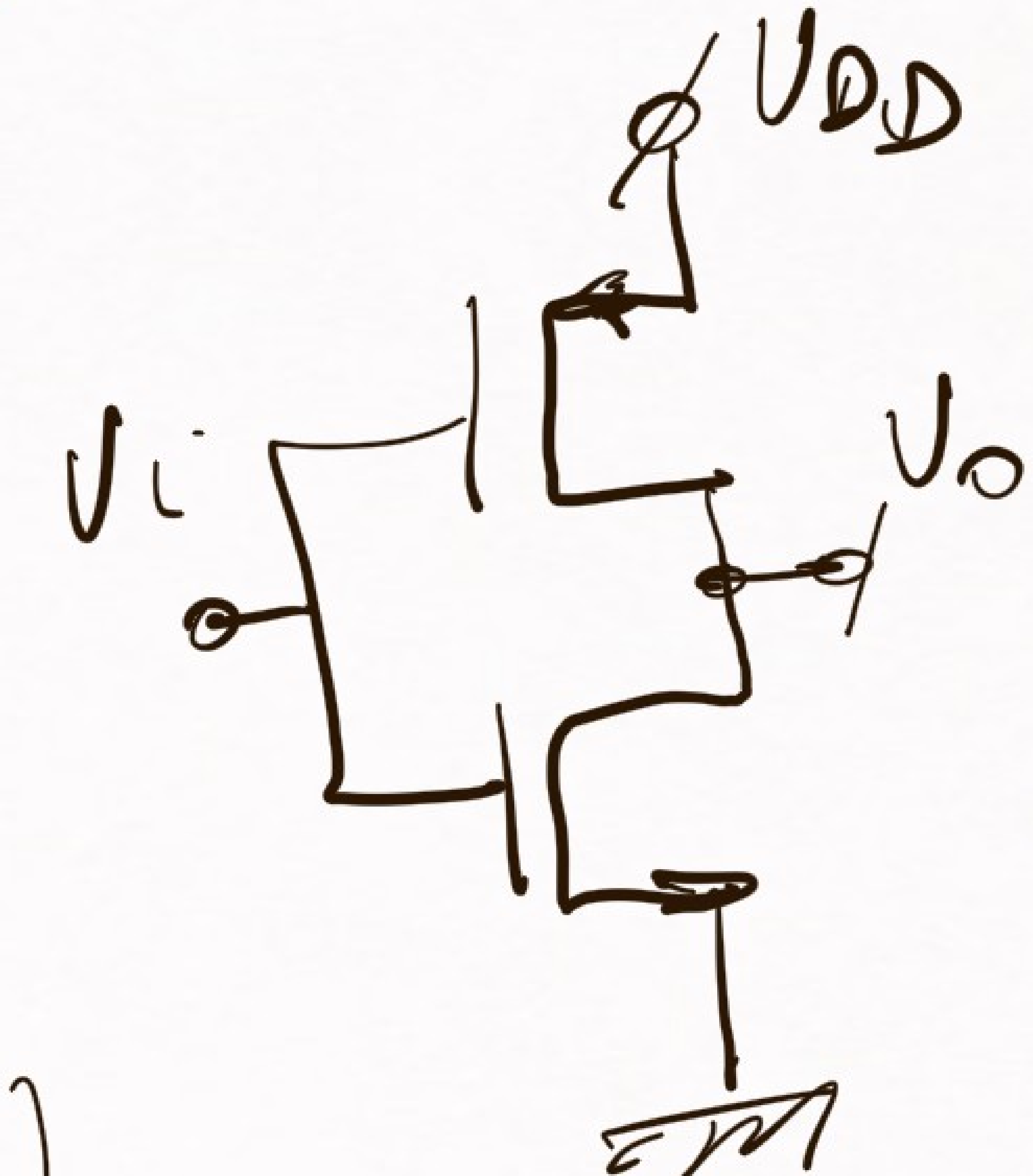
$\Rightarrow$ característica estática es simétrica y $V_C = \frac{V_{DD}}{2}$

Determinación de VIH

⇒ Zona en que PSAT, NLIN

$V_{toN} = |V_{toP}| = V_{to}$, $\gamma_N = \gamma_P = 0$, $\beta_N = \beta_P = \beta$

→ Caso simplificado



⇒ V_{IH} : V_i / $dV_o/dV_i = -1$

$V_o = f(V_i)$ ⇒ $I_{DN} = I_{DP}$

→ $I_{DN} = \beta\left((V_G - V_{to})(V_D - V_S) - \frac{1}{2}(V_D^2 - V_S^2)\right)$

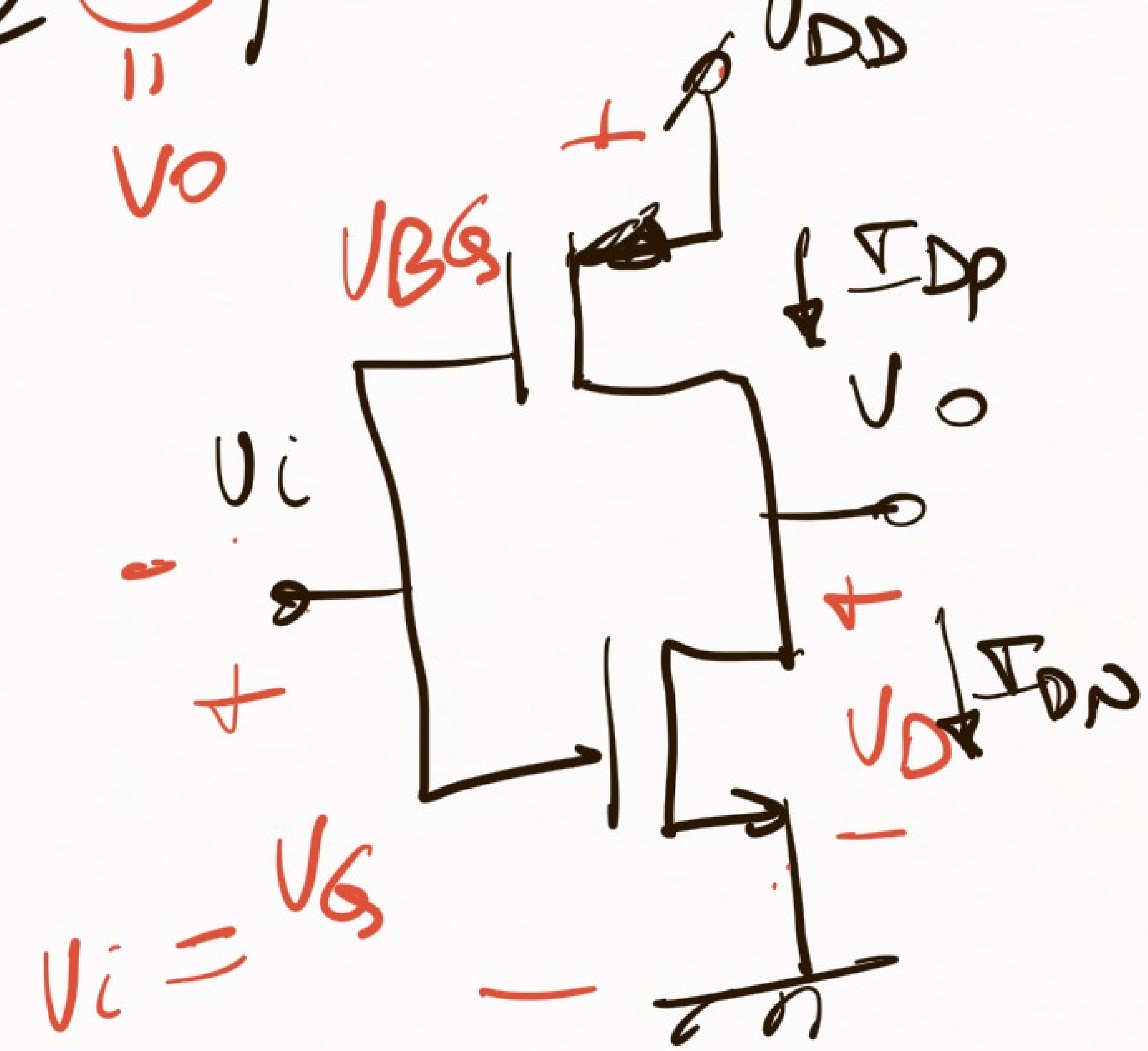
$I_{DP} = \frac{\beta}{2}(V_{BG} - V_{to})^2$ $(V_{BSP} = V_{SBN} = 0)$

$$I_{DN} = \beta\left((V_G - V_{to})V_D - \frac{1}{2}V_D^2\right)$$

$V_G = V_i$, $V_D = V_o$, $V_D = V_o$

$$I_{DP} = \frac{\beta}{2}\left(V_{BG} - V_{to}\right)^2$$

$V_{BG} = V_{DD} - V_i$



$\Rightarrow I_{DN} = I_{DP}$

$\hookrightarrow V_o = f(V_i)$

y luego $\frac{dV_o}{dV_i} = -1 \Rightarrow V_i = V_{IH}$

$$\beta\left((V_i - V_{to})V_D - \frac{1}{2}V_o^2\right) = \frac{\beta}{2}\left(V_{DD} - V_i - V_{to}\right)^2 \quad (I)$$

$\Rightarrow$ derivo respecto a V_i a ambos lados de la igualdad

$$(V_i - V_{to})V_o - \frac{1}{2}V_o^2 = \frac{1}{2}(V_{DD} - V_i - V_{to})^2 \quad (I)$$

derivando resp. a V_i

$$(V_i - V_{to})\frac{dV_o}{dV_i} + V_o - V_o \cdot \frac{dV_o}{dV_i} = -(V_{DD} - V_i - V_{to}) \quad (II)$$

($\frac{dV_o}{dV_i} = -1$, $V_i = V_{IH}$)

$V_i, V_o \,/\, \frac{dV_o}{dV_i} = -1$

$$V_o\Big|_{V_{IH}} = V_{IH} - V_{DD}/2 \Rightarrow \text{sustituyendo en } (I)$$

$$\Rightarrow \boxed{V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)}$$

Analogamente (o por simetría)

$$\Rightarrow \boxed{V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)}$$

$$\Rightarrow NM_H = \underbrace{V_{OH}}_{= V_{DD}} - \underbrace{V_{IH}} = \frac{1}{8}(3V_{DD} + 2V_t)$$

$$\Rightarrow NM_L = V_{IL} - \underbrace{V_{OL}}_{= 0} = V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

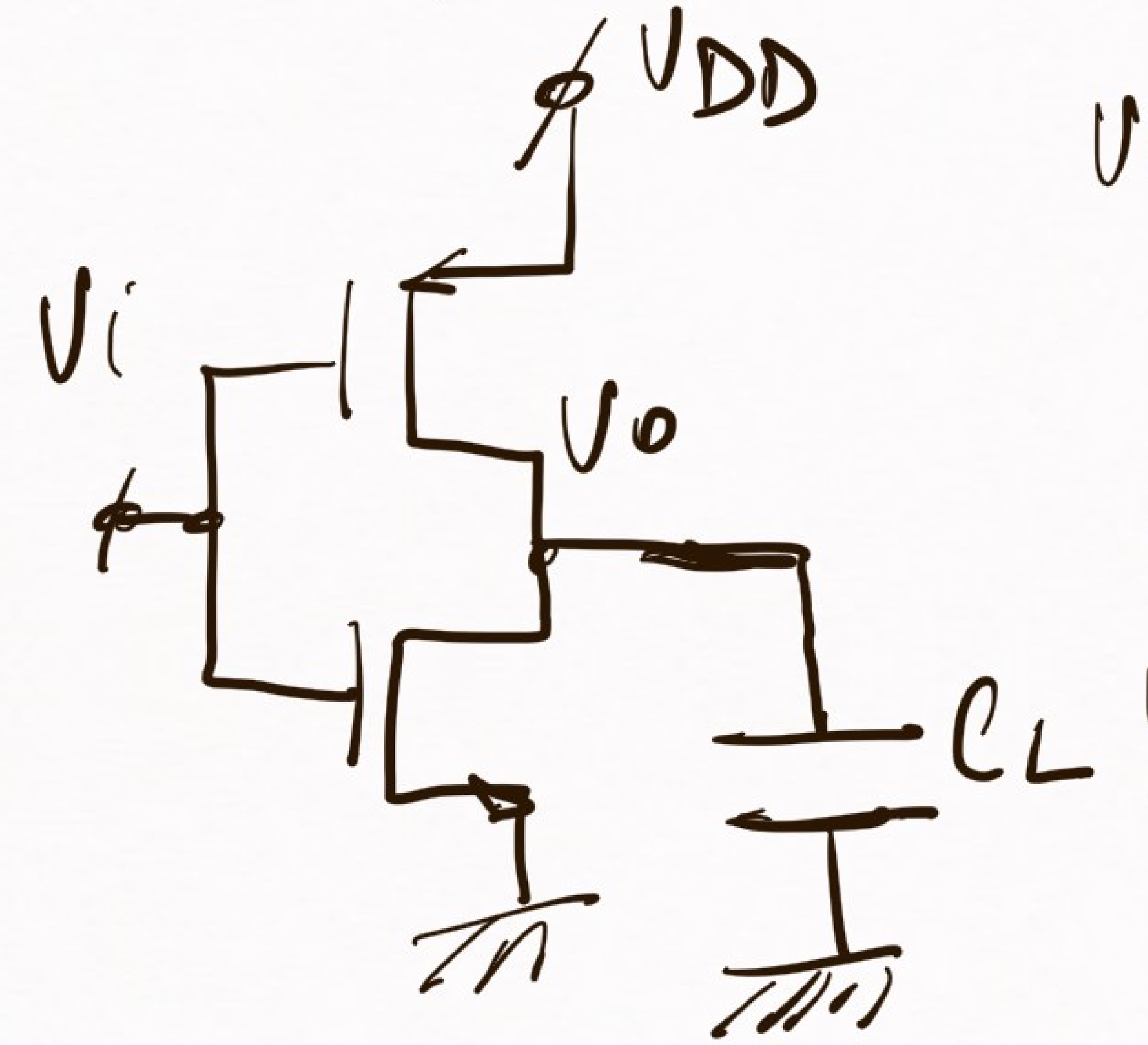
Ej: $V_{DD} = 5V$, $V_{t0} = 1V$

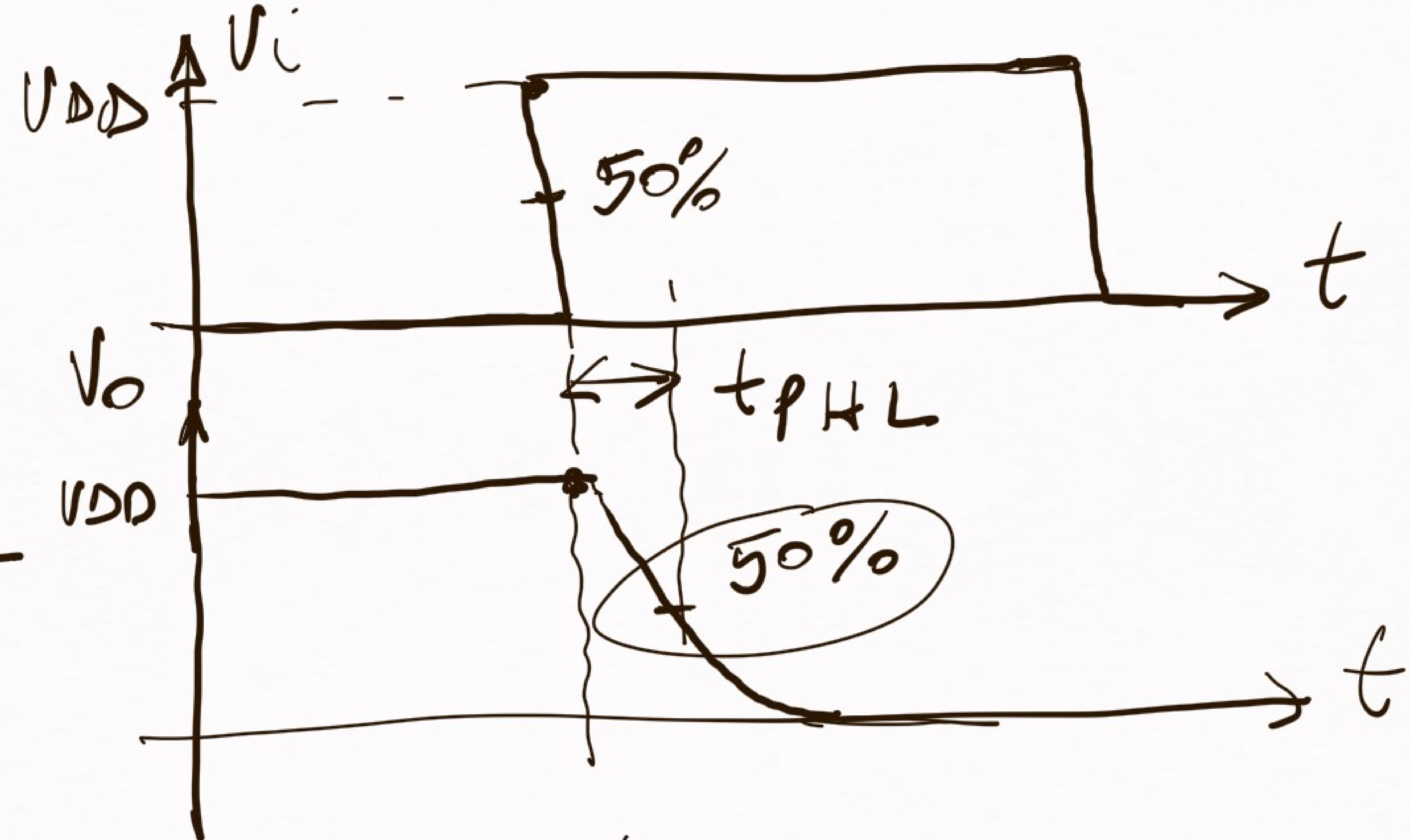
$$\Rightarrow V_{IL} = \underbrace{2{,}1V}_{= NM_L = NM_H}, \quad V_{IH} = 2.9V$$

usual:

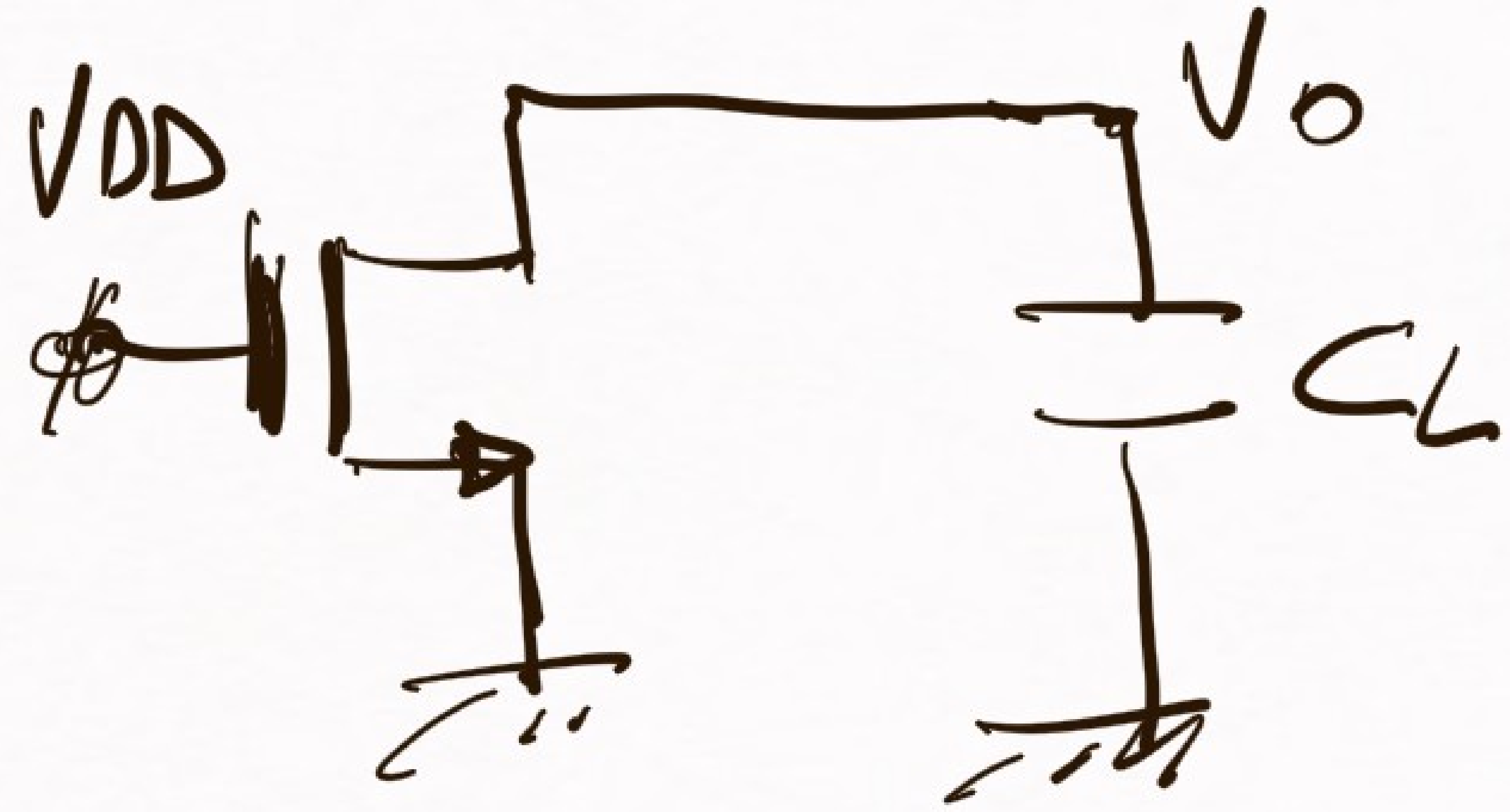
$NM_L = NM_H \simeq \frac{1}{3} V_{DD}$

Velocidad, tiempo de propagación:

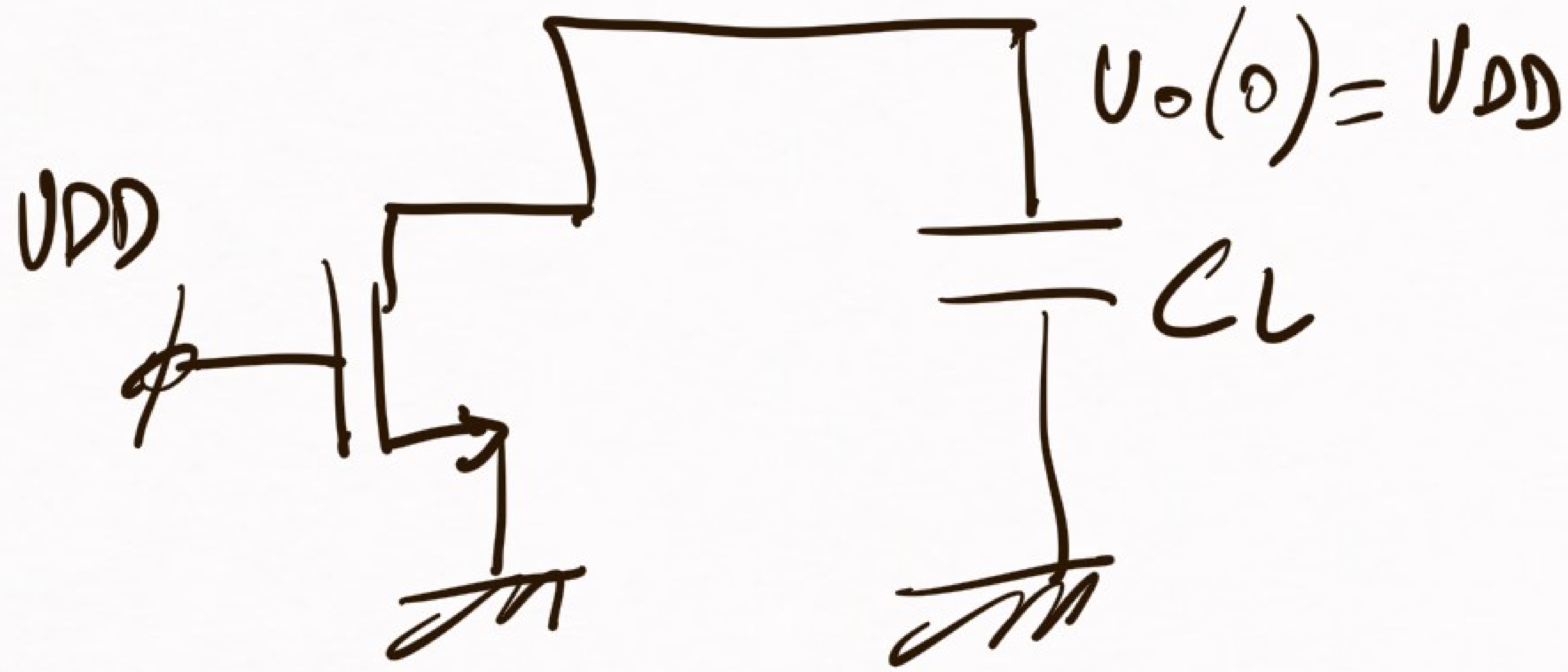


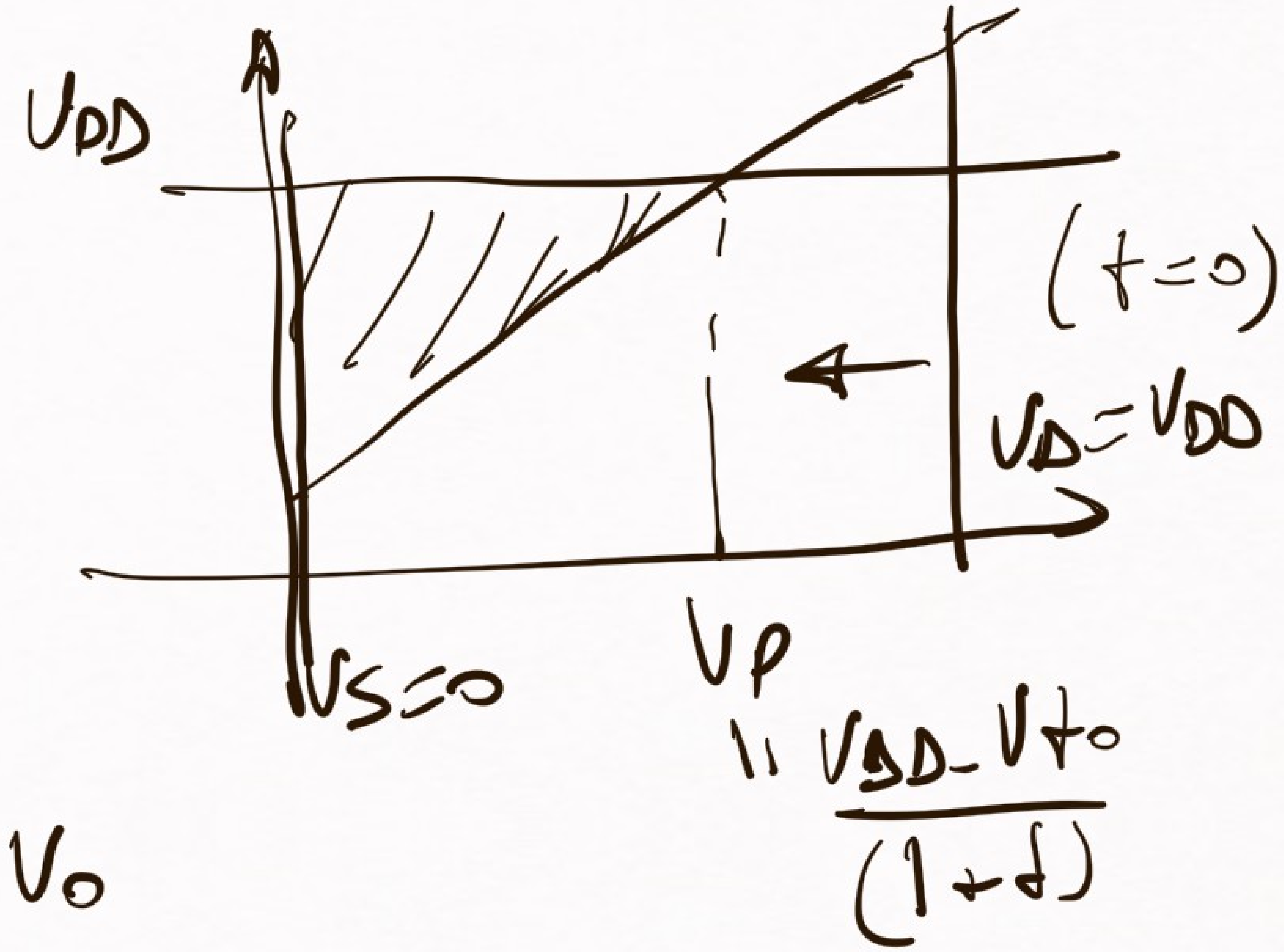


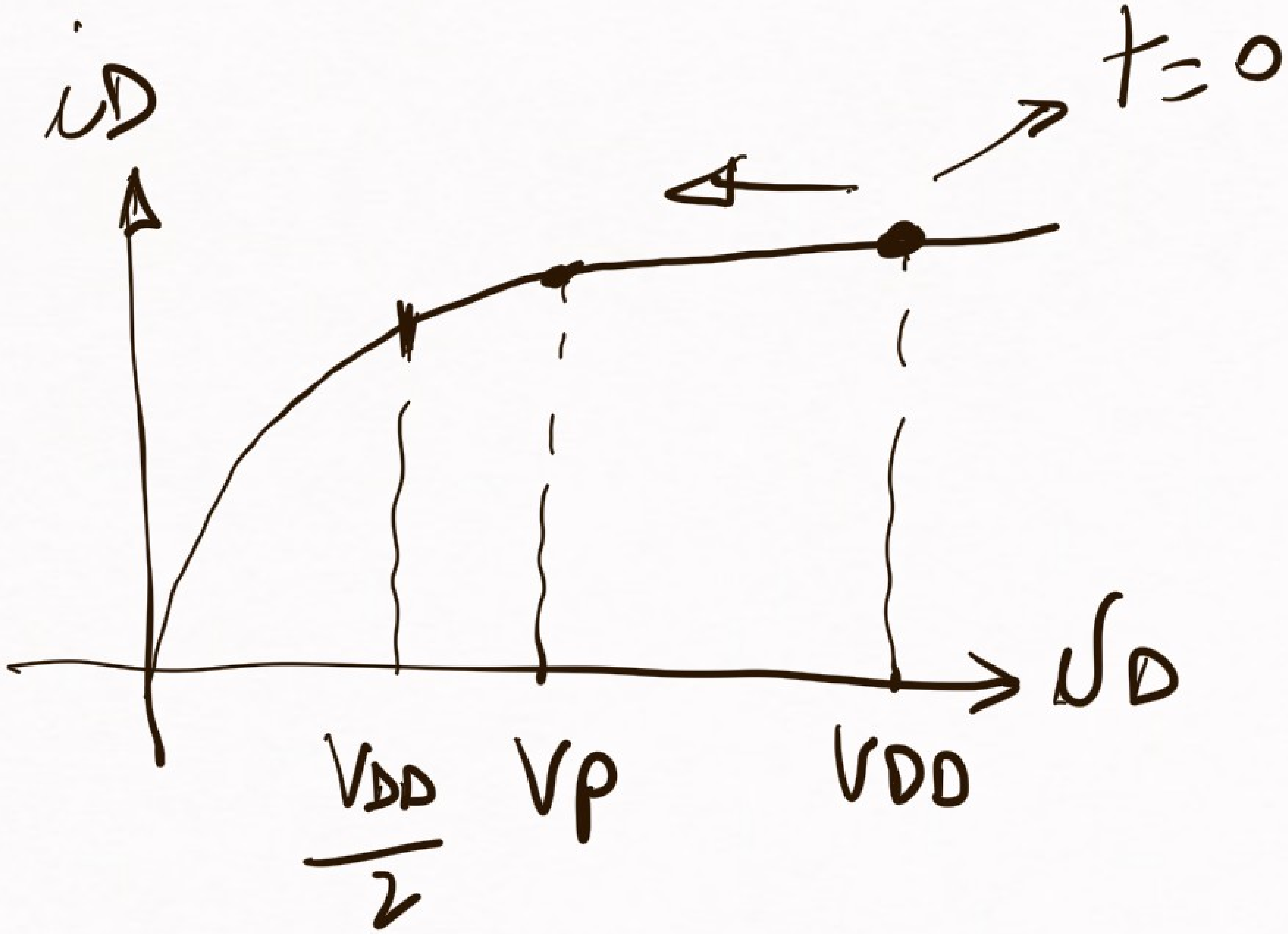
$V_i: 0 \rightarrow V_{DD} \Rightarrow$ P OFF, N conduce.

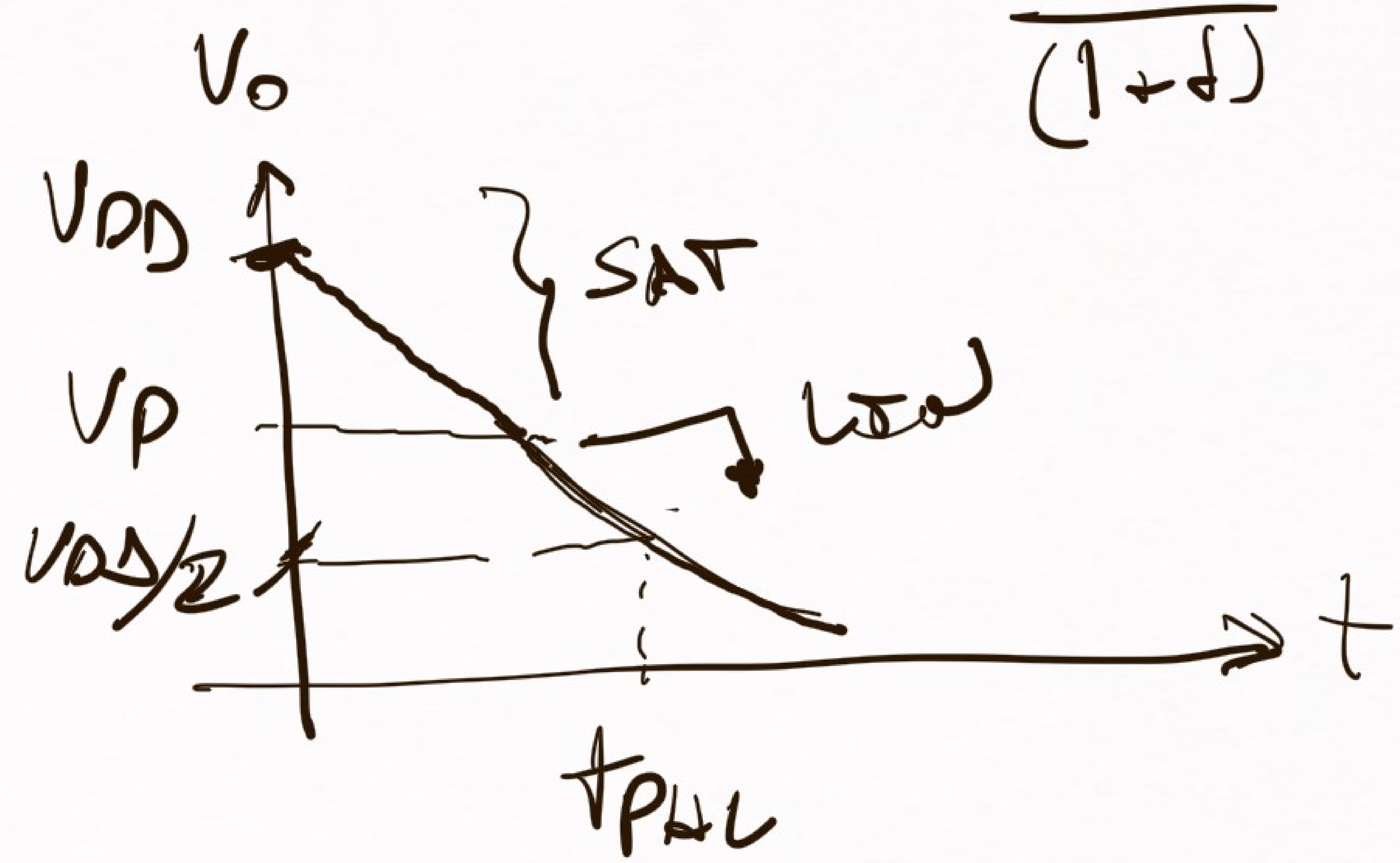


$V_o(t=0) = V_{DD}$


VDD
Vo(0) = VDD
CL


VDD
(t=0)
VD = VDD
VS=0
VP
= VDD-Vto / (1+δ)


iD
t=0
VD
VDD/2
VP
VDD


Vo
VDD
SAT
VP
VDD/2
t
tPHL

$\Rightarrow t_{pHL} = f\left(\mu \cdot C_{ox} \frac{W}{L}, C_L, V_{DD}, V_{to}, f\right)$

Si $V_{to} = \frac{1}{5} V_{DD}$ (relación aproximada de muchas tecnologías)

V_{DD}	V_{to}
5	1
3.3	0.6 ... 0.7
1.2	0.35

$$t_{pHL} = \frac{1.6\, C_L}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n \cdot V_{DD}}$$

$t_{pHL} \propto C_L$ | $t_{pHL} \propto \frac{1}{V_{DD}}$ | compromiso

$t_{pHL} \propto \frac{1}{\left(\frac{W}{L}\right)_n}$: $\left(\frac{W}{L}\right) \uparrow \Rightarrow (I_{DN}) \uparrow \Rightarrow t_{pHL} \downarrow$

pero carga de las etapas anteriores $\uparrow$

Consumo de energía

∃ 3 consumos:

1) Consumo estático
2) Consumo dinámico (debido a C_L)
3) Consumo por camino directo $V_{DD}-V_{SS}$ (durante la conmutación).

1) Consumo estático.

↳ idealmente es nulo

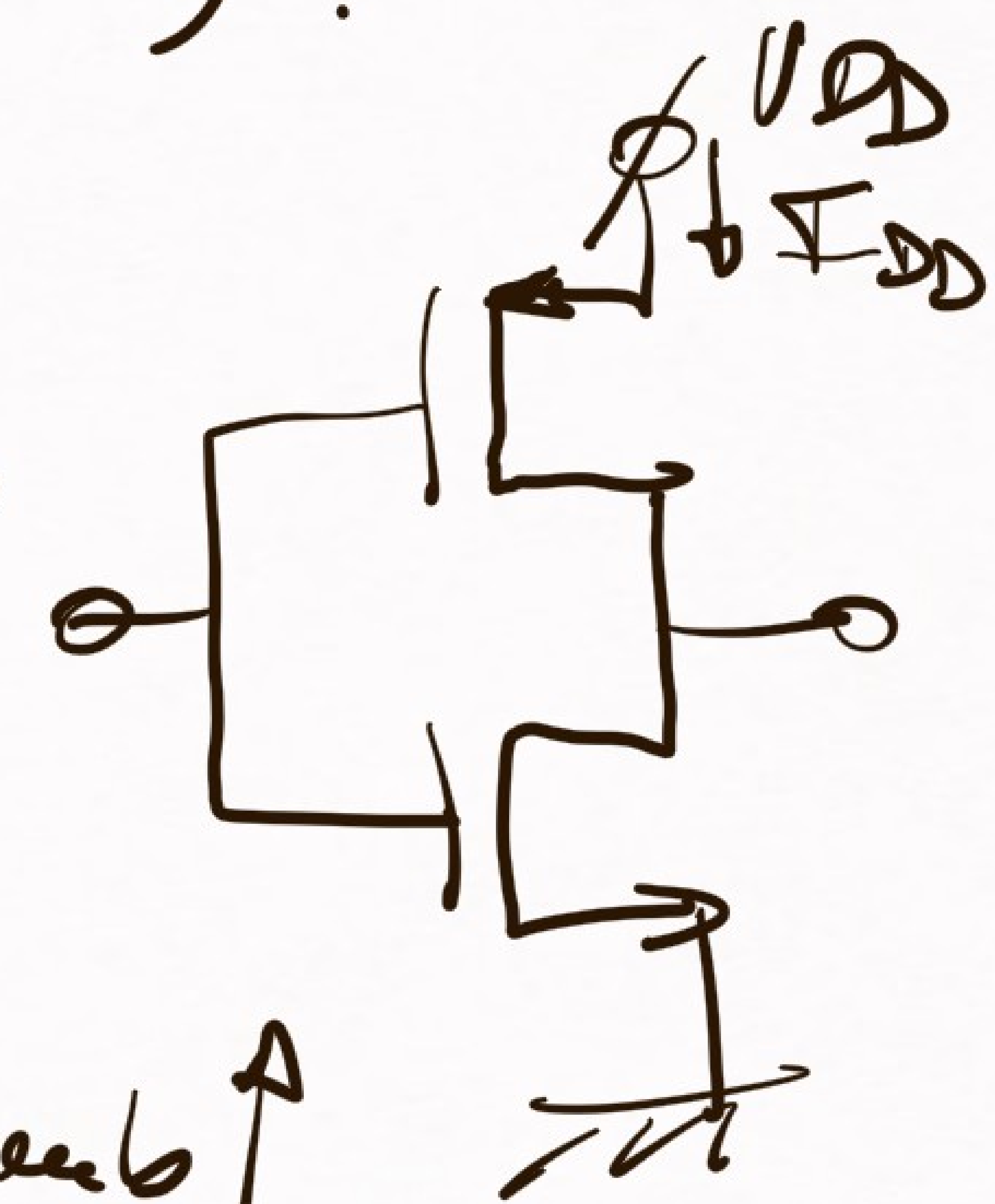
pero ∃ corriente subumbral

$V_{DD}\downarrow$ ⇒ hay que bajar V_{T0}

⇒ al bajar V_{T0} ⇒ corriente subumb↑

VDD

0



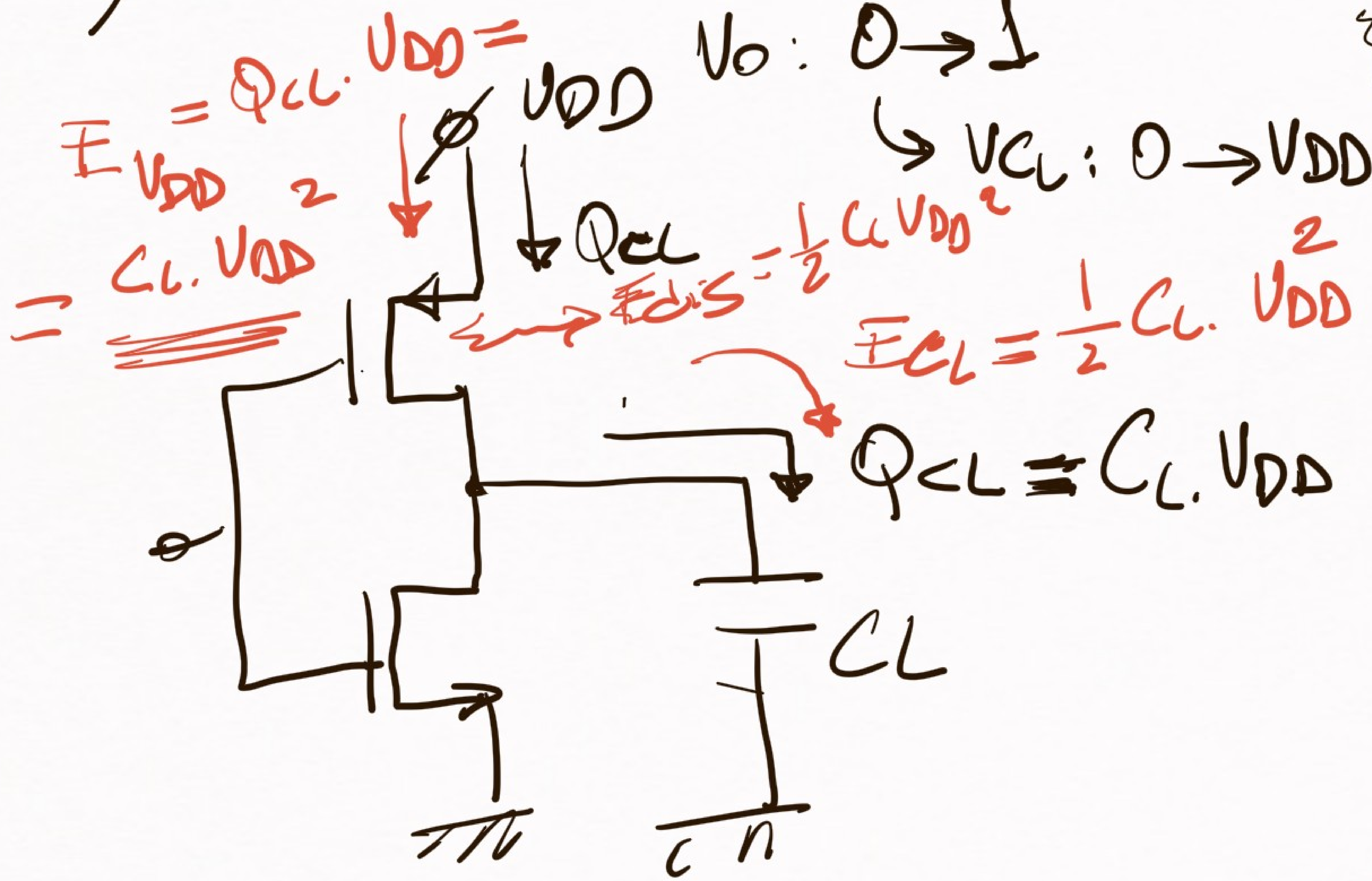
⇒ consumo estático es más importante en tecnologías orentados

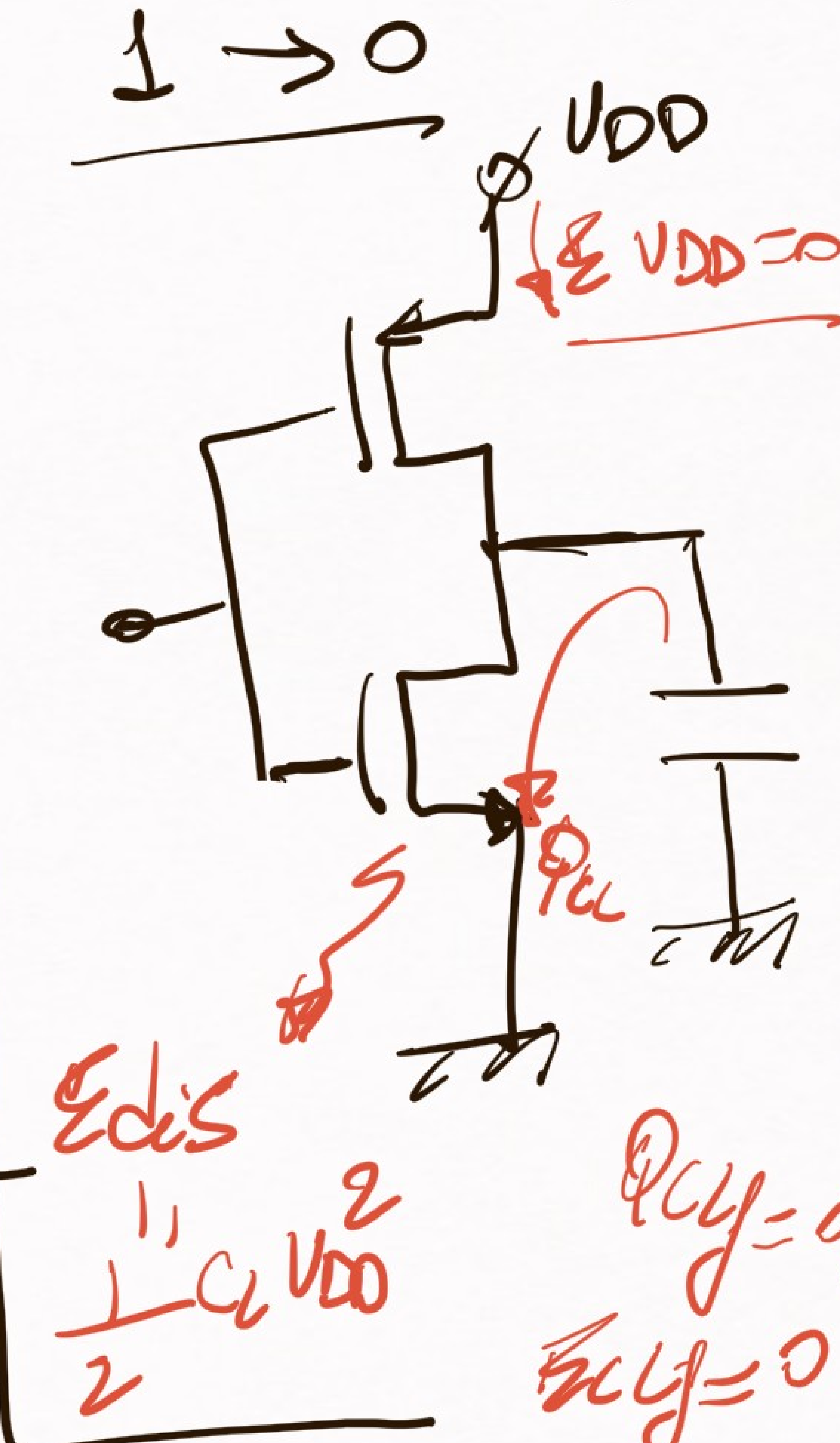
Ej: procesador i7, tecnología 45 nm (desktop), 2.93 GHz, 731 M transistores

$V_{DD} = 1.2V$ ⇒ $P_{DD} = 130\,W$ → $P_{estática} = 10W$

⇒ $I_{DD} \cong 110\,A$!!

2) Consumo dinámico (asociado a CL)





En un ciclo de periodo T
(en el que cargo y descargo el nodo)

$\Rightarrow E_{VDD} = C_L VDD^2$, $P_{VDD} = \frac{E_{VDD}}{T} = f \cdot C_L VDD^2$ Cons dinámico.

$$P_{VDD} = f \cdot C_L \cdot V_{DD}^2$$

$\Rightarrow P_{VDD} \propto f$

$\propto C_L$

$\propto V_{DD}^2$!!

$V_{DD} \downarrow \Rightarrow P_{VDD} \downarrow\downarrow$

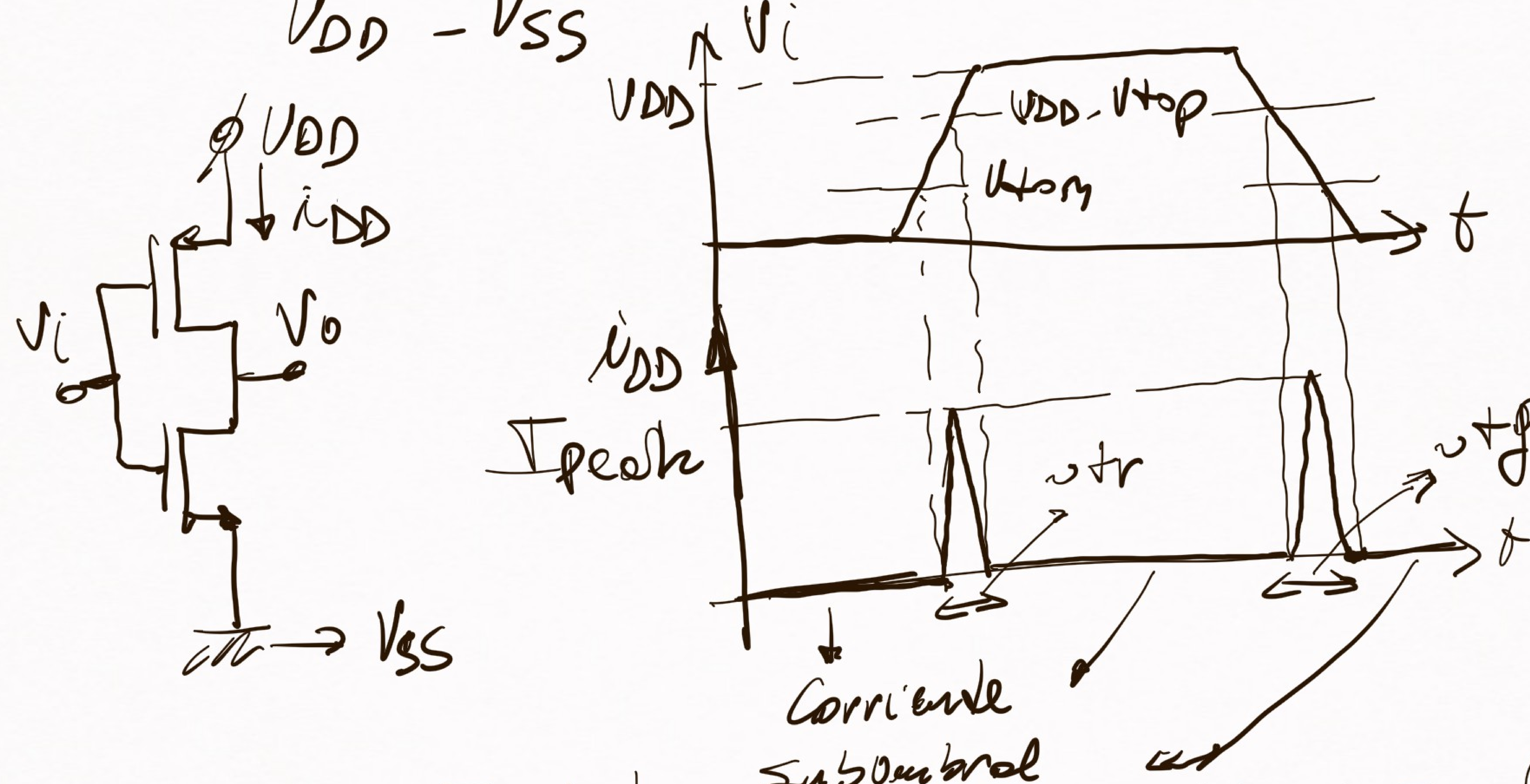
pero si $V_{DD} \downarrow$

$\Rightarrow t_{PHL} \uparrow$

$\Rightarrow$ DVFS: "Dynamic Voltage-Frequency scaling"

3) Consumo por camino directo

$V_{DD} - V_{SS}$

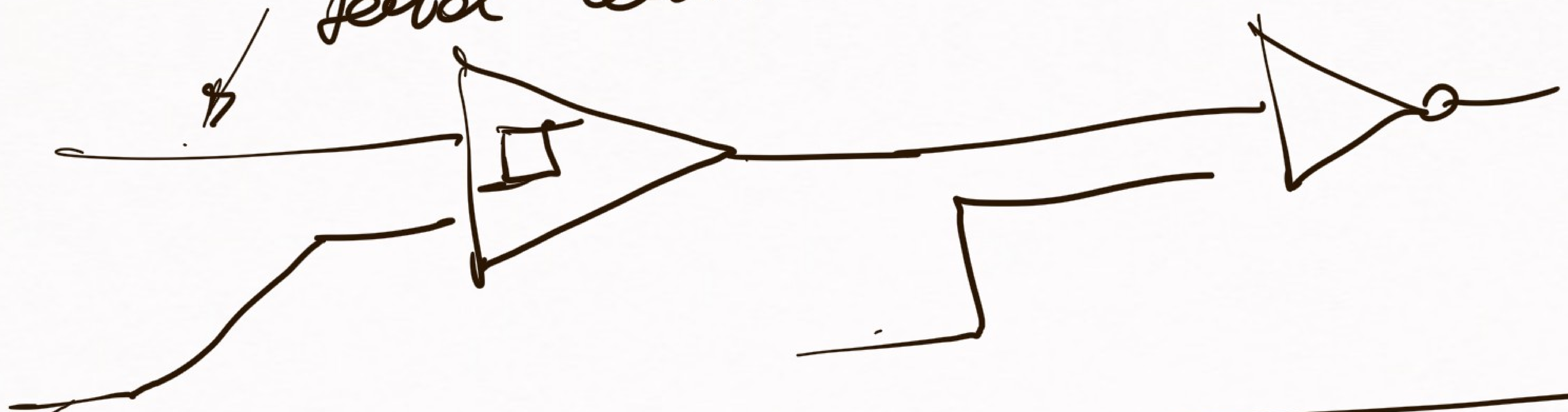


$$E_{VDD} = V_{DD} \cdot \frac{I_{peak} \cdot t_r}{2} + V_{DD} \frac{I_{peak} \cdot t_f}{2} = V_{DD} \cdot I_{peak} \frac{(t_r + t_f)}{2}$$

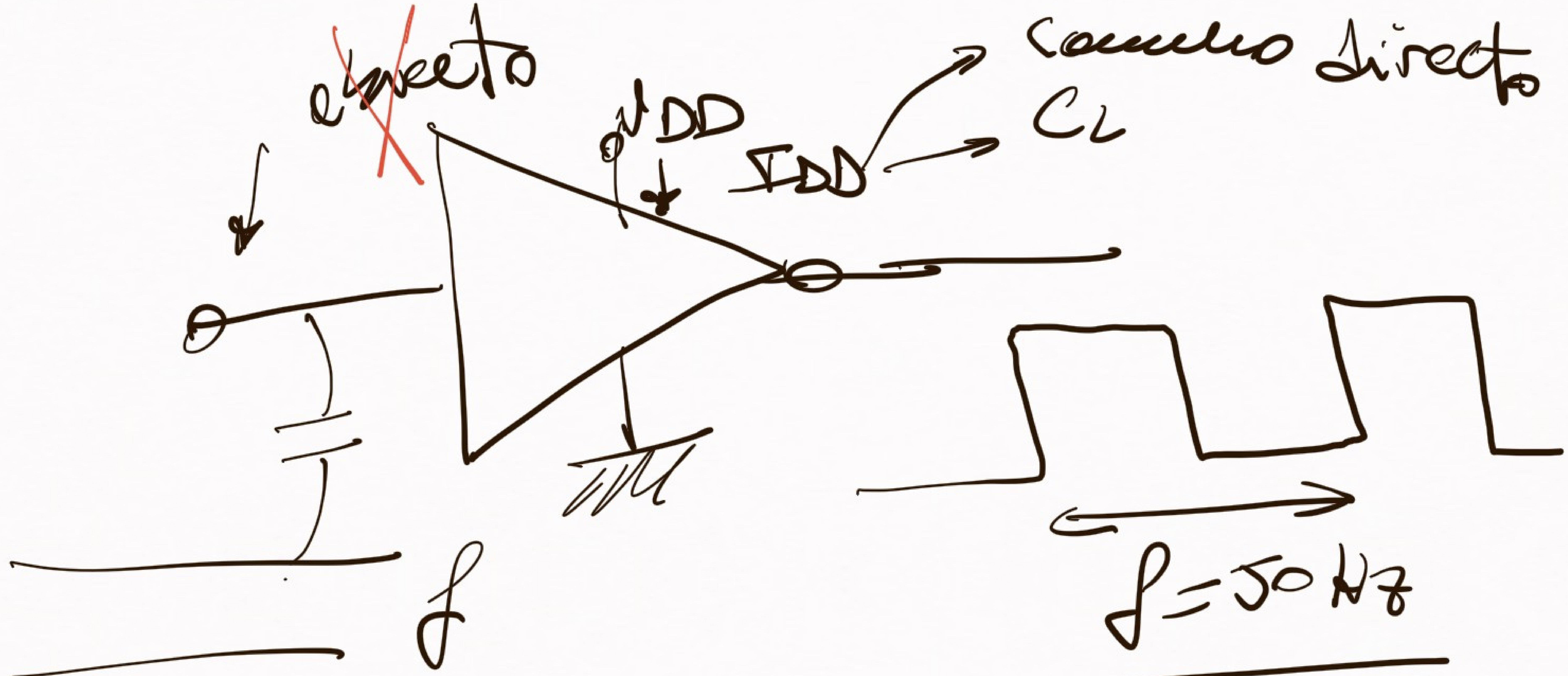
$E_{VDD} \propto \frac{(t_r + t_f)}{2}$ || $E_{VDD} \sim 20\% \, E_{dyn}$

⇒ cuidado con t_r o t_f muy lentos

señal lenta



Tanto para Idir cc, como para camino directo: cuidado con no tener entradas abiertas



(o otra frecuencia de una señal cercana)

inversor no usado