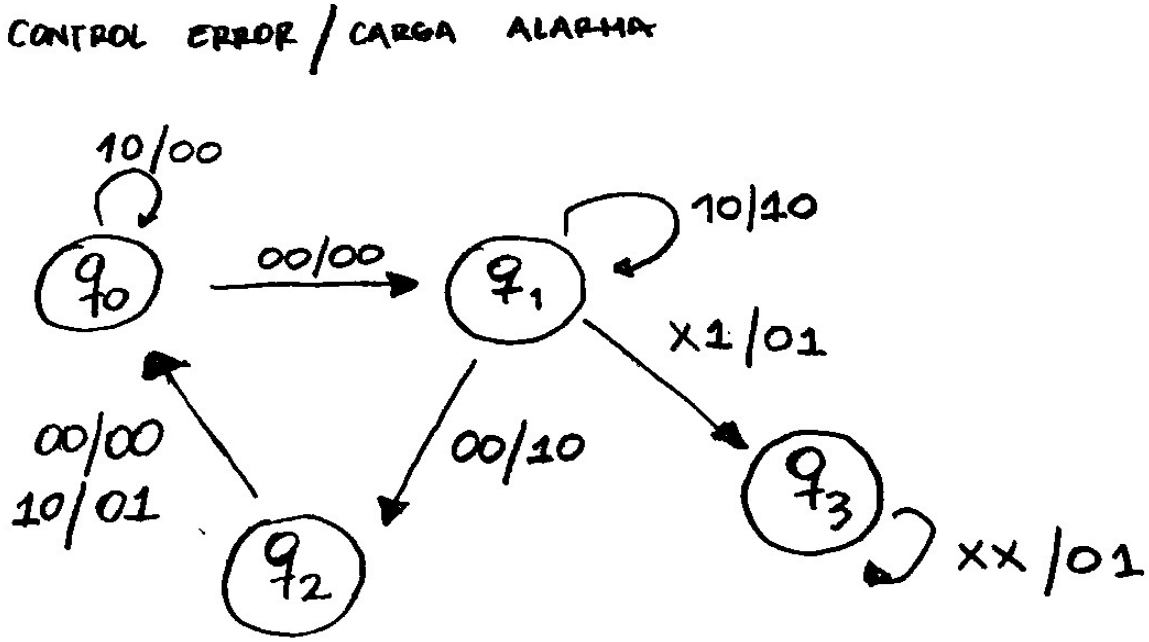
DISEÑO LOGICO
Prueba Escrita, 2018

Modor Reloj



RTL

```
MODULE: RTL_PAR2018
INPUTS: DAT, NUE, MED[8]
MEMORY: T_SAMPLE[8], ADD_MEM[10],  AUX[8], CONT_T[8]
OUTPUTS: WE, ADD[10], DATA[8],SEL[2], SH

   1. T_SAMPLE[7..0] ← 1111 1111 B
      ADD_M[9..0] ← 00 0000 0000 B
      AUX[7..0] ← 1111 1111 B
      CONT_T[8] ← 1111 1111 B


   2. SH=FIN_TIEMPO
      AUX[7..0]*NUE ← DAT,AUX[7..1]
      T_SAMPLE*!NUE ← AUX[7..0]
      CONT_T[8] ← INC (CONT_T).!FIN_TIEMPO
      ADD_MEM[10]*FIN_TIEMPO ← INC (ADD_MEM[10])            ; CONT CIRCULAR
      WE=FIN_TIEMPO
      → 2

END SEQUENCE
CONTROL RESET (1)

      FIN_TIEMPO =  MENORIGUAL (T_SAMPLE[7..0], CONT_T[7..0])
      DATA[8] = MED[8]
      ADD[10] =ADD_MEM[10]

END
```