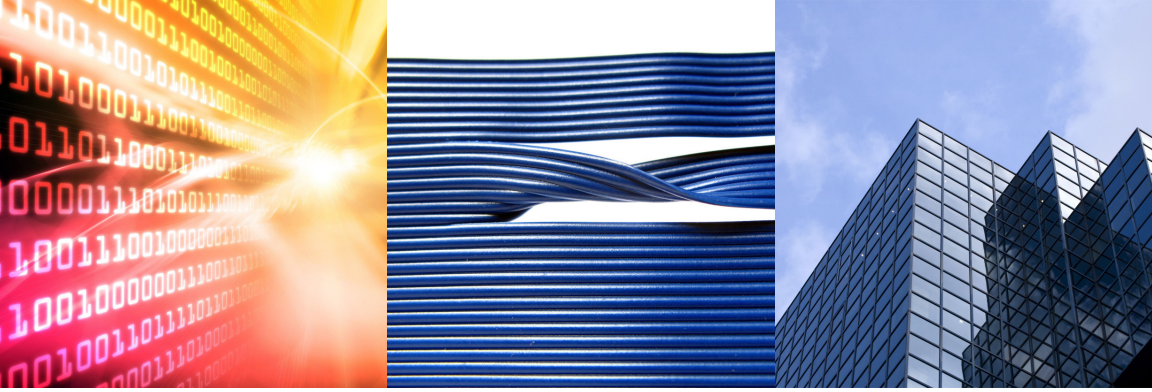

# Jitter & Wander measurements


**The AT-2048 is the ultimate tester designed specifically for field engineers that are installing, commissioning and trouble-shooting E1, Datacom circuits.** The AT-2048 has been designed in 2010 and manufactured in 2011 by ALBEDO Telecom in Barcelona. It is a brand new platform incorporating the latest available electronics and features such as Jitter and Wander. Consequently you will enjoy top performance, high accuracy and, of course, a very competitive price.

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# 1 Network Synchronization

*Synchronization* is the set of techniques that enable the frequency and phase of the equipment clocks in a network to remain constrained within the specified limits (see Figure 1.1). The first digital networks were asynchronous, and therefore did not call for properly working external synchronization. It was the arrival of SDH and SONET networks that started to make synchronization essential to maintain transmission quality and efficiency of supported teleservices.

*Bad synchronization* causes regeneration errors and *slips*. The effects of these impairments vary in different systems and services. Some isochronous[1] services, like telephony, tolerate a deficient synchronization rather well, and small or no effects can be observed by the end-user. Others, like digital TV transmission, fax, or compressed voice and video services, are more sensitive to synchronization problems. In HDLC, FRL, or TCP/IP types of data services, slips that occur force us to retransmit packets, and this makes transmission less efficient.

## 1.1 Architecture of Synchronization Networks

Synchronization networks can have hierarchical or nonhierarchical architectures. Networks that use *hierarchical synchronization* have a tree architecture. In such networks a master clock is distributed, making the rest of the clocks slaves of its signal. A network with all the equipment clocks locked to a single master timing reference is called *synchronous*. The following elements can be found in the hierarchical synchronization network:

1. A *master clock*, which is usually an atomic cesium oscillator with global positioning system (GPS) and/or Loran-C[2] reference. It occupies the top of the pyramid, from which many synchronization levels spread out (see Table 1.1).
2. High-quality *slave clocks*, to receive the master clock signal and, once it is filtered and regenerated, distribute it to all the NEs of their node.
3. *NE clocks,* which finish the branches of the tree by taking up the lowest levels

1. Isochronous (from the Greek "equal" and "time") pertains to processes that require timing coordination to be successful, such as voice and digital video transmission.
2. Loran-C is an electronic position fixing system using pulsed signals at 100 kHz.

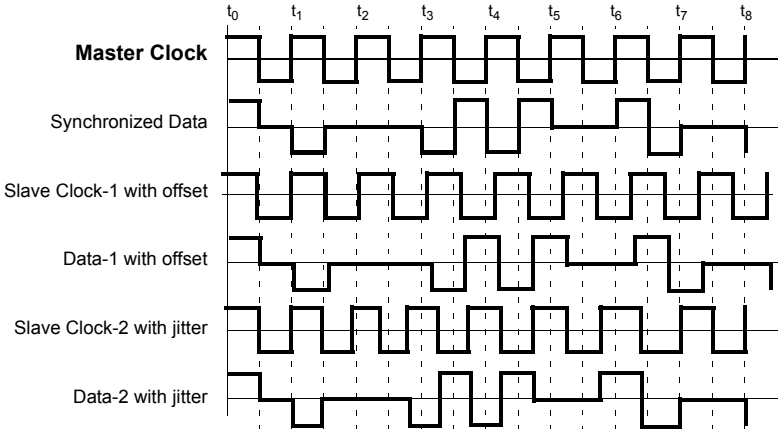



**Figure 1.1** A master clock that marks the significant instances for data transmission. Clocks 1 and 2 are badly synchronized, and the data transmitted with these references is also affected by the same phase error.

of the synchronization chain. Basically, they are the ones using the clock, although they may also send it to other NEs.

4. *Links*, responsible for transporting the clock signal. They may belong to the synchronization network only, or, alternatively, form a part of a transport network, in which case the clock signal is extracted from data flow (see Figure 1.3).

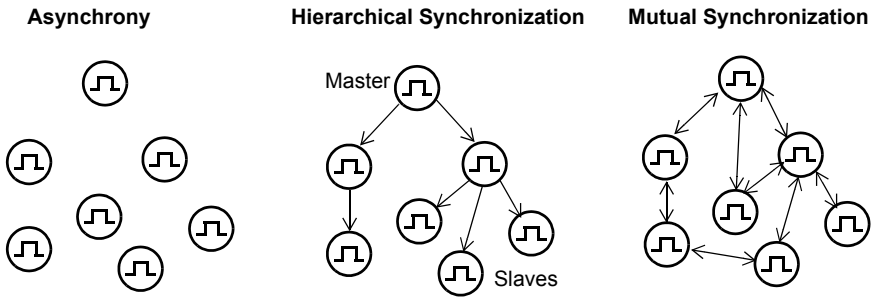



**Figure 1.2** Classes of synchronization architectures.

The pure hierarchical synchronization architecture can be modified in several ways to improve network operation. *Mutual synchronization* is based on cooperation between nodes to choose the best possible clock. There can be several master clocks, or even a cooperative synchronization network, besides a synchronization protocol

between nodes (see Figure 1.2). Bringing these networks into services is more complex, although the final outcome is very solid.

Those networks where different nodes can use a clock of their own, and correct operation of the whole depends on the quality of each individual clock, are called *asynchronous* (see Figure 1.2). Asynchronous operation can only be used if the quality of the node clocks is good enough, or if the transmission rate is reduced. The operation of a network (that may be asynchronous in the sense described above or not) is classified as *plesiochronous* if the equipment clocks are constrained within margins narrow enough to allow simple bit stuffing (see Figure 1.2).

General requirements for today's SONET and SDH networks are that any NE must have at least two reference clocks, of higher or similar quality than the clock itself. All the NEs must be able to generate their own synchronization signal in case they lose their external reference. If such is the case, it is said that the NE is in *holdover*.

A synchronization signal must be filtered and regenerated by all the nodes that receive it, since it degrades when it passes through the transmission path, as we will see later.

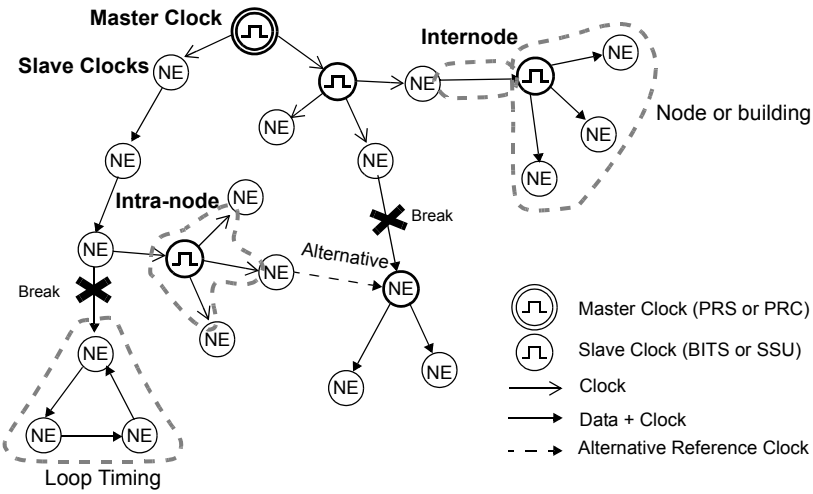



**Figure 1.3** Synchronization network topology for SONET and SDH. This figure does not show links that are for transport only.

**Table 1.1**
Clock performance.

| *Type* | *Performance* |
|---|---|
| Cesium | From $10^{-11}$ up to $10^{-13}$ |
| Hydrogen | From $10^{-11}$ up to $10^{-13}$ |
| GPS | Usually $10^{-12}$ |
| Rubidium | From $10^{-9}$ up to $10^{-10}$ |
| Crystal | From $10^{-5}$ up to $10^{-9}$ |

### 1.1.1 Synchronization Network Topologies

The synchronization and transport networks are partially mixed, since some NEs both transmit data and distribute clock signals to other NEs.

The most common topologies are:

1. *Tree*: This is a basic topology that relies on a master clock whose reference is distributed to the rest of the slave clocks. It has two weak points: it depends on only one clock, and the signals gradually degrade (see Figure 1.5).
2. *Ring*: Basically, this is a tree topology that uses SDH/SONET ring configurations to propagate the synchronization signal. The ring topology offers a way to make a tree secure, but care must be taken to avoid the formation of synchronizing loops.
3. *Distributed*: Nodes make widespread use of many primary clocks. The complete synchronization network is formed by two or more islands; each of them depending on a different primary clock. To be rigorous, such a network is asynchronous, but thanks to the high accuracy of the clocks commonly used as a primary clock, the network operates in a very similar way to a completely synchronous network.
4. *Meshed*: In this topology, nodes form interconnections between each other, in order to have redundancy in case of failure. However, synchronization loops occur easily and should be avoided.

Synchronization networks do not usually have only one topology, but rather a combination of all of them. Duplication and security involving more than one master clock, and the existence of some kind of synchronization management protocol, are important features of modern networks. The aim is to minimize the problems associated with signal transport, and to avoid depending on only one clock in case of failure. As a result, we get an extremely precise, redundant, and solid synchronization network.

## 1.2 INTERCONNECTION OF NODES

There are two basic ways to distribute synchronization across the whole network:

- *Intranode*, which is a high-quality slave clock known as either *synchronization supply unit* (SSU) or *building integrated timing supply* (BITS). These are responsible for distributing synchronization to NEs situated inside the node (see Figure 1.3).
- *Internode*, where the synchronization signal is sent to another node by a link specifically dedicated to this purpose, or by an STM-*n*/OC-*m* signal (see Figure 1.3).

### 1.2.1 Synchronization Signals

There are several signals suitable for transporting synchronization:

- Analog, of 1,544 and 2,048 kHz;
- Digital, of 1,544 and 2,048 Kbps;
- STM-*n*/OC-*m* line codes, from which one of the above-mentioned signals is derived, by means of a specialized circuit.

In any case, it is extremely important for the clock signal to be continuous. In other words, its mean frequency should never be less than its fundamental frequency (see Figure 1.4).

#### 1.2.1.1 Clock transfer across T-carrier/PDH networks

These types of networks are very suitable for transmitting synchronization signals, as the multiplexing and demultiplexing processes are bit oriented (not byte oriented like SONET and SDH), and justification is performed by removing or adding single bits. As a result, T1 and E1 signals are transmitted almost without being affected by

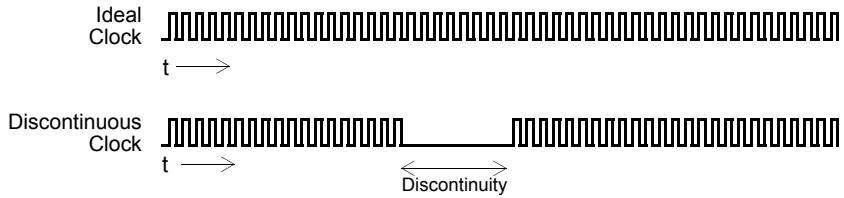



**Figure 1.4** A pure clock signal is continuous, as, for example, the one provided by an atomic clock. A discontinuous signal in its turn could be a signal delivered by a T1 circuit transported in SONET.

justification jitter, mapping or overhead-originated discontinuities. This characteristic is known as *timing transparency*.

There is only one thing to be careful with, and that is to not let T1 and E1 signals cross any part of SONET or SDH, as they would be affected by phase fluctuation due to mapping processes, excessive overhead, and pointer movements. In short, T1 or E1 would no longer be suitable for synchronization.

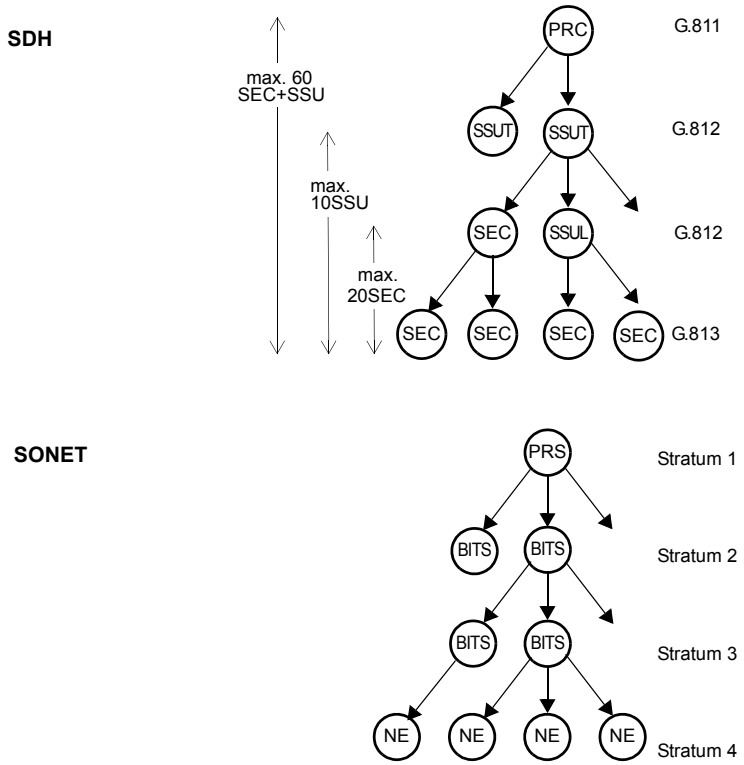



**Figure 1.5** Synchronization network model for SONET and SDH. Stratum 3 has the minimum quality required for synchronizing an NE. In SDH the figures indicate the maximum number of clocks that can be chained together by one signal.

### 1.2.1.2 Clock transfer across SDH/SONET links

To transport a clock reference across SDH/SONET, a line signal is to be used instead of the tributaries transported, as explained before. The clock derived from an STM-*n*/OC-*m* interface is only affected by wander due to temperature and environ-

mental reasons. However, care must be taken with the number of NEs to be chained together, as all the NEs regenerate the STM-*n*/OC-*m* signal with their own clock and, even if they were well synchronized, they would still cause small, accumulative phase errors.

The employment of STM-*n*/OC-*m* signals has the advantage of using the S1 byte to enable *synchronization status messages* (SSMs) to indicate the performance of the clock with which the signal was generated (see Figure 1.6). These messages are essential in reconstructing the synchronization network automatically in case of failure. They enable the clocks to choose the best possible reference, and, if none is available that offers the performance required, they enter the holdover state.

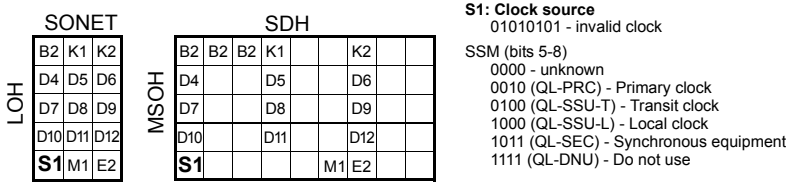



**Figure 1.6** The S1 byte is used to send SSMs in SDH and SONET.

### 1.2.2 Holdover Mode

It is said that a slave clock enters holdover mode when it decides to use its own generator, because it does not have any reference available, or the ones available do not offer the performance required. In this case, the equipment remembers the phase and the frequency of the previous valid reference, and reproduces it as well as possible. Under these circumstances, it puts an SSM=QL-SEC message into the S1 byte of STM-*n*/OC-*m* frames, and, if it was generating synchronization signals at 1.5 or 2 MHz, it stops doing so.

### 1.2.3 Global Positioning System

The *global positioning system* (GPS) is a constellation of 24 satellites that belongs to the U.S. Department of Defense. The GPS receivers can calculate, with extreme precision, their terrestrial position and the universal time from where they extract the synchronization signal. The GPS meets the performance required from a primary clock (see Table 1.1). However, the GPS system might get interfered with intentionally, and the U.S. Department of Defense reserves the right to deliberately degrade its performance for tactical reasons.

## 1.3 DISTURBANCES IN SYNCHRONIZATION SIGNALS

Since synchronization signals are distributed, degradation in the form of jitter and wander accumulate. At the same time they are affected by different phenomena that cause phase errors, frequency offset, or even the complete loss of the reference clock. Care must be taken to avoid degradation in the form of slips and bit errors by filtering and an adequate synchronization distribution architecture (see Figure 1.7).

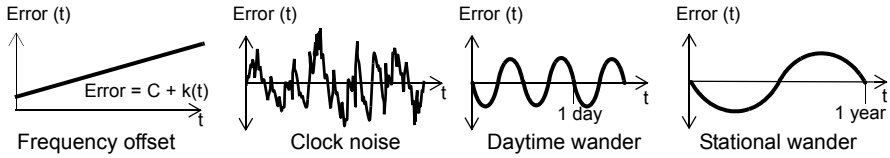



**Figure 1.7** Sources of phase variation.

### 1.3.1 Frequency Offset

Frequency offset is an undesired effect that occurs during the interconnection of networks or services whose clocks are not synchronized. There are several situations where frequency deviations occur (see Figure 1.8):

- On the boundary between two synchronized networks with different primary reference clocks;
- When tributaries are inserted into a network by nonsynchronized ADMs;
- When, in a synchronization network, a slave clock becomes disconnected from its master clock and enters holdover mode.

#### 1.3.1.1 Consequences of frequency offset in SDH/SONET

To compensate for their clock differences, SDH/SONET networks use pointer adjustments. Let us think of two multiplexers connected by STM-1 (see Figure 1.8), where ADM2 is perfectly synchronized, but ADM1 has an offset of 4.6 parts per million (ppm).

$$f_1 = 155{,}52Mbps$$

$$f_2 = 155{,}52Mbps + 4{,}6ppm = 155{,}52\left(1 + \frac{4{,}6}{10^6}\right)Mbps$$

ADM1 inserts a VC-4, but as ADM2 uses another clock, it should carry out pointer adjustments periodically, to compensate for the difference between the two clocks.

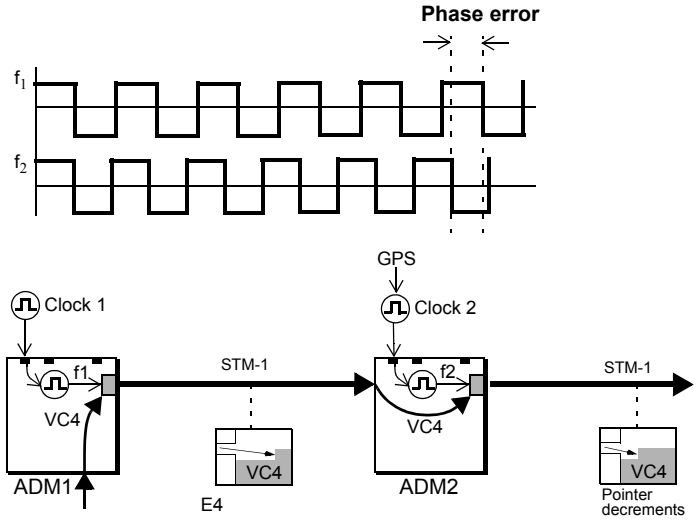



**Figure 1.8** Comparison of two reference signals that synchronize two SDH multiplexers. Periodical pointer adjustment occurs due to the frequency offset there is between the two signals.

That is to say, a 4.6 ppm frequency in STM-1 equals to:

$$f_3 = f_2 - f_1 = 155{,}52\left(1 + \frac{4{,}6}{10^6}\right) - 155{,}52 \qquad Mbps$$

$$f_3 = (155{,}52 \cdot 10^6)\left(1 + \frac{4{,}6}{10^6} - 1\right) = 155{,}52 \times 4{,}6 = 715{,}4 \qquad bps$$

However, this difference does not affect the whole STM-1 frame, but only the VC-4, and therefore we will only consider the difference of size between the two:

$$R = (VC4)_{bytes} / (STM1)_{bytes} = 261 / 270 = 0{,}96$$

$$f_d = f_3 \times R = 691{,}5 \text{ bps}$$

A pointer movement, here, is a decrement of 3 bytes that makes it possible to fit 24 more bits from VC-4 in the STM-1 frame. The adjustment period is:

$$T_{ptr} = Decrement_{bits} / f_d = 24_{bits} / 691{,}5_{bps}$$

$$T_{ptr} = 34{,}7 \times 10^{-3} s$$

That is, ADM2 decrements the AU-4 pointer every 34.7 ms to compensate for the ADM1 drift (see Figure 1.9).

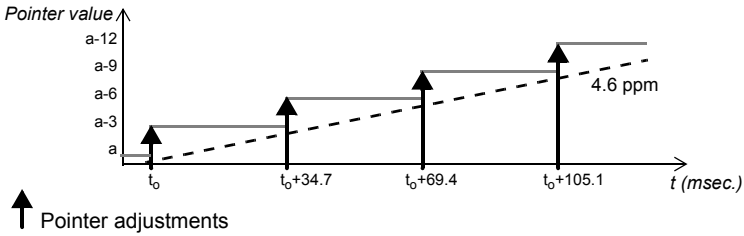



**Figure 1.9** The position of the VC-4 container drifts, due to AU pointer adjustments to compensate for the differences between the two clocks.

### 1.3.2 Phase Fluctuation

In terms of time, the phase of a signal can be defined as the function that provides the position of any significant instant of this signal. It must be noticed that a time reference is necessary for any phase measurement, because only a phase relative to a reference clock can be defined. A significant instant is defined arbitrarily; it may for instance be a trailing edge or a leading edge, if the clock signal is a square wave (see Figure 1.10).

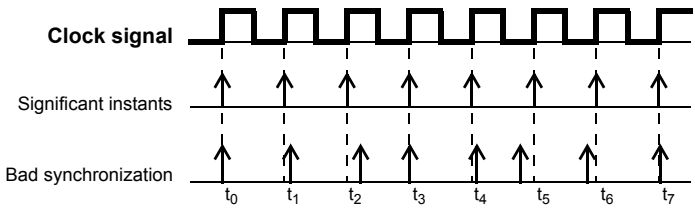



**Figure 1.10** Phase error of a signal in relation to its ideal frequency.

Here, when we talk about a phase, we think of it as being related to clock signals. Every digital signal has an associated clock signal to determine, on reception, the instants when to read the value of the bits that this signal is made up of. The clock recovery on reception circuits reads the bit values of a signal correctly when there is no phase fluctuation, or when there is very little. Nevertheless, when the clock recovery circuitry cannot track these fluctuations (absorb them), the sampling instants of the clock obtained from the signal may not coincide with the correct instants, producing bit errors.

When phase fluctuation is fast, this is called jitter. In the case of slow phase fluctuations, known as wander, the previously described effect does not occur.

Phase fluctuation has a number of causes. Some of these are due to imperfections in the physical elements that make up transmission networks, whereas others result from the design of the digital systems in these networks.

#### 1.3.2.1 Jitter

Jitter is defined as short-term variations of the significant instants of a digital signal from their reference positions in time, ITU-T Rec. G.810 (see Figure 1.11). In other words, it is a phase oscillation with a frequency higher than 10 Hz. Jitter causes sampling errors and provokes slips in the *phase-locked loops* (PLL) buffers (see Figure 1.12). There are a great many causes, including the following:

*Jitter in regenerators*

As they travel along line systems, SONET and SDH signals go through a radio-electrical, electrical, or optical process to regenerate the signals. But clock recovery in regenerators depends on the bit pattern transported by the signal, and the quality of the recovered clock becomes degraded if transitions in the pattern are distributed heterogeneously, or if the transition rate is too low. This effect can be countered by means of scrambling, which is used to destroy correlation of the user-generated bit sequence. The most commonly used line codes add extra transitions in the pattern, to allow proper clock recovery at the receiving end.

Moreover, this type of jitter is accumulative, which means that it increases together with the increase in the number of repeaters looked at.

*Jitter due to mapping/demapping*

Analog phase variation in tributary signals is sampled and quantized when these are multiplexed in a higher-order signal. This is an inherent mechanism in any TDM system. In SDH, for instance, every 125 μs, certain bytes of the phase are available for adjusting the phase. In short, the phase of tributary signals is quantized.

Also, a tributary signal may be synchronized with a different clock than the clock used to synchronize the aggregate signal that will carry it. The above situations give rise to *phase justification*: Bits of the tributary signal are justified, to align them with the phase of the aggregate signal frame; that is, creating jitter.

*Pointer jitter*

The use of pointers in SDH/SONET makes it possible to discard the effects of bad synchronization, but these pointer movements provoke an extensive phase fluctuation. Pointer movements are equal to discontinuities in the transported tributaries.

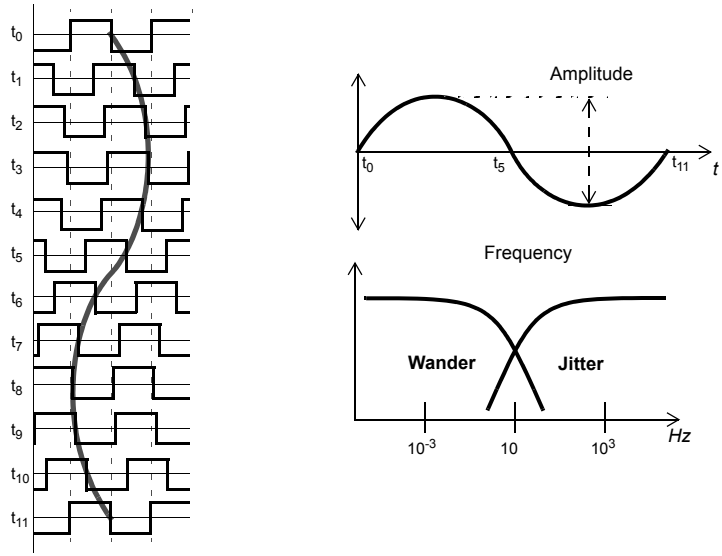



**Figure 1.11** A phase fluctuation of a signal is an oscillating movement with an amplitude and a frequency. If this frequency is more than 10 Hz, it is known as jitter, and when it is less than that, it is called wander.

Once the tributary has been extracted, the PLL circuit must continuously adapt itself to bit flows. If the VC-4 pointer has incremented in an STM-1, it will receive 24 bits less, and it must slow down to maintain a constant level for its buffer. If by contrast it has decremented, it will receive 24 bits more and should accelerate. As a result, the extracted tributary will contain jitter.

### 1.3.2.2 Wander

Wander is defined as long-term variations of the significant instants of a digital signal from their reference positions in time (ITU-T Rec. G.810). Strictly speaking, wander is defined as the phase error comprised in the frequency band between 0 and 10 Hz of the spectrum of the phase variation. Wander is difficult to filter when crossing the *phase-locked loops* (PLLs) of the SSUs, since they hardly attenuate phase variations below 0.1 Hz. This is because slow phase variations get compensated with pointer adjustments in SDH/SONET networks, which is one of the main causes of jitter (see Figure 1.11).

Wander brings about problems in a very subtle way in a chained sequence of events. First, it causes pointer adjustments, which are then reflected in other parts of the network in the form of jitter. This in its turn ends up provoking slips in the output buffers of the transported tributary.

The following are the most typical causes of wander:

*Changes in temperature*

Variations between daytime and nighttime temperature, and seasonal temperature changes have three physical effects on transmission media:

- There are variations in the propagation rate of electrical, electromagnetic or optical signals.
- There is variation of length, when the medium used is a cable (electrical or optical), due to changes between daytime and nighttime or winter and summer.
- There is different clock behavior when temperature changes occur.

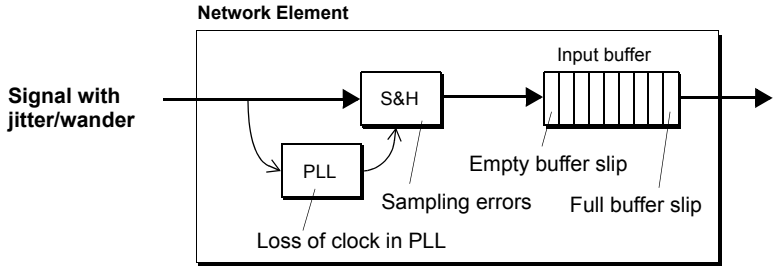



**Figure 1.12** Jitter and wander affect every stage of data recovery, producing a number of sampling errors, clock, losses, and overflow.

*Clock performance*

Clocks are classified according to their average performance in accuracy and offset. The type of resonant oscillator circuit used in the clock source and the design of its general circuitry both add noise, and this results in wander.

## 1.4 Synchronization of Transmission Networks

T-carrier and PDH networks have their first hierarchy perfectly synchronous. In E1 and DS1 frames, all the channels are always situated in their own timeslots. The rest of the hierarchical multiplexion levels are not completely synchronous, but frequency differences can be accommodated by the bit stuffing mechanism.

T-carrier and PDH nodes do not need to be synchronized, since each of them can maintain their own clock. The only requirement is that any clock variations must

be kept within the specified limits, so that the available justification bits can be fitted in without problems caused by clock differences.

**Table 1.2**
Stratum timing accuracy.

| *Stratum* | *Identifier* | *Accuracy* | *Drift* |
|---|---|---|---|
| 1 | ST1 | $1 \times 10^{-10}$ | 2.523/year |
| 2 | ST2 | $1.6 \times 10^{-8}$ | 11.06/day |
| 3 | ST3 | $4.6 \times 10^{-6}$ | 132.48/hour |
| 4 | ST4 | $3.2 \times 10^{-5}$ | 15.36/minute |

### 1.4.1 Synchronization in SONET and SDH

In SONET and SDH, the NEs must be synchronized to reduce pointer movements to a minimum. Pointer movements, as we have seen, are a major cause of jitter. The synchronization network follows a master-slave hierarchical structure:

- *Primary reference clock,* in SDH, or *primary reference source,* in SONET: This is the one that provides the highest quality clock signal. It may be a cesium atomic clock, or a *coordinated universal time* (UTC) signal transmitted via the GPS system.
- *Synchronization supply unit,* in SDH, or *building integrated timing supplies,* in SONET: This clock takes its reference from the PRC and provides timing to the switching exchanges and NEs installed in the same building (it is also known as *building synchronization unit*) or on the same premises. It is usually an atomic clock, although not of such a high quality as the PRC.
- *Synchronous equipment clock* (SEC): This clock takes its reference from an SSU, although it is of lower quality (for example, quartz). It is the internal clock of all the NEs (multiplexer, ADM, etc.).

Whereas a PRC/PRS clock is physically separate from the SDH/SONET network, an SSU/BITS clock may be a separate piece of equipment, in which case it is called a *stand-alone synchronization equipment*, or it may be integrated into an NE (DXC or multiplexer). By definition, an SEC is integrated into an NE. The timing between clocks is transmitted by SDH/SONET sections (STM-*n*/OC-*m*) or PDH/T-carrier paths (2 or 1.5 Mbps) that can cross various intermediary PDH/T-carrier multiplexing stages, and various PDH/T-carrier line systems. The interfaces for these clocks are 2 or 1.5 Mbps, 2 or 1.5 MHz and STM-*n*/OC-*m*, and their presence or absence depends on the specific implementation of the device.

#### 1.4.1.1 SONET synchronization network

In a SONET synchronization network, the master clock is called *primary reference source* (PRS), whereas slave clocks are building integrated timing supply (BITS) that end up synchronizing the NEs. The GR-1244-CORE specifies the rules and performance margins for both PRS and BITS.

BITS synchronizes the network equipment, and it is also used by switches. The performance required to synchronize a node is Stratum 3 (see Table 1.2).

#### 1.4.1.2 SDH synchronization network

In an SDH synchronization network, the master clock is called *primary reference clock* (PRC), whereas *synchronization supply units* (SSUs) are slave clocks and the NE is a *synchronous equipment clock* (SEC). All of them must be kept inside the performance margins defined by the corresponding recommendations (see Table 1.3).

**Table 1.3**
SDH timing accuracy.

| *Use* | *Accuracy* | *Drift* | *ITU-T* |
|---|---|---|---|
| PRC | $1 \times 10^{-11}$ | — | G.811 |
| SSU-T | $5 \times 10^{-10}$ | $10 \times 10^{-10}$/day | G.812 |
| SSU-L | $5 \times 10^{-8}$ | $3 \times 10^{-7}$/day | G.812 |
| SEC | $4.6 \times 10^{-6}$ | $5 \times 10^{-7}$/day | G.813 |

### 1.4.2 Synchronization Models

In SDH/SONET networks, there are at least four ways to synchronize the add and drop multiplexers (ADM) and *digital cross connects* (DXC) (see Figure 1.13):

1. *External timing*: The NE obtains its signal from a BITS or *stand-alone synchronization equipment* (SASE). This is a typical way to synchronize, and the NE usually also has an extra reference signal for emergency situations.
2. *Line timing*: The NE obtains its clock by deriving it from one of the STM-*n*/OC-*m* input signals. This is used very much in ADM, when no BITS or SASE clock is available. There is also a special case, known as *loop timing*, where only one STM-*n*/OC-*m* interface is available.
3. *Through timing*: This mode is typical for those ADMs that have two bidirectional STM-*n*/OC-*m* interfaces, where the Tx outputs of one interface are syn-

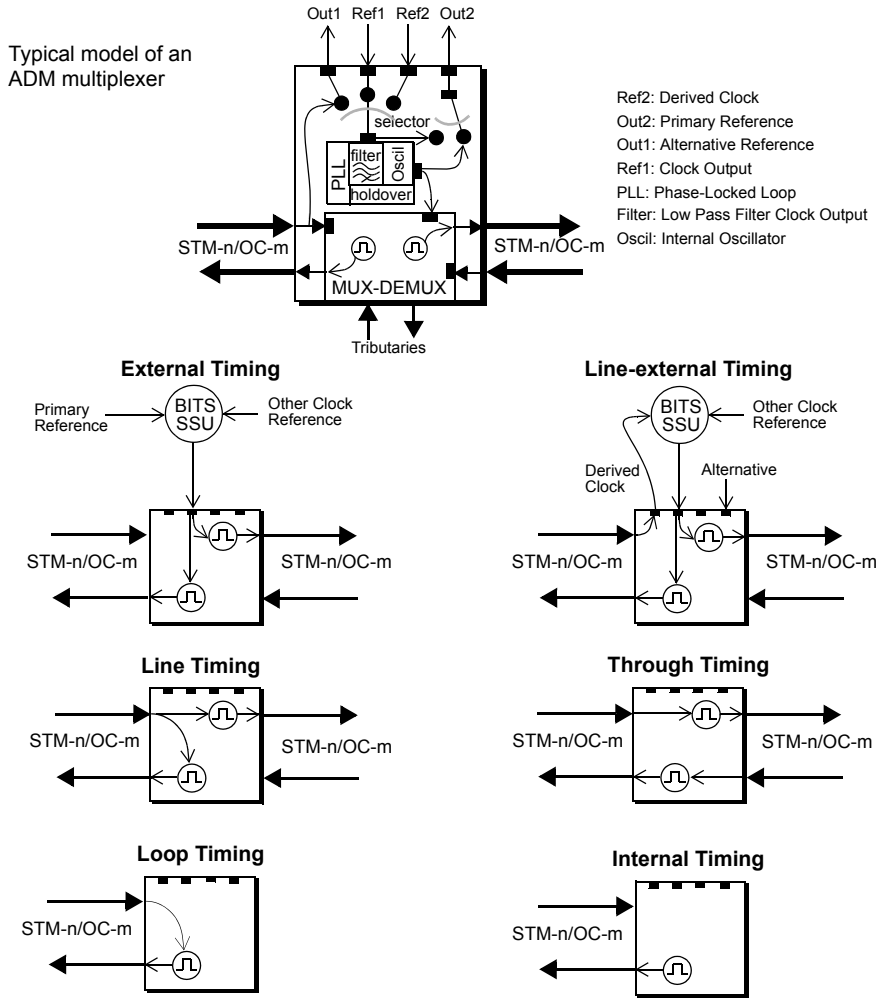



**Figure 1.13** Synchronization models of SDH/SONET network elements.

chronized with the Rx inputs of the opposite interface.

4. *Internal timing*: In this mode, the internal clock of the NE is used to synchronize the STM-*n*/OC-*m* outputs. It may be a temporary holdover stage after losing the synchronization signal, or it may be a simple line configuration where no other clock is available.

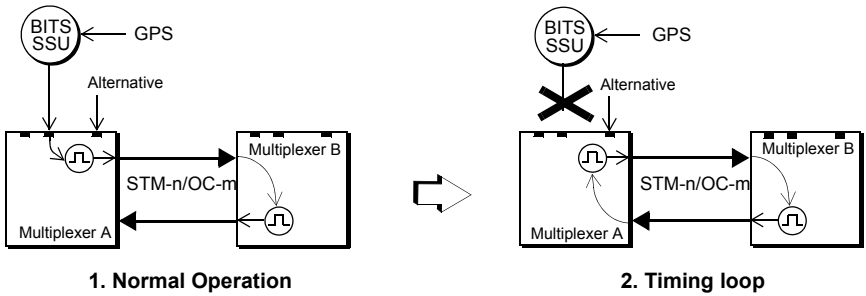



**Figure 1.14** A synchronization pitfall. The multiplexer A, when left without a reference, should have remained in holdover state, if it did not have another clock signal. Generally, secondary clock references should not be taken in line timing synchronization.

### 1.4.3 Timing Loops

A timing loop is in bad synchronization when the clock signal has closed itself, but there is no clock, either master or slave, that would autonomously generate a non-deficient clock signal. This situation can be caused by a fault affecting an NE in such a way that it has been left without a reference clock, and therefore it has chosen an alternative synchronization: a signal that has turned out to be the same signal, returning by another route (see Figure 1.14). A synchronization loop is a completely unstable situation that may provoke an immediate collapse of part of the network within the loop.

The ring network synchronization chain should avoid a synchronization loop (see Figure 1.15).

## 1.5 Digital Synchronization and Switching

Digital switching of *n* x 64-Kbps channels implies that the E1 and T1 frames must be perfectly aligned to make it possible to carry out channel exchange (see Figure 1.16).

The frames are lined by means of a buffer in every input interface of a switch. The bits that arrive at $f_i$ frequency get stored in them, to be read later at the frequency used by the switch, $f_o$.

But if the clocks are different, $|f_i - f_o| > 0$, the input buffer sooner or later ends up either empty or overloaded. This situation is known as a *slip*: If the buffer becomes empty, some bytes are repeated, whereas if the buffer is overloaded, some valid bits must be discarded in order to continue working. That is to say, slips are

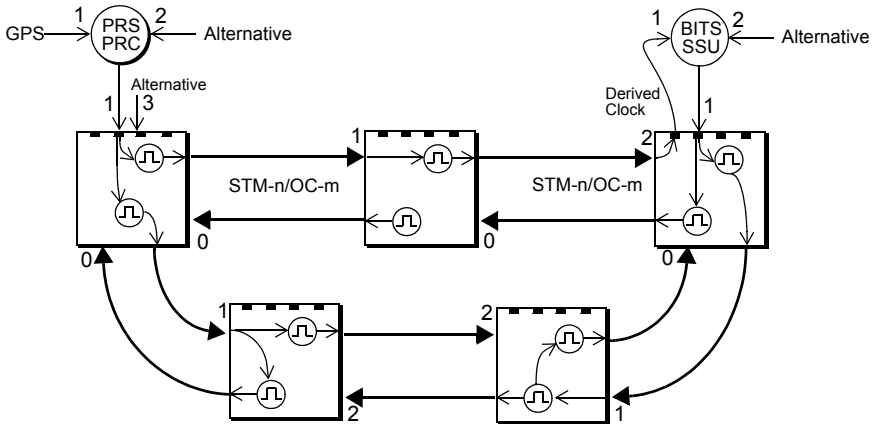



**Figure 1.15** The ring network synchronization chain. "1" is the primary reference, "2" and "3" are alternative clocks, and "0" is to avoid a synchronization loop.

errors that occur when PLLs cannot adapt themselves to clock differences or phase variations in frames.

$$f_d = 86{,}000 \times |f_i - f_o| / n \qquad (slips/day)$$

where
86,400 is number of seconds per day
n: bits repeated or discarded per slip
$f_i$ = input bit rate
$f_o$ = output bit rate

When effects are caused by slips:

- In the *voice* they are usually not noticed; a click may be noticed when voice is sent compressed;
- In a *facsimile* they may damage many text lines;
- In *modems* they cause microbreaks and may sometimes break the whole connection;
- In *digital TV*, there is loss of color or frame synchronization;
- In *data networks* like SNA, HDLC, frame relay, TCP/IP, there is loss of performance.

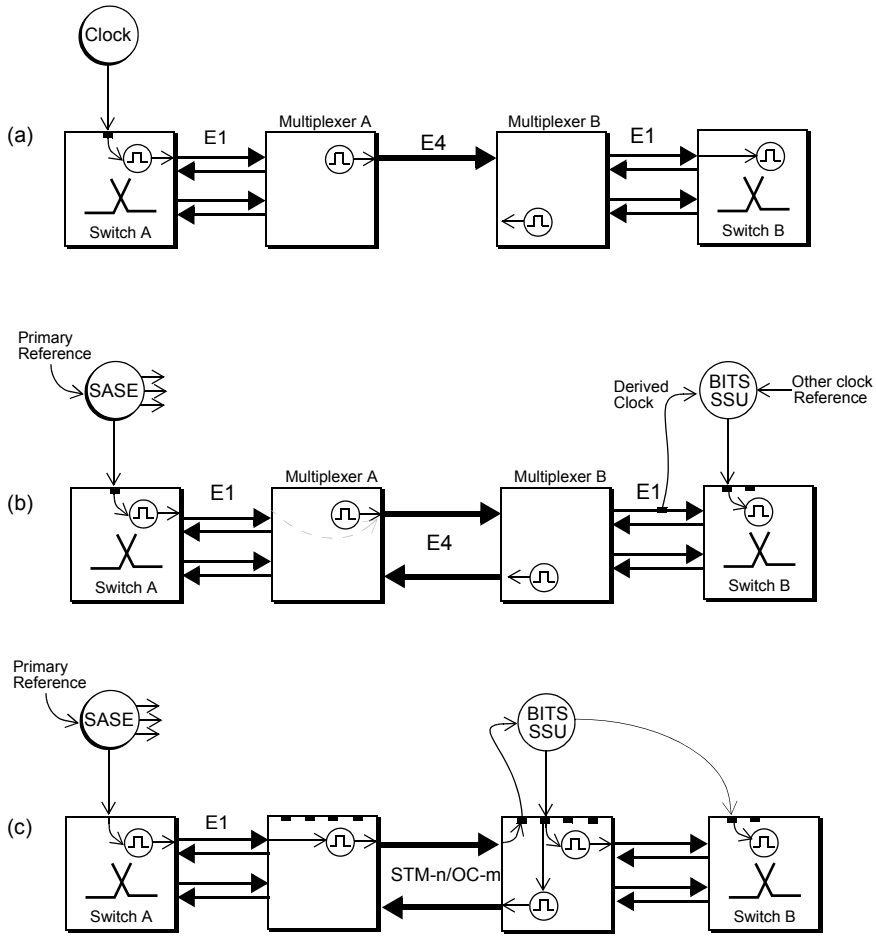



**Figure 1.16** Synchronization of two digital centrals: (a) by signal derived from the PDH chain; (b) by PDH and SASE chain; and (c) across SDH network.

## 1.6 SSU IN A SYNCHRONIZATION NETWORK

The SSU is in charge of synchronizing all the NEs of its node. It has many alternative clock inputs or references, to confront possible clock signal losses. It may be integrated in an ADM or CXC multiplexer, or it can be a stand-alone equipment, in which case it is known as SASE (see Figure 1.17).

Depending on their performance, there are two types of SSUs:

- *Synchronization supply unit transit* (SSU-T): These are of higher quality and they are used to synchronize NEs, or as references for other SSUs.
- *Synchronization supply unit local* (SSU-L): These are of lower quality, and they only synchronize the NEs of their own node.

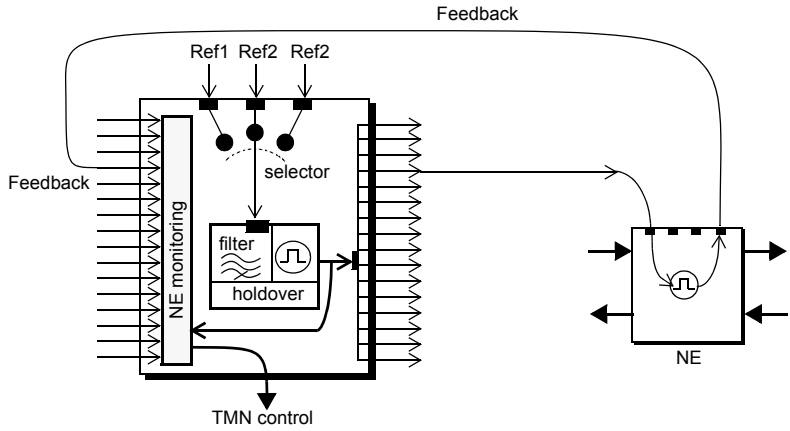



**Figure 1.17** Diagram of an SSU function model.

### 1.6.1 Functions of SSU

An SSU has many functions, and they can be described as follows:

1. The SSU accepts many clock references, tests their performance and selects one of them, filtering it from noise and other interference.
2. It sends the signal chosen to an internal oscillator that acts as a reference to generate a new synchronization signal.
3. The new signal is distributed between all the NEs of its node, and it may also be sent to another SSU in another node.
4. If the reference chosen starts to degrade or is lost, the SSU should switch to one of its alternative references.
5. If no valid reference is found, the SSU enters holdover mode, generating a clock of its own that emulates the characteristics of the previous valid reference.

In the case of an SASE, there are other functions as well:

1. It monitors the synchronization status of the NEs of its node by means of return links.
2. It continuously informs the TMN control level of both its own synchronization status and that of the NEs of its node.

## 1.7 TREATMENT OF JITTER

Jitter is one of the three effects that disturb the timing of networks that are traditionally considered: jitter, wander and slips. The first two are variations of the same physical effect: phase fluctuation. Slips are a different phenomenon, although related to the above.

### 1.7.1 Phase fluctuation

In temporary terms, the phase of a signal can be defined as the function that provides the position of any significant instant of said signal relative to its origin in time. A significant instant is defined arbitrarily, for instance it may be a trailing edge or leading edge if the signal is a square wave (clock signal).

In this field, when we talk about a phase we think of this as being related to clock signals. Every digital signal has an associated clock signal, through which are determined, on reception, the instants in which the value of the bits it is made up of must be read. The circuits of clock recovery on reception read the bit values of a signal correctly when there is no phase fluctuation or when there is very little. Nonetheless, when the phase fluctuation presented by the signal received is fast enough, due to technological limitations, said circuits may not be able to trace these fluctuations (absorb them). It is in these cases that the sampling instants of the clock obtained from the signal may not coincide with the correct instants, producing bit errors.

When the phase fluctuation is fast, this is called *jitter*. In the case of slow phase fluctuations, known as *wander*, the previously described effect does not occur. Random pointer adjustments do occur, however, that may be the cause of *jitter* in the tributary signals carried by the synchronous signals.

### 1.7.2 Causes of phase fluctuation

Phase fluctuation has various causes. Some of these are due to imperfections in the physical elements that make up the transmission networks, whereas others result from the design of the digital systems in said networks.

#### 1.7.2.1 Frequency deviations

There are two cases in which frequency deviations occur between clocks that are significant for transmission networks:

- on the border between two synchronized networks with different primary reference clocks;
- when in a synchronization network a *servant* clock becomes disconnected from its *master* clock, entering holdover mode.

Given that the phase is the integral of the frequency, a frequency offset will produce a phase fluctuation or variation that will be its integral. For instance, a constant frequency offset produces a linear phase fluctuation.

#### 1.7.2.2 Wander in the clock sources

The type of resonant oscillator circuit used in the clock source and in the design of its general circuitry add noise to the clock signal generated, which results in slow phase fluctuation or *wander*.

#### 1.7.2.3 Jitter in the regenerators

As they travel along the line systems, the PDH and SDH signals suffer the generation process (radio-electrical, electrical or optical repeaters). The faulty recuperation of the timing in the repeaters and the intersymbol interference owing to the lack of equalization may lead to *jitter* that depends on the shape of the data signal transmitted. Moreover, this type of jitter is accumulative, i.e. it increases in line with the increase in the number of repeaters looked at. This effect can be countered in SDH by means of scrambling, which creates a new wave shape for the data carried in each regenerator section.

#### 1.7.2.4 Wander due to temperature variation

Variations in temperature between daytime and night, and between the different seasons, have two physical effects on transmission media:

- variation of propogation rate of electromagnetic waves;
- variation of length when the media used is a cable, be it electrical or optical.

#### 1.7.2.5 Jitter due to phase quantification

Analog phase variation in tributary signals is sampled and quantified when these are multiplexed in a higher order (nivel superior) signal. It is a mechanism inherent in any TDM system. In SDH, for instance, every 125 μs there are certain bytes of the

phase available for adjusting the phase. In short, the phase of the tributary signals is quantified.

Passing now to other matters, a tributary signal may have been generated in a different geographical location to the aggregate signal that will carry it, and will therefore be synchronized with a different reference clock.

The above situations give rise to the phenomena of justification of the phase: bits of the tributary signal are justified to align them with the phase of the frame of the aggregate signal, in short creating a jitter.

#### 1.7.2.6 Jitter due to desynchronization of tributary signals

Phase fluctuation resulting from justification does not constitute a problem so long as the tributary signal travels in the aggregate signals. However, when we want to recover the tributary signal (for instance, a PDH signal that is travelling inside an SDH signal), the effect of the phase justification (pointer adjustments) becomes noticeable and the desynchronizers must employ techniques that minimize the *jitter* introduced, a phase transient that can only be controlled in the best of cases.

### 1.7.3 Consequences of phase fluctuations

Whereas in PDH networks *wander* is irrelevant since it is absorbed by the receiver circuits (phase looked loops or PLL) because it is so slow and can be traced, *jitter* reduces the operation margin of the system. In SDH systems both types of fluctuation are relevant, *jitter* due to the presence of PLL in the clock recovering circuits and *wander* because of the presence of FIFO-type buffers.

Some of the effects of these fluctuations are:

- bit errors;
- high amplitude or low frequency *jitter* has the effect of varying the average rate of the input signal; this can lead to emptying or saturation in input buffers, and therefore to slips in PDH systems of pointer adjustments in SDH systems;
- undesired phase modulations in digitalized analog signals carried by SDH networks, especially TV signals;
- in mixed PDH/SDH networks, *wander* causes random pointer adjustments that lead to *jitter* in the payload carried, possible slips and an overall worsening of quality.

### 1.7.4 Jitter metrics and measurement

The parameters that characterize the jitter of a digital signal are amplitude and frequency. The amplitude quantifies the extent to which a significant instant deviates from its ideal reference position. The frequency tells us how quickly this significant instant is moving relative to its ideal position in time.

If we look at the amplitude of phase fluctuation with time as a recurrent signal, when its frequency is higher than 10 Hz the fluctuation is said to be fast and this is jitter. Phase fluctuation is not usually a recurrent signal in real cases, and for this reason we analyze the presence of frequency components in its spectrum above or below 10 Hz to determine if what we have is jitter or wander.

#### 1.7.4.1 Unitary interval

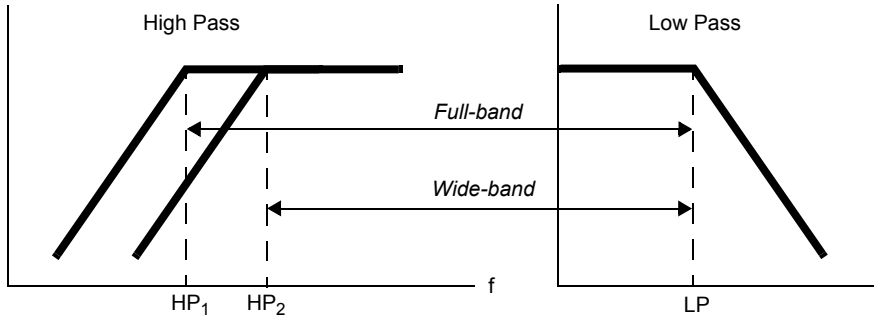
With the aim of freeing the quantification of the jitter (amplitude) of the signal rate being considered, a unit of measurement for amplitude has been defined that is called *unitary interval* (UI). A unitary interval is defined as the time equivalent to the bit time for the work rate being considered. Thus, a unitary interval for a 2 Mbit/s signal corresponds to approximately $488 \times 10^{-9}$ s, whereas for an STM-1 signal it corresponds to 6.4 ns.

#### 1.7.4.2 Jitter measurement filters

The simplest jitter measurements have the goal of obtaining peak-to-peak amplitude values in UI within a specific band of frequencies over a specific measurement interval. This means that any instrument capable of measuring these fluctuations must have a bank of weighting filters that limit the band of the signal measured. These filters are defined (their frequency cutoffs and slopes) by ITU-T recommendations.

ITU-T recommendation G.823 establishes the levels of jitter (in the following figure $B_1$ and $B_2$) that can be found in PDH interfaces, from 64 kbit/s to 140 Mbit/s. Two measurement filters are specified:

- *Full-band*. This filter measures the jitter over the whole band of frequencies on which phase fluctuation is thought to exist, this band depending on the specific hierarchical interface. This filter is specified between the frequencies HP1 and LP (high pass filter and low pass filter, respectively).
- *Wide-band*. This filter allows us to characterize the spectral distribution of the high frequency jitter, which is the jitter that is most likely to cause problems in clock recovery circuits.




| $HP_1$ | $HP_2$ | LP |
|---|---|---|
| 20 Hz | 3 kHz | 20 kHz |
| 20 Hz | 18 kHz | 100 kHz |
| 20 Hz | 3 kHz | 400 kHz |
| 100 Hz | 10 kHz | 800 kHz |
| 200 Hz | 10 kHz | 3500 kHz |

$HP_1$-LP: $B_1$ ($UI_{pp}$)
$HP_2$-LP: $B_2$ ($UI_{pp}$)

| | $B_1$ | $B_2$ |
|---|---|---|
| **64 kbit/s** | 0.25 | 0.05 |
| **2 Mbit/s** | 1.5 | 0.2 |
| **8 Mbit/s** | 1.5 | 0.2 |
| **34 Mbit/s** | 1.5 | 0.15 |
| **140 Mbit/s** | 1.5 | 0.075 |

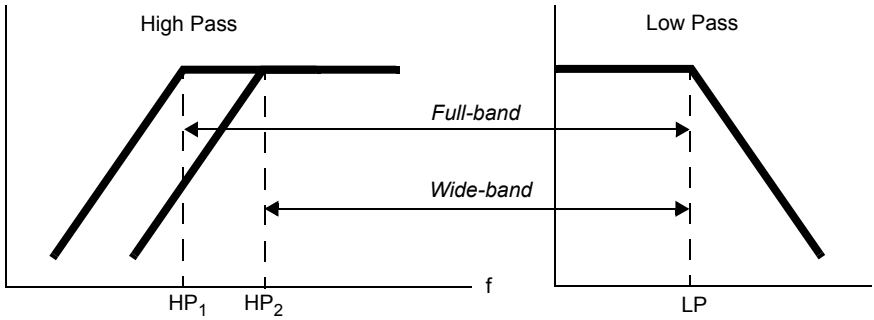
**Figure 1.18** Jitter measurement filters for PDH in line with G.823.

In a similar way to the case of PDH, measurement filters are established for SDH, this time under recommendation G.825. In this case, a full-band filter and a wide-band filter are also defined, as shown below.

In short, the weighting of the measurement via filters serves to find out the spectral content of the jitter in each band of frequencies (pass bands of the programmed filters). These weightings allow conclusions to be drawn when problems appear, or even let us predict them. For instance, the concentration of energy in a specific band of low frequencies may result in the generation of specific synchronization problems or in the operation of the terminal equipment.

### 1.7.4.3 Measurement interval

As mentioned above, the measurement of the amplitude of jitter must be performed over a given measurement interval. The usual measurement period is 60 seconds, although in the case of jitter measurement, longer periods are required owing to pointer adjustments (phase quantification), since these occur sporadically and often infrequently.




| | $HP_1$ | $HP_2$ | LP |
|---|---|---|---|
| **STM-1** | 500 Hz | 65 kHz | 1.3 MHz |
| **STM-4** | 1 kHz | 250 kHz | 5 MHz |
| **STM-16** | 5 kHz | 1 MHz | 20 MHz |

**$HP_1$-LP: 1.5 $UI_{pp}$**

**$HP_2$-LP: 0.15 $UI_{pp}$**

**Figure 1.19** Jitter measurement filters for SDH, in line with G.825.

### 1.7.5 Measurement of jitter in output interfaces

This measurement attempts to quantify the amplitude of jitter (expressed in UI) present in the output port of a specific network element. The ITU specifies and limits the maximum amount of jitter allowed in a network. In particular, ITU-T recommendations G.825 (for SDH) and G.823 (for PDH) limit this maximum amount of jitter in the output ports of network elements. This output jitter may be generated by the network element itself, or it may result from the transfer of jitter from one of the inputs of the element, be it the data input or the synchronization input. The measurement is performed quantifying the amplitude of jitter in a specific bandwidth, specified by the above-mentioned regulations for each rate in the PDH and SDH hierarchies. The measurement diagram can be seen below. Should we wish to measure the jitter generated by the network element itself, we have to connect an input signal that is free of jitter.

### 1.7.6 Measurement of jitter tolerance

Network elements are designed to *tolerate* a certain amount of jitter at their inputs without losing synchronization or introducing errors. This amount is specified in ITU-T recommendations G.823 for PDH and G.958 and G.825 for SDH.

Jitter tolerance is therefore defined as the maximum amplitude of jitter at the input of a network element without producing bit errors or errors of synchronism. These amounts are specified in the form of masks by the recommendations. In these masks jitter amplitude is specified in UI versus frequency. It is recommendable to

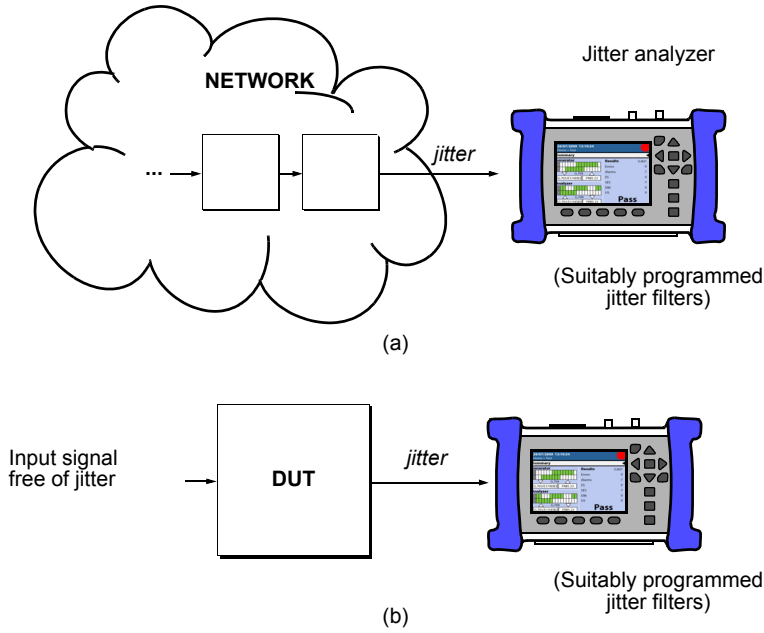



**Figure 1.20** (a)Jitter in output port: general case. (b) Instrinsic jitter. DUT (Device Under Test): is the network element being considered.

synchronize the measurement configuration with a reference clock common to both the network element and the measurement instrument with the aim of avoiding occasional pointer adjustments. The input signal in which jitter will be introduced must be a pattern suitable to the frame rate of the work signal, depending on its hierarchical rate (for instance, those stipulated by O.150 for PDH or test structures O.181 for SDH).

The type of network element considered determines what input and output interfaces come into play to perform the measurement:

- Regenerators: measurements made in the output line interface that corresponds to the input line interface in which jitter is inserted.
- Multiplexers: measurements made on the channel in the output aggregate signal that corresponds to the input interface in which jitter is inserted.
- Demultiplexers: any tributary interface is representative for the aggregate input interface on which jitter is inserted.

More precisely, the measurement is made inserting sinusoidal jitter (by agreement “convención”) in the input port. The amplitude of the tone of jitter introduced

is increased until events are measured in the output port considered. This is repeated at set frequencies. There are three methods of performing the tolerance measurement:

- Onset of errors
- BER penalty
- Excess jitter in output

#### 1.7.6.1 Onset of errors

This is the usual method of checking that the buffering and clock recovery functions are working properly in the network elements. It consists of increasing the jitter amplitude until we can observe the signal deteriorating until it reaches a certain threshold (for instance, the threshold recommended by O.171 - for PDH signals - is two seconds with errors in a period of 30 seconds). At this point, the amplitude is registered of the jitter introduced, which corresponds to the tolerance to this frequency. The test is repeated for a set range of frequencies.

#### 1.7.6.2 BER penalty

This method is more appropriate for line systems (regenerators), normally using optical interfaces. In this case the tolerance level is established when the deterioration of the signal is the same as that produced by lowering the transmission power by 1 dB, i.e. if the error rate produced for a set amplitude of senoidal jitter coincides with that measured when the power is lowered by 1 dB, said amplitude is the tolerance to jitter for that frequency. The test is repeated for a set range of frequencies.

#### 1.7.6.3 Excess jitter in output

If jitter is injected in the input, and in the output of the transmission system considered the jitter measured exceeds the limits of the corresponding interface, it is understood that the tolerance level has been exceeded at the input. This type of test is used in the bringing into service of dedicated lines, following ETSI recommendations.

#### 1.7.6.4 Tolerance masks

Jitter tolerance measurements are aimed at checking that certain limits of jitter amplitude, pre-established by ITU recommendations in a set range of frequencies, are not exceeded. These limits are represented in masks or amplitude-frequency graphs in recommendations G.823 (for PDH) and G.825 (for SDH). The frequencies at which tolerance should be measured are those shown in the masks.

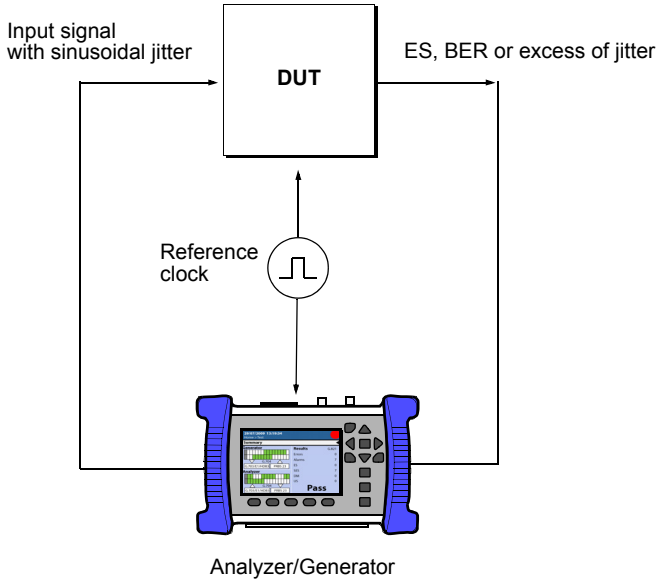


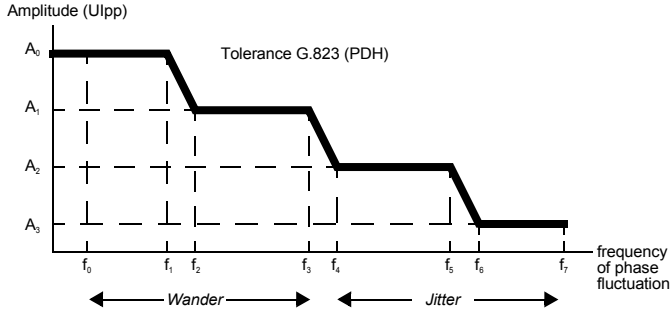

**Figure 1.21** Configuration of measurement for jitter tolerance.

For optical regenerators in SDH networks the recommendation G.958 likewise defines tolerance values by means of two masks: one for A-type devices and another for B-type devices. The mask for A-type devices fits recommendation G.825, while the mask for B-type devices in much more restrictive.

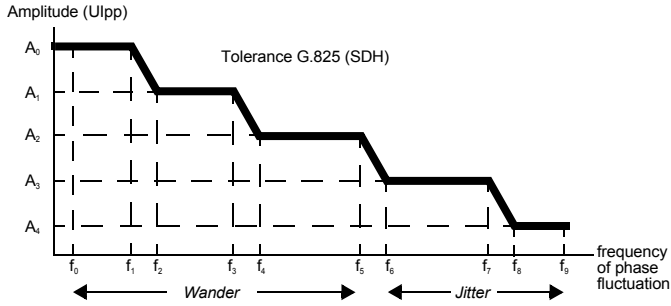
### 1.7.7 Measurement of jitter transfer

Network elements have a limited capacity to eliminate the jitter that may occur in their input ports. In order to evaluate this filtering capacity, the function of jitter transfer is defined as the relation between the amplitudes of jitter in output and input for a set range of frequencies. As is usual in functions of transfer, this relation of amplitudes is expressed in dB. Similarly to the case of tolerance, the jitter introduced in the input of the network element in order to perform the measurement is sinusoidal by nature.

One important aspect to consider is inherent jitter, i.e. the jitter generated inside the network element. In order to perform a correct measurement of transfer this inherent jitter must be substracted from the output jitter, i.e. the measurement must be calibrated. In measurements of transfer there also exists the possibility of applying filter to the output of the network element (as in the case of output jitter). The depends on the particular measurement being performed by the user.




| G.823 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $f_0$ | $f_1$ | $f_2$ | $f_3$ | $f_4$ | $f_5$ | $f_6$ | $f_7$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **64 kbit/s** | 1.15 | - | 0.25 | 1.5 | 12 μHz | - | - | - | 20 Hz | 600 Hz | 3 kHz | 20 kHz |
| **2 Mbit/s** | 36.9 | 18 | 1.5 | 1.5 | 12 μHz | 4.88 mHz | 0.01 Hz | 1.667 Hz | 20 Hz | 2.4 kHz | 18 kHz | 100 kHz |
| **8 Mbit/s** | 152 | - | 1.5 | 1.5 | 12 μHz | - | - | - | 20 Hz | 400 Hz | 3 kHz | 400 kHz |
| **34 Mbit/s** | 618.6 | - | 1.5 | 1.5 | - | - | - | - | 100 Hz | 1 kHz | 10 kHz | 800 kHz |
| **140 Mbit/s** | 2506.6 | - | 1.5 | 1.5 | - | - | - | - | 200 Hz | 500 kHz | 10 kHz | 3.5 MHz |

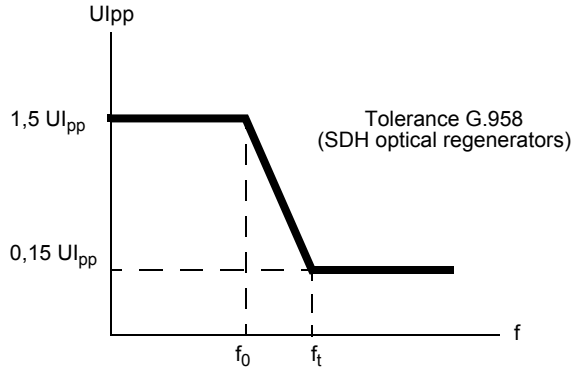



| G.825 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $f_0$ | $f_1$ | $f_2$ | $f_3$ | $f_4$ | $f_5$ | $f_6$ | $f_7$ | $f_8$ | $f_9$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **STM-1** | 2800 | 311 | 39 | 1.5 | (*) | 12 μHz | 178 μHz | 1.6 mHz | 15.6 mHz | 125 mHz | 19.3 Hz | 500 Hz | (**) | 65 kHz | 1.3 MHz |
| **STM-4** | 11200 | 1244 | 156 | 1.5 | 0.15 | 12 μHz | 178 μHz | 1.6 mHz | 15.6 mHz | 125 mHz | 9,65 Hz | 1 kHz | 25 kHz | 250 kHz | 5 MHz |
| **STM-16** | 44790 | 4977 | 622 | 1.5 | 0.15 | 12 μHz | 178 μHz | 1.6 mHz | 15.6 mHz | 125 mHz | 12.1 Hz | 5 kHz | 100 kHz | 1 MHz | 20 MHz |

(*): STM-1e = 0.075; STM1-o = 0.15

(**): STM-1e = 3.25; STM1-o = 6.5

**Figure 1.22** Tolerance masks G.823 and G.825. Note: UIpp is the UI value from peak to peak. Note: STM-1e indicates electrical interface and STM-1o optical.




| Tipo A | $f_0$ | $f_t$ |
|---|---|---|
| **STM-1** | 6.5 kHz | 65 kHz |
| **STM-4** | 25 kHz | 250 kHz |
| **STM-16** | 5 kHz | 1 MHz |

| Tipo B | $f_0$ | $f_t$ |
|---|---|---|
| **STM-1** | 1.2 kHz | 12 kHz |
| **STM-4** | 1.2 kHz | 12 kHz |
| **STM-16** | 1.2 kHz | 12 kHz |

**Figure 1.23** Tolerance masks, G.958.

In line with the measurement configuration shown in the previous figure, the function of jitter transfer J(f) is defined as:

$$J(f) = 20 \log \frac{\text{Output jitter - Inherent jitter}}{\text{Input jitter}} \quad \text{(dB)}$$

### 1.7.7.1 Jitter transfer in PDH

Recommendations G.742 and G.751 establish the requirements of jitter transfer for plesiochronous multiplexers and demultiplexers. These requirements are set out in a common way in accordance with a set mask, in such a way that the performance specified for these network elements will be in line with the tolerable jitter levels in an interface, as specified in recommendation G.823.

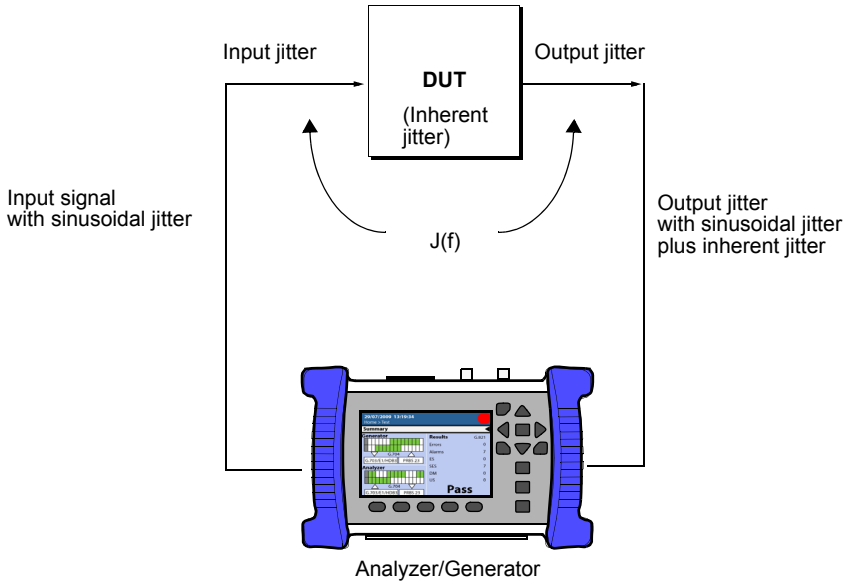


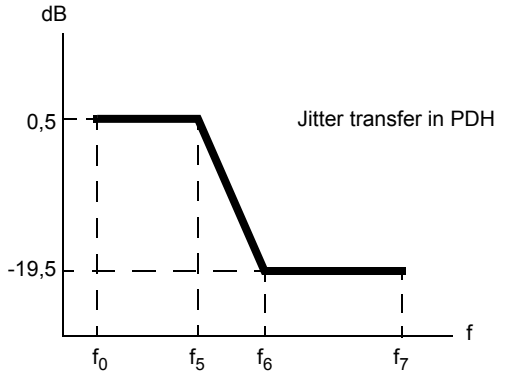

**Figure 1.24** Configuration of measurement of jitter transfer.

One particularity of the transfer measurements in PDH is that the pattern signal is not formed based on pseudo-random binary sequences, but rather with the 4 bit binary word “1000”, as specified, for instance, in point 6 of recommendation G.742.

### 1.7.7.2 Jitter transfer in SDH

In order to check the transfer of jitter between SDH synchronous interface, the network element under test must be synchronized with the input interface in which jitter is generated, since the reference synchronism of the network element is exactly what determines the timing of its STM-N outputs. With this prior condition, it is established that the network element cannot amplify the jitter above 2.3 % (0.2 dB) of the pass-band, which is determined by its clock recovery filter. This bandwith typically reaches 1 Hz for network elements with G.813 category clocks (ETS 300 462-5).

Obviously, it makes sense to check the transfer of jitter between PDH tributary ports of the network element. In this case, the performance of the device must satisfy the previously mentioned recommendations: G.742, G751 and G.823.




| $f_0$ | $f_5$ | $f_6$ | $f_7$ | |
|---|---|---|---|---|
| < 20 Hz | 40 Hz | 400 Hz | 100 kHz | **2 Mbit/s** |
| <20 Hz | 100 Hz | 1 kHz | 400 kHz | **8 y 34 Mbit/s** |
| <20 Hz | 300 Hz | 3 kHz | 800 kHz | **140 Mbit/s** |

**Figure 1.25** Mask of jitter transfer for PDH. Note: the numbering of the frequencies in the graph is not correlative but no significant frequency is missing, this is simply how the mark is shown in the recommendations.

### 1.7.8 Mapping jitter and combined jitter

Jitter from phase quantification and desynchronization results in specific and relevant cases: *mapping jitter* and *combined jitter*.

#### 1.7.8.1 Mapping jitter

Mapping is the process through which PDH signals are introduced in SDH signals for transport. This takes place in multiplexers. The clock source of the signals is independent from the SDH clock source so the PDH data is asychronous with the SDH signals. In other words, the clocks of the tributary systems have no fixed relation with the multiplexer or even between themselves. The tributary signals are plesiochronous, i.e. they allow deviations within a margin of allowance relative to their nominal clock value. In order to resolve this asynchronicity, the background bits process is used, by which the PDH signal becomes part of the payload of a virtual SDH container, which has a greater capacity. This excess capacity is filled with background bits to obtain the constant rate specified for the container.

At the transmitting end, the bits of the tributary signals are continuously recorded in elastic memories, but they are read discontinously, since in order to proceed to

their reading (and later transmission) these memories must first be filled (otherwise they would end up emptying). Reading is carried out at the maximum rate possible, since the clock adaptation process performed by the multiplexer provides the transmission channel with a higher capacity than the sum total of the tributary rates plus the permitted tolerance (deviations relative to the nominal value). Since we want the reading clock to stop at times but the output rate of the multiplexer's aggregate signal must remain constant, background bits are sent when there are no bits of information to be transmitted.

At the receiving end, these background bits must be extracted in order to recover the tributary signals correctly. For this reason, these bits are not written in the elastic memories of the receiver. The frames contain indications that let them decide whether a bit is a background bit or not. If the bit received is a background bit, the writing clock is stopped. On reception, therefore, writing is discontinous whereas reading is continuous (since everything contained in the memory forms part of the message).

On reception, the reading clock is derived from the writing clock, which is discontinuous, by means of a phase locked loop (PLL). Since the low pass filter of the PLL is not able to completely eliminate the discontinuities in the writing process, a residual phase modulation remains, and this is known as *mapping jitter* (also *stuffing jitter*).

#### 1.7.8.2 Combined jitter

Mapping jitter is measured when there are no pointer adjustments in the aggregate signals. The pointer adjustment mechanism is one of the causes of jitter (pointer jitter) but this cannot be separated from the phenomenon of mapping jitter, which is inherent in the generation of SDH signals. For this reason, pointer jitter cannot be measured separately from mapping jitter, which will always be present, and the fluctuation measured is known as combined jitter.

Pointer jitter is the most important kind of jitter found in SDH networks. It represents the main cause of disturbance in hybrid PDH/SDH networks and compared to mapping jitter is a component with much greater weight when it comes to quantifying combined jitter. The cause of this type of phase fluctuation is the pointer adjustment mechanism, and it appears in those tributaries that, once disassembled (extracted from their virtual container), have undergone pointer changes along their path.

The pointer mechanism forms the basis of the structure of SDH signals. The essential difference between an SDH frame and a PDH frame is that in the first, the overhead information from the higher order signals is enough to determine the position of the overheads of the signals in the lower order. Pointers are values (divided

into various octets) that contain the position of the overheads. For example, for the mapping of 2 Mbit/s signals in SDH, two pointer levels are used. The higher level (AU-4 pointer) identifies where the VC-4 virtual containers start within the STM-1 frame. The lower level (TU-12 pointer) identifies the start of a VC-12 virtual container relative to the VC-4. In one STM-1 frame there will therefore be one AU-4 pointer and 63 TU-12 pointers.

When there are clear differences in the clock signals from two different networks or two different elements within the same network, it is necessary to compensate for these differences by *offsetting* the signals from the lower order into the upper order (for example, VC-4 virtual containers in the STM-1 frame). This is achieved by increasing or decreasing the value of the pointer by one unit (depending on the appropriate adjustment at that time). The value of this offset depends on the pointer on which the adjustment is being carried out. Returning to the case of mapping a signal of 2 Mbit/s in SDH, an AU-4 pointer adjustment means an offset of 24 bits, whereas if it is a TU-12 pointer the offset is of eight bits. The adjustment of an AU-4 pointer contributes more to jitter due to the fact that it appears more commonly than TU-12 pointer adjustment.

In any case, these offsets cause abrupt phase variations in lower order signals (tributaries). As is the case with mapping jitter, the reading clock at the receiving end is derived from a PLL circuit. The low pass filter in the control loop of the PLL tries to smooth out these phase jumps, but they nonetheless cause residual phase modulation to remain. This is pointer jitter, and it is the main contributor to combined jitter.

#### 1.7.8.3 Measurement of combined jitter

In order to check how effectively a network element compensates for the effects of pointer adjustments, some pointer adjustments are generated that have been specially designed to submit the element to stress, in such a way that situations are simulated that may taken place under normal working conditions. A pointer adjustment is a change in its value, for instance, a unitary increase or decrease. The pointer sequences are defined in ITU-T recommendation G.783. The measurement consists of checking the output jitter against this entry stimulus. Combined jitter (which is largely pointer jitter) apears in the tributaries of a synchronous signal when these are extracted from the signal. The following figure illustrates the measurement figure with an example.

### 1.7.9 Jitter in dedicated lines

Although tolerance to jitter is usually checked by means of senoidal stimulus, there are certain cases in which this test is not performed in this way, as is the case with dedicated lines. In this type of system it is necessary to have a method that char-

acterizes and supplies more reliable results about the real level of tolerance to jitter than those obtained through the use of frequency tones. This is due to the fact that, although these tones are useful for checking that the buffers of the devices are working correctly, at the end of the day they are not exact enough when it comes to reproducing the random characterstics of the jitter that is found in 'real' systems.

The ETSI has defined a series of broadband signals for checking tolerance to jitter in dedicated lines. These take advantage of the random characteristics of the PRBS patterns in order to modulate the phase of the data signal of the line (2 Mbit/s in the example) following the appropriate filtering. The tolerance of the line to the jitter introduced is evaluated at the remote end of the line depending on the errors that appear and the amount of output jitter; this way, the tests that the European Commission's ONP conditions require all operators to perform on bringing dedicated lines into service can be carried out.

## 1.8 Treatment of wander

With the aim of guaranteeing the correct operation of SDH networks, its elements must be synchronized, i.e. obey a common reference clock. The common reference signal to which the clocks of the network elements themselves are synchronized usually come from high quality clocks that act as Primary Reference Clocks (PRC). Based on these clocks, the signal is distributed in a network of subsiduary clocks until it reaches the network elements. There exists then a network of clocks that synchronizes the SDH network.

Here, wander is a critical type of phase fluctuation, since it becomes accumulative in the synchronization chain. This slow phase fluctuation can often be observed on the border between two different SDH networks, each with its own PRC, and on the international borders where networks are found that use different reference clocks. The causes of this wander are:

- changes in round trip delay in cables (temperature);
- drifts in the Phase Locked Loops (PLL) of the clocks;
- phase fluctuations due to the reconfiguration of the synchronization change, either by the operator themselves or by the automatic protective switching mechanism;
- differences in frequency resulting from a loss of synchronization in a network node (limit of 4.6 ppm).

### 1.8.1 Synchronization of SDH networks

A functional separation can be established between the SDH network and the network of clocks that synchronizes it (even if this separation is not physical is some cases, as will be seen). The synchronization network obeys a master-slave hierarchical structure in which three types of clocks are defined:

- PRC (Primary Reference Clock): this is the one that provides the highest quality clock signal. It may be a Cesium atomic clock, or a UTC coordinated universal time signal transmitted via the GPS system.
- SSU (Synchronization Supply Unit): clock that takes its reference from the PRC and provides timing to the switching exchanges and network elements installed in the same building (it is also sometimes known as *building synchronism unidad*) or on the same premises. It is usually an atomic clock although not of as a high quality as the PRC.
- SEC (Synchronous Equipment Clock): clock that takes its reference from an SSU and of lower quality (may be quartz). It is the internal clock of each network element (multiplexer, ADM, etc.).

Whereas a PRC clock is physically separate from the SDH network, an SSU clock may be a separate piece of equipment, in which case it is called an SASE (Stand Alone Synchronization Equipment), or it may be integrated in a network element (DXC or multiplexer). By its very definition, an SEC is integrated in a network element. The timing between clocks is transmitted via SDH sections (STM-N) or PDH paths (2 Mbit/s) that can cross various intermediary PDH multiplexing stages and various PDH line systems. The interfaces for these clocks are 2 Mbit/s, 2 MHz and STM-N and their presence or absence depends on the specific implementation of the device.

Owing to the problem of wander in synchronization chains, the ITU and the ETSI have produced some recommendations for limiting said phase fluctuation in all these clocks (PRC, SSU and SEC) and guaranteeing the correct operation of the SDH network.

### 1.8.2 Measurement of relative and absolute wander

Understanding wander as the difference of phase (or of time, if you prefer) between two clock signals, it is important to distinguish between relative and absolute measurement of wander.

The absolute measurement of wander at a given instant is the phase difference that exists, at that moment, between the clock of a signal and the Coordinated Universal Time (UTC), as defined in ITU-T recommendation G.810 and ETSI standard

ETS 300 462-1. Carrying out this measurement, for which a high quality clock source is required that is derived directly from the UTC (such as that provided by a GPS receiver), we can see the effective quality provided by the synchronization network.

The measurement of relative wander at a given instant is the phase difference that exists, at that moment, between any two clocks in the network. In particular, it makes sense to perform the measurement of relative wander on two interfaces when we want to check such aspects as the generation of wander in a synchronous element (checking the gap between input and output interfaces), the possible appearance of pointer adjustments between two STM-N signals that converge in a single network element, etc...

In short, the difference between both types of measurement depends on the reference clock chosen: in the case of absolute measurement the clock measured is compared with the most stable reference that exists.

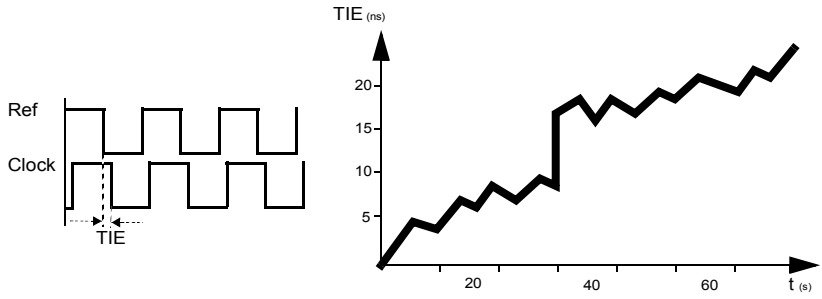



**Figure 1.26** Amplitude of slow phase fluctuation or TIE.

### 1.8.3 The metrics of Wander: TIE, MTIE and TDEV

Given that wander is a slow phase fluctuation (spectral components below 10 Hz), the measurements require long periods of time. It is also necessary to detect phase transients during these measurements, which requires high temporal resolution, and as a result there is a great accumulation of data. With the aim of summarizing this great amount of information, three parameters are defined that are fundamental in the measurement of wander: TIE, MTIE and TDEV.

### 1.8.3.1 TIE (Time Interval Error)

The TIE (Time Interval Error) is the amplitude of the slow phase fluctuation, i.e. it indicates the phase variation of the clock to be measured relative to the phase of an ideal reference clock in each instant of the measurement. Usually, TIE=0 is taken as a reference at the start of the measurement. The TIE can be expressed in absolute time (ns, μs, ms) or relative to the period of the signal (unitary intervals), although it is usually expressed in absolute time.

### 1.8.3.2 MTIE (Maximum Time Interval Error)

The MTIE (Maximum Time Interval Error) is defined as the highest peak to peak value of TIE in a certain observation time, τ. In other words, in order to calculate the MTIE, a temporal window must be scrolled over the function TIE(t), recording the maximum peak to peak value of the TIE: $TIE_{pp}$. This can be repeatedfor different values of τ, thus obtaining a graph of MTIE (τ), as shown below:

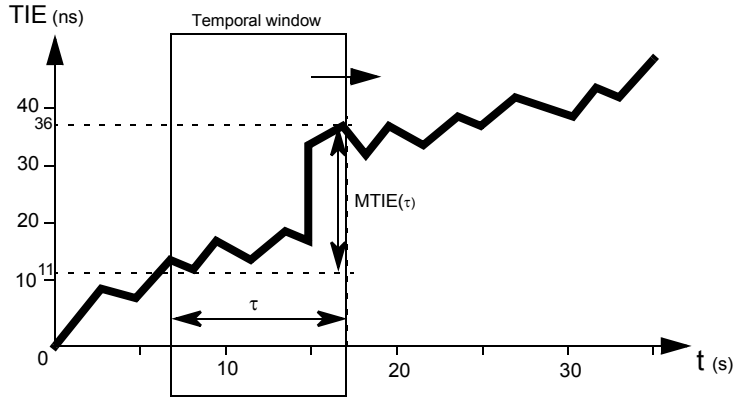



**Figure 1.27** MTIE ($\tau$): maximum peak to peak amplitude of the slow phase fluctuation or TIE in an observation window $\tau$.

### 1.8.3.3 Application of the MTIE

Through the MTIE a good characterization can be obtained of the size of the buffers of the synchronous instruments. The buffers of the digital instruments, associated to the clock recuperators (PLL), allow frequency fluctuations to be absorbed, but they have to have a limited size to avoid increasing latency. These sizes are calculated using the MTIE.

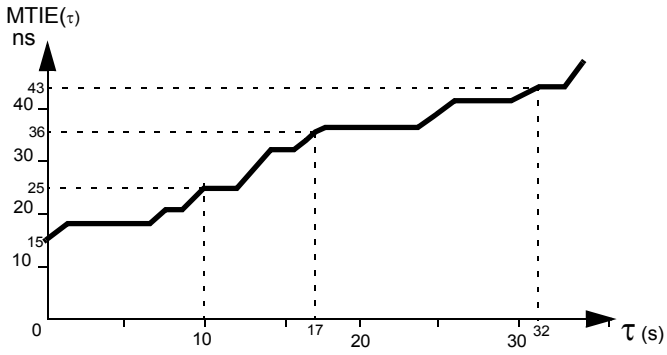



**Figure 1.28** MTIE ( $\tau$) versus observation window $\tau$.

### 1.8.3.4 TDEV (Time Deviation)

Time Deviation of TDEV is a measurement that characterizes the spectral content of the TIE(t) signal. In other words, it gives a measurement of the energy of the frequency components of wander. As is the case with MTIE, the TDEC is a function of the observation time $\tau$. The functional diagram of a TDEC measurement ciruit is shown below.

The first block H(f) is a filter whose pass-band $(0, 1/\tau)$ is centered on the value $0.42/\tau$. The analysis is therefore restricted to the pass-band mentioned. The second block calculates the root mean square value (r.m.s), which evaluates the energy of the components in the band analyzed. By varying the value of $\tau$, we can then analyse the different bands of frequency that interest us. The above considerations have as their source ITU-T recommendation G.810. A correct calculation of the TDEV recommends that the duration of the measurement be $12\tau$ although $3\tau$ is enough, i.e. we must have samples of TIE at least in the time interval $(0, 3\tau)$, t=0 being the instant when the measurement starts. Given that the TDEV is an r.m.s value, it is always positive (sum of square.

### 1.8.3.5 Application of the TDEV

The TDEV allows for the evaluation of the short-term stability of the clock signal. It allows us to characterize the transfer of wander in the network element used in order to limit the accumulation of this phase fluctuation throughout the same (ETSI specifications on transfer of wander between ports of a synchronization source - clock - specify said transfer in terms of TDEV). What's more, the TDEV converges for many types of phase noise, which allows us to identify the source and eventually correct the causes of degradation of transmission.

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