Catálogo de Xilinx

Diseño Lógico 2 - 2022

Instituto de Ingeniería Eléctrica

Facultad de Ingeniería

Universidad de la República

PLD

- Solo Celda Lógicas (Ni memorias, ni DSP)
+ Ultra Low-Power
+ Instant-on

Uso:
- Glue-logic
- Circuitos secuenciales

Cool Runner-II

XC2C128	-4	TQ	G	144	C
Device	Speed Grade -4 thru -10 (Fastest to Slowest)	Package Type QFN Packages (QF): Quad, flat, no-lead (0.5mm lead spacing) VQFP Packages (VQ): Very thin QFP (VQ44: 0.8mm lead spacing, VQ100: 0.5mm lead spacing) Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5mm ball spacing) TQFP Packages (TQ): Thin QFP (0.5mm lead spacing) FBGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0mm ball spacing) FBGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0mm ball spacing)	Pb-Free	Pin Count	Temperature Grade (C, I)

		High performance and ultra-low power consumption in a single-chip, instant-on programmable device (1.8V)					
	Part Number	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
Logic Resources	System Gates	750	1,500	3,000	6,000	9,000	12,000
	Macrocells	32	64	128	256	384	512
	Product Terms Per Macrocell	56	56	56	56	56	56
Clock Resources	Global Clocks	3	3	3	3	3	3
	Product Term Clocks Per Function Block	16	16	16	16	16	16
I/O Resources	Maximum I/O	33	64	100	184	240	270
	Input Voltage Compatible			1.5 / 1.8 / 2.5 / 3.3			
	Output Voltage Compatible			1.5 / 1.8 / 2.5 / 3.3			
Speed Grades	Min. Pin-to-Pin Logic Delay (ns)	3.8	4.6	5.7	5.7	7.1	7.1
	Commercial Speed Grades (Fastest to Slowest)	-4, -6	-5, -7	-6, -7	-6, -7	-7, -10	-7, -10
	Industrial Speed Grades (Fastest to Slowest)	-6	-7	-7	-7	-10	-7(1), -10

XC2C256-7TQG144I : USD 25.6

FPGA

The gate length is also an approximate measure of transistor speed and of how densely you can pack transistors together in a hand-crafted layout.

Serie 6 | 45nm

- Spartan-6:
  - Cost-optimized for system I/O expansion
  - LX
  - LXT: agrega transivers (PCIe y GT)
- Herramientas desarrollo: ISE Design Suite
- Shipments to at least 2027

CoolRunner-II vs SPARTAN-6

	Part Number	XC2C512
Logic Resources	System Gates	12,000
	Macrocells	512
	Product Terms Per Macrocell	56
Clock Resources	Global Clocks	3
	Product Term Clocks Per Function Block	16
I/O Resources	Maximum I/O	270
	Input Voltage Compatible	
	Output Voltage Compatible	
Speed Grades	Min. Pin-to-Pin Logic Delay (ns)	7.1
	Commercial Speed Grades (Fastest to Slowest)	-7, -10
	Industrial Speed Grades (Fastest to Slowest)	-7(1), -10

Part Number	XC6SLX4	XC6SLX45	XC6SLX150	XC6SLX150T
Slices(1)	600	6,822	23,038	23,038
Logic Cells(2)	3,840	43,661	147,443	147,443
CLB Flip-Flops	4,800	54,576	184,304	184,304
Max. Distributed RAM (Kb)	75	401	1,355	1,355
Block RAM (18Kb each)	12	116	268	268
Total Block RAM (Kb)(3)	216	2,088	4,824	4,824
Clock Mgmt Tiles (CMT)(4)	2	4	6	6
Max. Single-Ended I/O Pins	132	358	576	540
Max. Differential I/O Pairs	66	179	288	270
DSP48A1 Slices(5)	8	58	180	180
Endpoint Block for PCIe®	—	—	—	1
Memory Controller Blocks	0	2	4	4
GTP Low-Power Transceivers	—	—	—	8
Commercial Speed Grade(10)	-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N
Industrial Speed Grade(10)	-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N
Configuration Memory (Mb)	2.7	11.9	33.8	33.8

XC6SLX9-2TQG144C (único FPGA con empaque no BGA):

- 2019 : USD 16.52

- 2022: No hay stock

XC6SLX45-2FGG484C : USD 62.93

Serie 7 | 28nm

- Spartan-7
  - Baja densidad, bajo costo. Punto entrada a serie 7
  - Similares recursos a Spartan 6, con mas DSP
  - XC7S50-1FGGA484C : USD 57.96
- Artix-7
  - Orientado a aplicaciones que requieren I/O alta velocidad.
  - Sobre Spartan-7: agrega transivers PCIe y GTP (6.6Gb/s),
- Kintex-7
  - Mejor relación precio/performance.Easy Path
  - Sobre Artix-7: agrega transivers GTX (6.6Gb/s), más DSP para similar cantidad de Logic Cells
- Virtex-7
  - Orientado a High Performance y capacidad. Easy Path
  - Sobre Kintex-7: más de todo!!!
- Herramienta desarrollo: Vivado

Spartan - Artix - Kintex - Virtex

	Part Number	XC7S6	XC7S100
Logic Resources	Logic Cells	6,000	102,400
	Slices	938	16,000
	CLB Flip-Flops	7,500	128,000
Memory Resources	Max. Distributed RAM (Kb)	70	1,100
	Block RAM/FIFO w/ ECC (36 Kb each)	5	120
	Total Block RAM (Kb)	180	4,320
Clock Resources	Clock Mgmt Tiles (1 MMCM + 1 PLL)	2	8
I/O Resources	Max. Single-Ended I/O Pins	100	400
	Max. Differential I/O Pairs	48	192
Embedded Hard IP Resources	DSP Slices	10	160
	Analog Mixed Signal (AMS) / XADC	0	1
	Configuration AES / HMAC Blocks	0	1

	Part Number	XC7A12T	XC7A200T
Logic Resources	Logic Cells	12,800	215,360
	Slices	2,000	33,650
	CLB Flip-Flops	16,000	269,200
Memory Resources	Maximum Distributed RAM (Kb)	171	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)	20	365
	Total Block RAM (Kb)	720	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	10
I/O Resources	Maximum Single-Ended I/O	150	500
	Maximum Differential I/O Pairs	72	240
Embedded Hard IP Resources	DSP Slices	40	740
	PCIe® Gen2[1]	1	1
	Analog Mixed Signal (AMS) / XADC	1	1
	Configuration AES / HMAC Blocks	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]	2	16

	Part Number	XC7K70T	XC7K480T
	EasyPath™ Cost Reduction Solutions[1]	—	XCE7K480T
Logic Resources	Slices	10,250	74,650
	Logic Cells	65,600	477,760
	CLB Flip-Flops	82,000	597,200
Memory Resources	Maximum Distributed RAM (Kb)	838	6,788
	Block RAM/FIFO w/ ECC (36 Kb each)	135	955
	Total Block RAM (Kb)	4,860	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)	6	8
I/O Resources	Maximum Single-Ended I/O	300	400
	Maximum Differential I/O Pairs	144	192
Integrated IP Resources	DSP48 Slices	240	1,920
	PCIe® Gen2[2]	1	1
	Analog Mixed Signal (AMS) / XADC	1	1
	Configuration AES / HMAC Blocks	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)	8	32

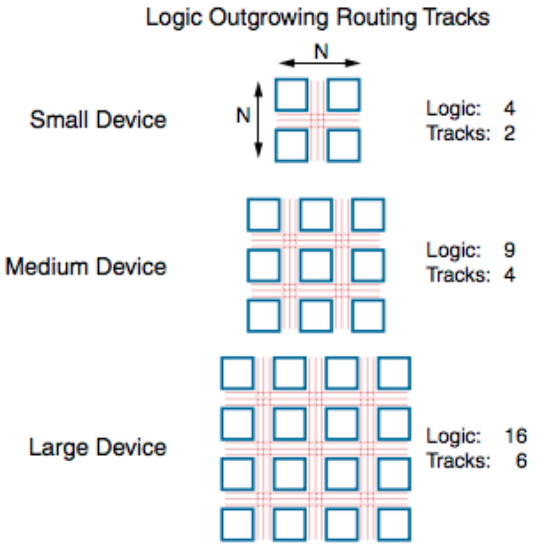
	Part Number	XC7VX330T	XC7VH870T
	EasyPath™ Cost Reduction Solutions[1]	XCE7VX330T	—
Logic Resources	Slices	51,000	136,900
	Logic Cells	326,400	876,160
	CLB Flip-Flops	408,000	1,095,200
Memory Resources	Maximum Distributed RAM (Kb)	4,388	13,275
	Block RAM/FIFO w/ ECC (36 Kb each)	750	1,410
	Total Block RAM (Kb)	27,000	50,760
Clocking	CMTs (1 MMCM + 1 PLL)	14	18
I/O Resources	Maximum Single-Ended I/O	700	300
	Maximum Differential I/O Pairs	336	144
Integrated IP Resources	DSP Slices	1,120	2,520
	PCIe® Gen2[2]	—	—
	PCIe Gen3	2	3
	Analog Mixed Signal (AMS) / XADC	1	1
	Configuration AES / HMAC Blocks	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)[3]	—	—
	GTH Transceivers (13.1 Gb/s Max Rate)[4]	28	72
	GTZ Transceivers (28.05 Gb/s Max Rate)	—	16

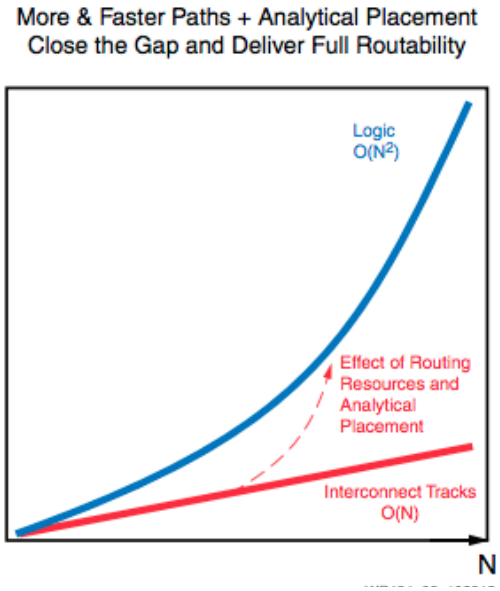
No alcanza!!

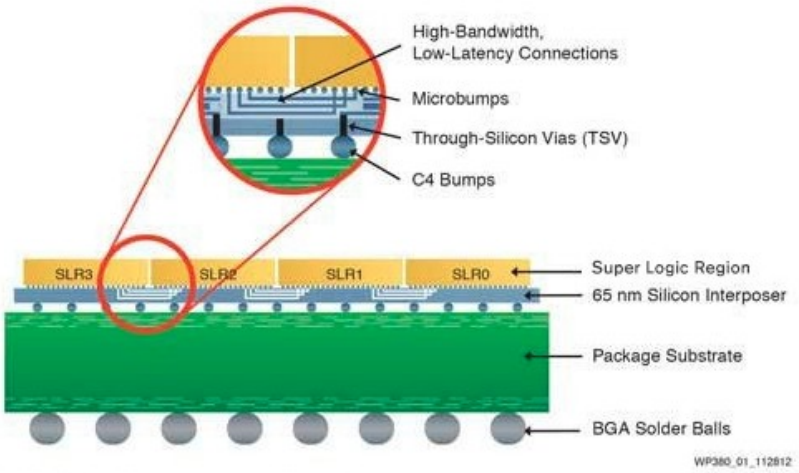
- red 1Gb/s -> multiples 100Gb/s a 1Tb/s
- video: 1080p -> 4K y 8K
- celular: 3G -> LTE a LTE Advanced

- Sumado a requerimientos seguridad (+capacidad computo)
- Solución: UltraScale (20nm)

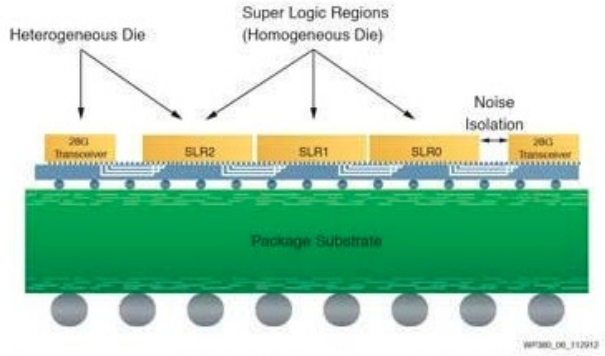
UltraScale | 20nm: + rutas > -delay







FPGA Enabled by SSI Technology



Heterogeneous 3D FPGA with Integrated 28G Transceivers

UltraScale | 20nm: +clk buf > -skew

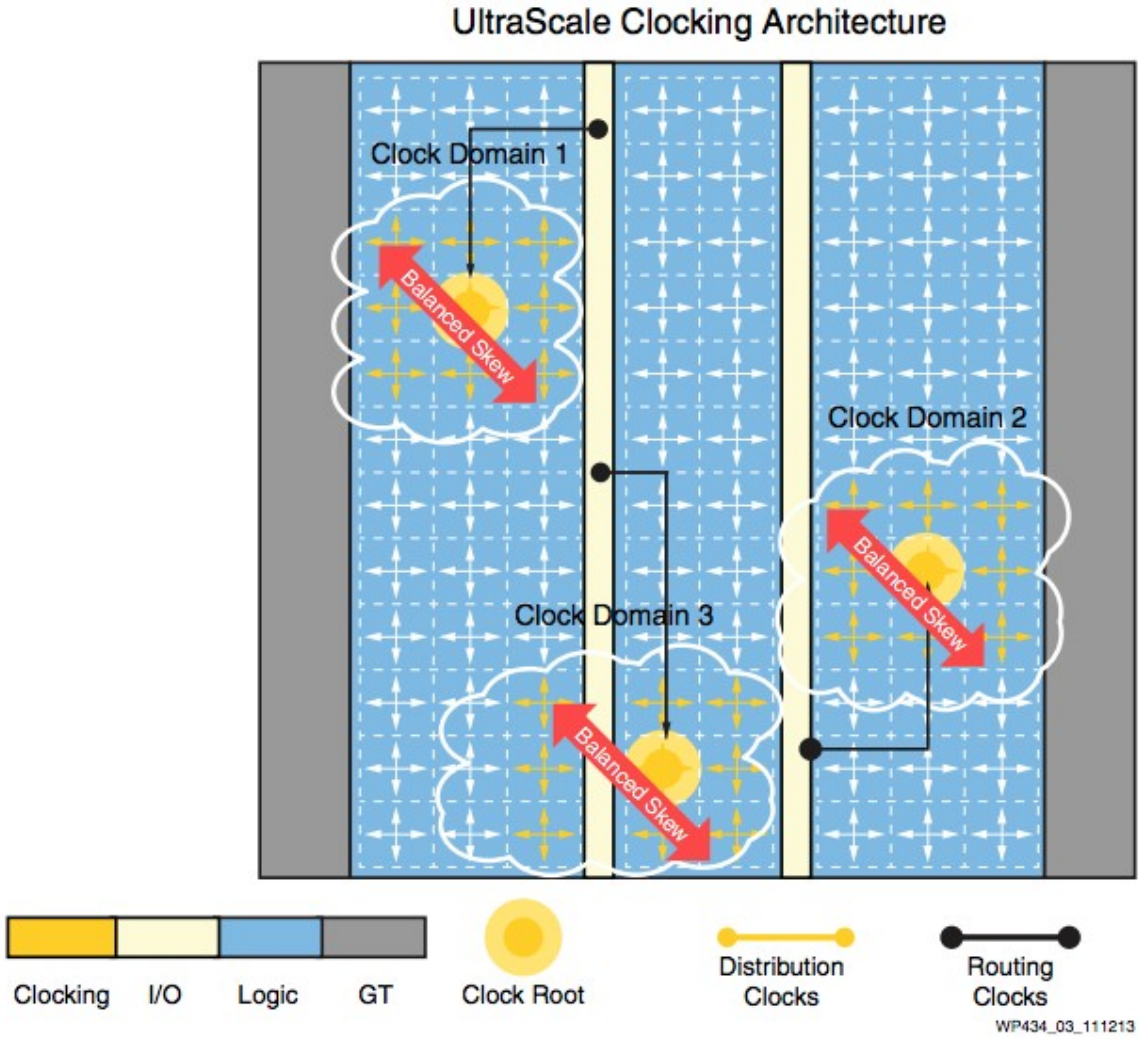


Figure 3: **UltraScale Clocking Architecture**

UltraScale|20nm: nCLB > +optimo

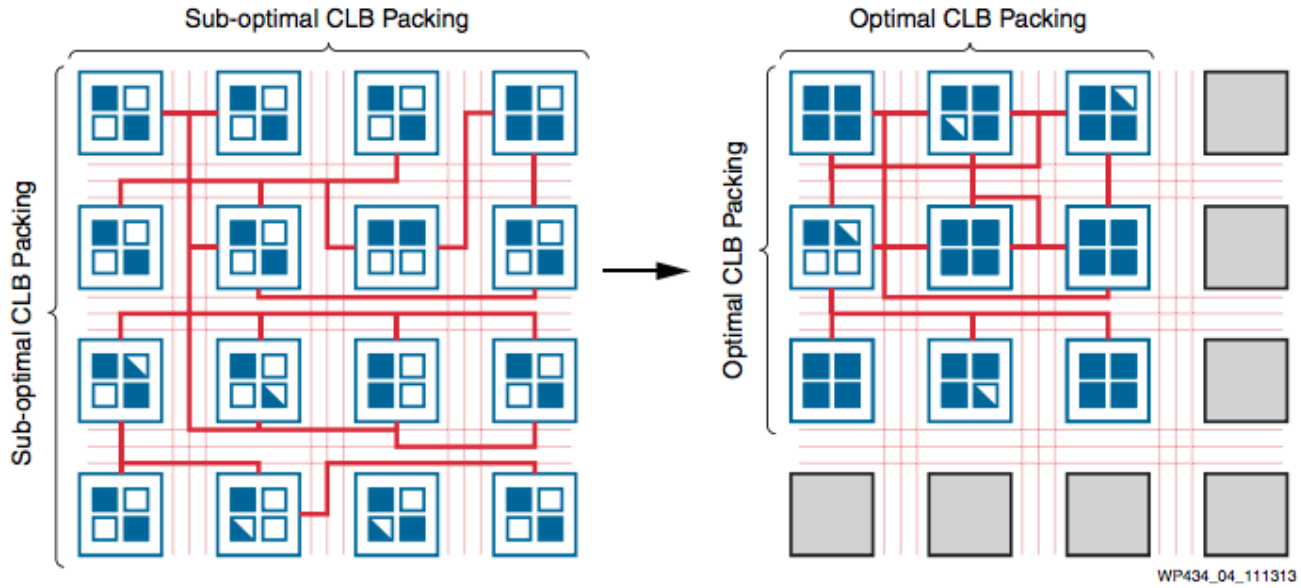


Figure 4: **Efficient Placement of Logic Resources**

28nm vs 20nm

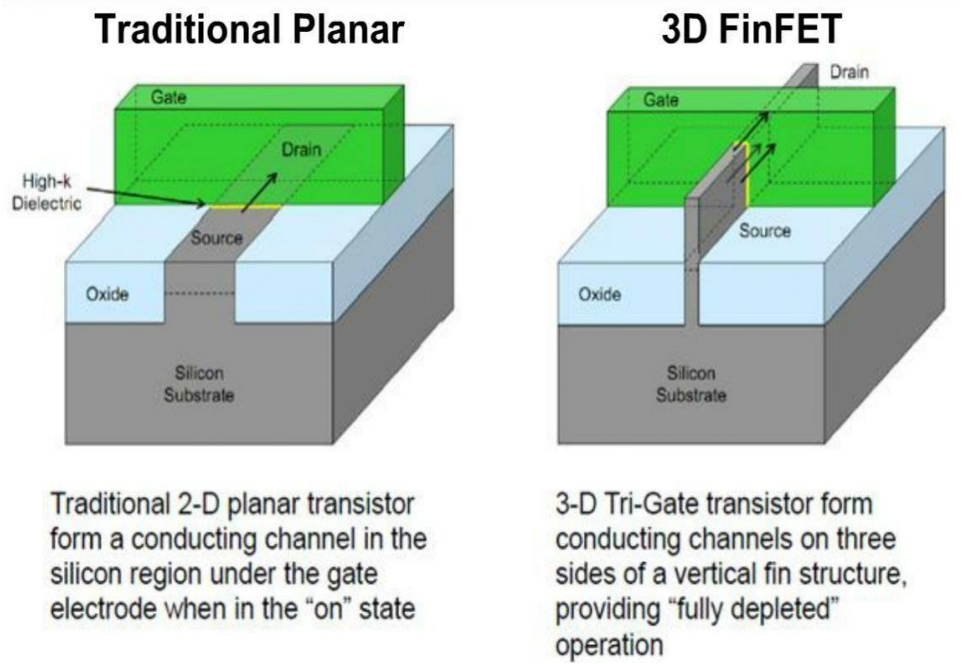
***Table 1:* 20 nm and 28 nm Devices Maximum Values**

Device Resources	Kintex-7	Kintex UltraScale	Virtex-7	Virtex UltraScale
Logic Cells / System Logic Cells	478	1,451	1,995	5,541
Block RAM (Mb)	34	76	68	133
DSP48	1,920	5,520	3,600	2,880
Peak DSP Performance (GMACs)	2,845	8,180	5,335	4,268
Transceiver Count	32	64	96	120
Peak Transceiver Line Rate (Gb/s)	12.5	16.3	28.05	30.5
Peak Transceiver Bandwidth (Gb/s)	800	2,086	2,784	5,616
PCI Express Blocks	1	6	4	6
100G Ethernet Blocks	–	2	–	9
150G Interlaken Blocks	–	2	–	9
Memory Interface Performance (Mb/s)	1,866	2,400	1,866	2,400
I/O Pins	500	832	1,200	1,456

Kintex UltraScale y Virtex UltraScale: Misma arquitectura (DSP, RAM, CLB, etc) pero diferente combinación de recursos

UltraScale+ | 16nm

- Compatible con arquitectura UltraScale, pero mejoras en performance/Watt
- 3D FinFET: menor consumo dinámico



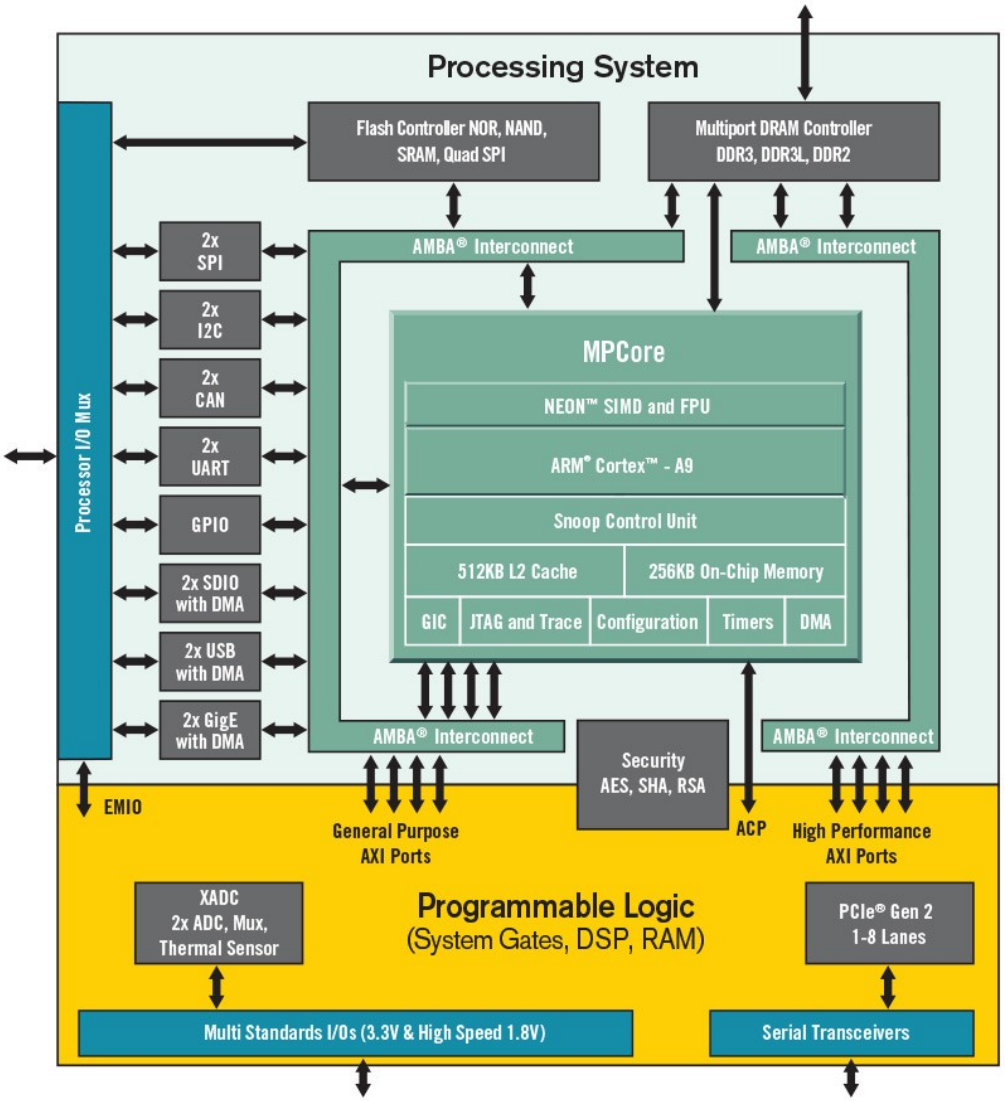
Traditional 2-D planar transistor form a conducting channel in the silicon region under the gate electrode when in the "on" state

3-D Tri-Gate transistor form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

ASIC - like

- ASIC-like clocking
- ASIC-like I/O Bandwidth

SoC


Processing System
Flash Controller NOR, NAND, SRAM, Quad SPI
Multiport DRAM Controller DDR3, DDR3L, DDR2
Processor I/O Mux
2x SPI
2x I2C
2x CAN
2x UART
GPIO
2x SDIO with DMA
2x USB with DMA
2x GigE with DMA
AMBA® Interconnect
AMBA® Interconnect
MPCore
NEON™ SIMD and FPU
ARM® Cortex™ - A9
Snoop Control Unit
512KB L2 Cache
256KB On-Chip Memory
GIC
JTAG and Trace
Configuration
Timers
DMA
AMBA® Interconnect
AMBA® Interconnect
Security AES, SHA, RSA
EMIO
General Purpose AXI Ports
ACP
High Performance AXI Ports
XADC 2x ADC, Mux, Thermal Sensor
Programmable Logic (System Gates, DSP, RAM)
PCIe® Gen 2 1-8 Lanes
Multi Standards I/Os (3.3V & High Speed 1.8V)
Serial Transceivers

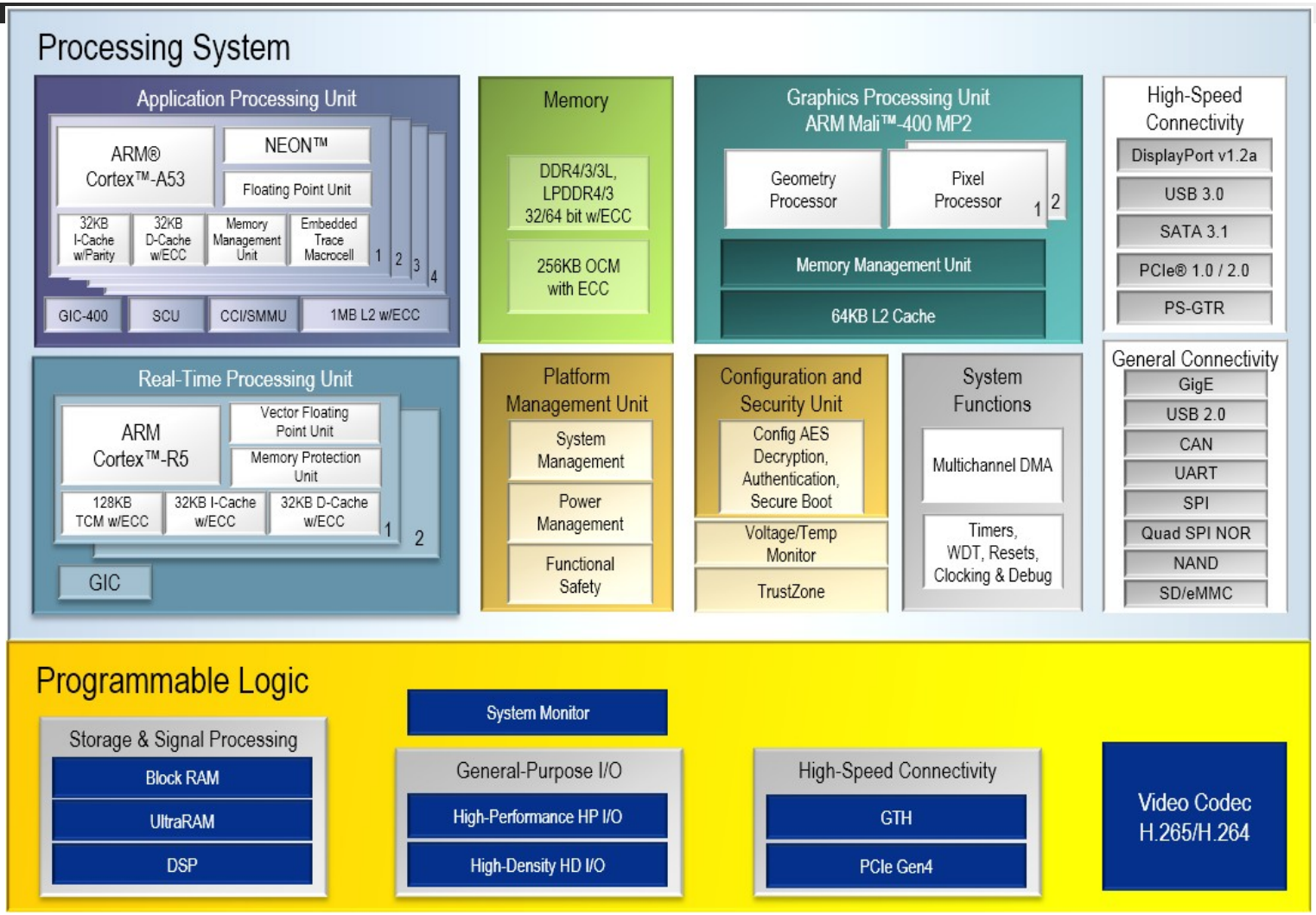
SoC | Opciones

Cost-Optimized	Mid-Range	High-End	High-End
ZYNQ	ZYNQ UltraSCALE+	ZYNQ UltraSCALE+	ZYNQ RFSoC
Zynq-7000 SoC Artix Devices Dual Arm® Cortex®-A9	Zynq UltraScale+ MPSoC CG Devices Dual Arm Cortex-A53 Dual Arm Cortex-R5	Zynq UltraScale+ MPSoC EV Devices Quad Arm Cortex-A53 Dual Cortex-R5 + GPU + Video Codec	Zynq UltraScale+ RFSoC with RF Data Converters Quad Arm Cortex-A53 Dual Cortex-R5
Zynq-7000S SoC Artix Devices Single Arm Cortex-A9	ZYNQ Zynq-7000 SoC Kintex Devices Dual Arm Cortex-A9	Zynq UltraScale+ MPSoC EG Devices Quad Arm Cortex-A53 Dual Cortex-R5 + GPU	Zynq UltraScale+ RFSoC with SD-FEC Cores Quad Arm Cortex-A53 Dual Arm Cortex-R5
			Zynq UltraScale+ RFSoC with RF Data Converters & SD-FEC Cores Quad Arm Cortex-A53 Dual Arm Cortex-R5

SoC Zynq (Cost-Optimized)

		Cost-Optimized Devices						Mid-Range Devices			
	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System (PS)	Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz			Dual-Core ARM Cortex-A9 MPCore Up to 1GHz[1]			
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor									
	L1 Cache	32KB Instruction, 32KB Data per processor									
	L2 Cache	512KB									
	On-Chip Memory	256KB									
	External Memory Support[2]	DDR3, DDR3L, DDR2, LPDDR2									
	External Static Memory Support[2]	2x Quad-SPI, NAND, NOR									
	DMA Channels	8 (4 dedicated to PL)									
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO									
	Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot									
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts									
Programmable Logic (PL)	7 Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex®-7	Kintex-7	Kintex-7	Kintex-7
	Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM	1.8Mb	2.5Mb	3.8Mb	2.1Mb	3.3Mb	4.9Mb	9.3Mb	17.6Mb	19.2Mb	26.5Mb
	(# 36Kb Blocks)	(50)	(72)	(107)	(60)	(95)	(140)	(265)	(500)	(545)	(755)
	DSP Slices	66	120	170	80	160	220	400	900	900	2,020
	PCI Express®	—	Gen2 x4	—	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC[2]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[3]	AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config									

SoC Zynq UltraSCALE+ (Mid-Range)



XCZU4EV-1SFVC784E USD 988 (2019), USD 1.276 (2022) @Digikey

Fuente información

https://www.xilinx.com/support/documentation/selection-guides/cost-optimized-product-selection-guide.pdf

https://www.xilinx.com/support/documentation/selection-guides/7-series-product-selection-guide.pdf

https://www.xilinx.com/support/documentation/selection-guides/zynq-7000-product-selection-guide.pdf

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https://www.xilinx.com/support/documentation/white_papers/wp434-ultrascale-smarter-systems.pdf

https://www.quora.com/What-are-FinFETs-and-will-they-ever-be-able-to-replace-MOSFETS