Equivalent circuit extraction for an SMA connector

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Abstract

A physical based method is used for estimating the equivalent circuit model of an SMA connector soldered on the top plane of a two layers board and connected to a single-end strip line. Starting from the Scattering parameters evaluated by using a 3-D full wave analysis based on a Finite Integration Technique, the equivalent circuit is extracted by modeling each part of the structure. The circuit is then validated by comparing the outputs obtained by a SPICE simulation of the circuit results with those computed by means of the full wave solution.

Introduction

At bitrates above one Gb/s the effects of boards' discontinuities on the integrity of the signals can not be neglected. For a correct design, the effects of parasitic, packaging, boards' materials and traces' geometries must be characterized and quantified. An essential step in this process of characterization is the measurement of the properties of the board in terms of scattering parameters (S-parameters), input impedance, noise voltage, etc. [1]. Microstrip and stripline structures can not be connected directly to the coaxial ports of a network analyzer (NA). The structure or device under test must be physically connected to the NA by some kind of transition network or fixture. One of the most frequently used fixture or connector for this kind of applications is the surface mounted adapter (SMA) [2]. Several techniques can be used to remove the effects of the adapter from the measurement. The technique that is best suited for a given application depends on the accuracy desired, the availability of calibration standards, the amount of time available. Among these techniques the de-embedding is a mathematical process that removes the effects of the adapter which are embedded in the measurements by subtracting out the S-parameters of an equivalent network that represents the fixture.
This paper proposes a SPICE-like equivalent circuit of an SMA. Each part of the circuit is related to one part of the connector and the values of the passive circuit elements are related to the SMA properties and dimensions. In the next SECTION the considered SMA and PCB configuration is introduced and a physical-based circuit is proposed. In SECTION III a full-wave simulation of the structure is performed by means of the Finite Integration Technique (FIT) and the computed S-parameters are compared with those obtained by the equivalent circuit; SECTION IV offers some conclusions. It is worthy to note that the development of an equivalent circuit for the SMA has the advantage of requiring less computational efforts for being solved than any three dimensional full wave model and its use avoids the performing of repeated NA calibrations [3-7].

Extraction of a physical based equivalent circuit

From an engineering point of view the interesting properties of an SMA connector, and hence, the equivalent circuit able to predict those properties, are those of an SMA mounted on a board and not simply isolated. Because of this it has been chosen to characterize an SMA connected to a short section of a stripline. This appendix (with different length, width, etc.) will be always present in any application.
The considered SMA connector has a nominal impedance $Z_{SMA} = 50\ \Omega$ and its relevant dimensions (taken by a commercial catalogue) are reported in Fig.1a. In order to characterize its electrical performances with the aim of obtaining an equivalent circuit of its behavior, the SMA is considered mounted on a simple three-layers boards as depicted in Fig. 1b. The central conductor of the SMA is soldered in a through hole via and connected to a 2 cm long stripline (among the two internal reference planes), with characteristic impedance $Z_c = 50\ \Omega$. The four lateral pins connect the external part of the SMA with the two reference planes. The topology of the proposed equivalent circuit is shown in Fig. 2.

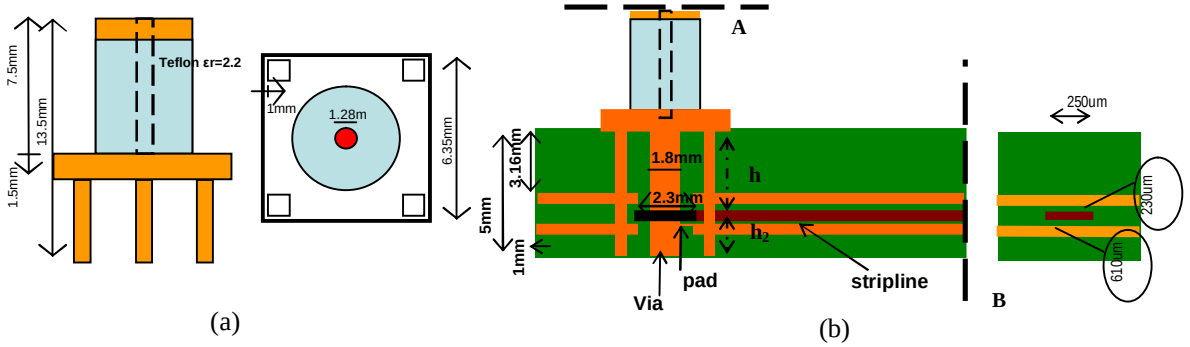

Figure 1. (a) Top and lateral view of the SMA connector with dimensions, (b) cross section of the board

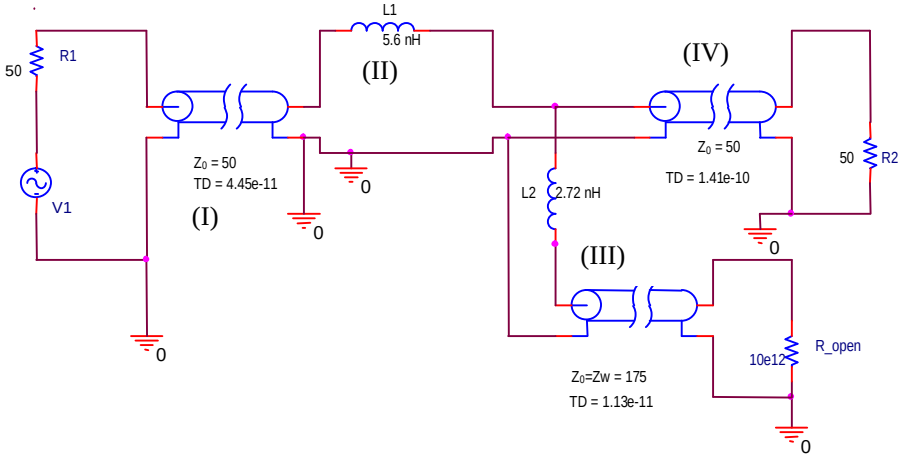

Figure 2. SPICE equivalent circuit for the structure in Fig. 1b.

The block labeled (I) is a lossless transmission line (TL) representing the upper external (with respect to the board) part of the SMA. Its characteristic impedance Z_0 is $Z_0 = Z_{SMA}$ and its flight time TD is

$$TD = \sqrt{\varepsilon_r}\,\frac{h}{c_0} \tag{1}$$

where ε_r is the electric permettivity of the dielectric filling the connector, h is the height of the SMA's external part, c_0 the speed of light. The block labeled (II) represents the inductance of the central pin from the top surface of the board to the stripline pad. At this point the electromagnetic energy, in form of voltage and current waves, is splitted in two parts: one flows along the stripline, the other continue through the via hole that act as an open-end TL. Block (III) represents the inductance of the remaining part of the via hole and its TL behavior. Because there is no clear reference conductor for this TL (vertically placed with respect to the reference planes) the characteristic impedance is taken equal to the wave impedance [8]

$$Z_w = \sqrt{\frac{\mu_0 \mu_r}{\varepsilon_0 \varepsilon_r}} \tag{2}$$

in which ε_r and μ_r are the relative effective permettivity and permeability respectively of the board's dielectric. The block (IV) represents the short stripline with $Z_0 = Z_c$ and TD as in (1).

Numerical Examples

The proposed circuit model for the SMA has been used to compute the S-parameters of the structure in Fig.1b and compare them with those evaluated by means of a three dimensional full wave simulation based on the Finite Integration Technique [9]. In this latter simulation the conductive parts of the PCB are considered as perfect electric conductors, the dielectric materials have ε_r = 2.2 (Teflon) for the

SMA connector and $\varepsilon_r = 4.5$ (FR4) for the board and are considered lossless, the computational domain is bounded by absorbing boundary conditions. Particular attention has been given to the excitation: the two "ports" at which the S-parameters are evaluated are the upper surface of the SMA (labeled as **A** in Fig. 1a) and the end of the stripline (labeled **B** in Fig. 1b). In order to ensure a TEM structure of the electromagnetic field (essential condition for a meaningful interpretation of the scattering matrix) lumped voltage sources are not suitable because they would excite higher order modes. Because of this the TEM excitation has been given by considering fictitious wave guide structures at planes **A** and **B** that cause a TEM structure of the field at these planes. Fig. 3 show the comparison between the S-parameters, in magnitude and phase, evaluated by the three dimensional FIT model and by the equivalent circuit through the SPICE solver. The agreement among the results shows the robustness of the proposed model. To obtain these results the inductances L_1 and L_2 in Fig. 3 are computed as

$$L_i = L' h_i \qquad i = 1,2 \tag{3}$$

where $L' = 1.7$ nH/m is in the range of the per unit length inductance of the via [2] and h_i is the length of the considered portion of the via.

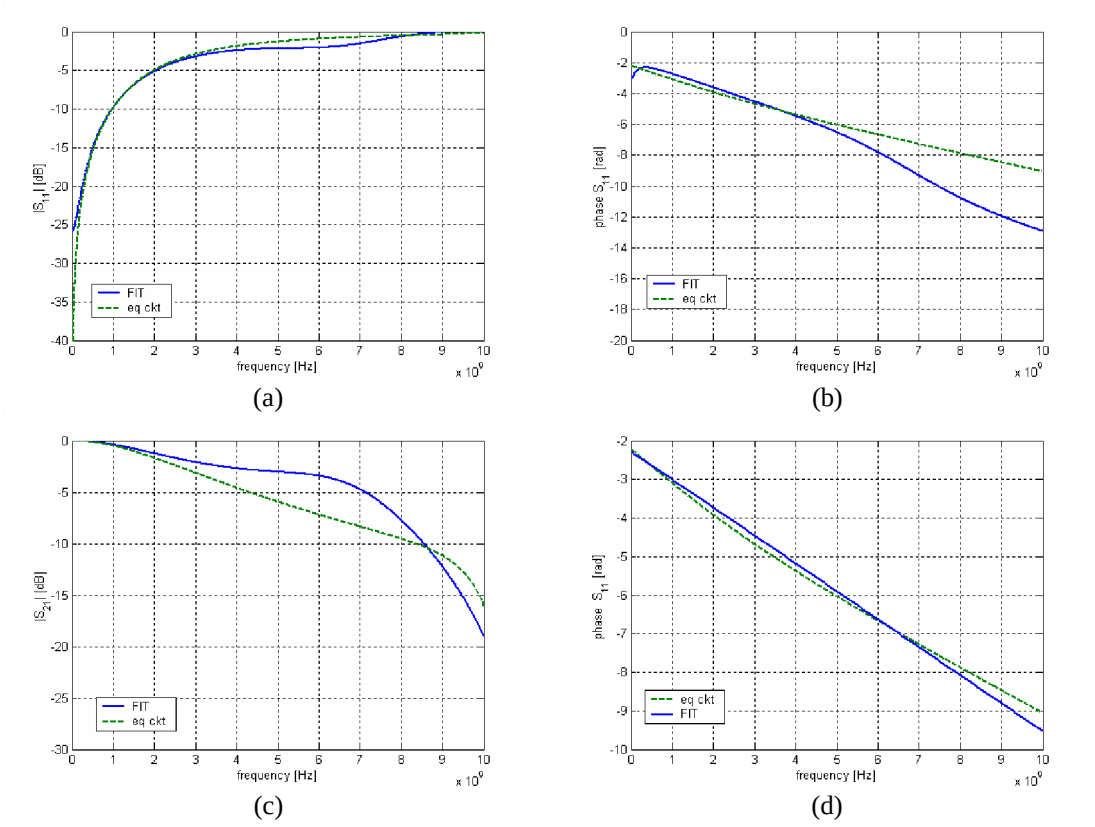

Figure 3. Comparison between S-parameters computed by FIT and by the equivalent circuit (eq. ckt.): (a), (b) S_{11} magnitude and phase, (c), (d) S_{21} magnitude and phase.

As a further example the S-parameters of the SMA connector are evaluated for the more complex stack-up represented in Fig. 4. The equivalent circuit model is the same proposed in Fig.2 with L_1 and L_2 calculated by using (3) and TD time equals to 7.9ps for the block labeled (III). Also in this case the agreement is satisfactory over the frequency range (Fig. 5).

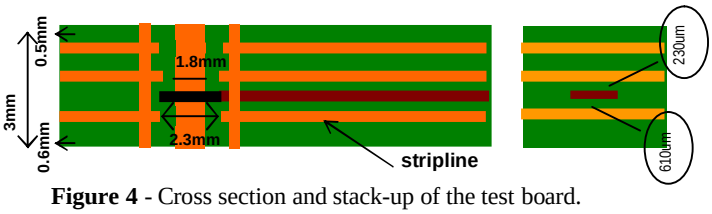

Figure 4 - Cross section and stack-up of the test board.

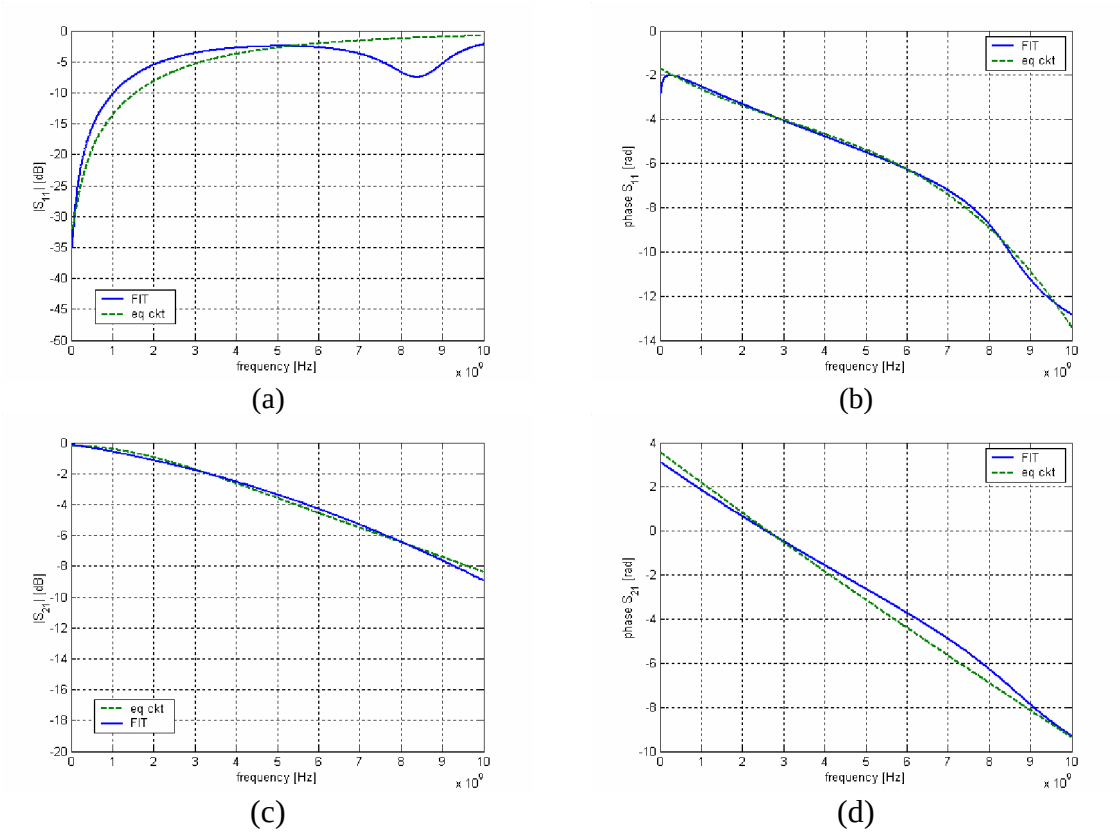

Figure 5 - Comparison between S-parameters computed by FIT and by the equivalent circuit (eq ckt): (a), (b) S_{11} magnitude and phase, (c), (d) S_{21} magnitude and phase.

Conclusions

This work presents a physical based equivalent circuit for a SMA connector. The global circuit is build up by single blocks strictly related to the geometry and physics of the device. Rules are given to quantify the circuit elements of each block. The results of a detailed full wave analysis are used as test for the equivalent circuit showing the reliability and robustness of the latter.

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