

Capítulos de libros:

- Interconnection Networks [Apéndice F de Computer Architecture - A quantitative approach]
- Arquitecturas VLIW & EPIC [Apéndice H de Computer Architecture - A quantitative approach]
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- Review de Arquitectura de Computadoras [Apéndice K de Computer Architecture - A quantitative approach]
- Warehouse Scale Computers [Capítulo 6 - Computer Architecture - A quantitative approach]
- Multithreading [Capítulo 7 - Modern Processor Design]
- Intel P6 Microarchitecture [Capítulo 11 - Modern Processor Design]

Artículos:

- Jenga: Software-Defined Cache Hierarchies, Po-An Tsai (MIT CSAIL), Nathan Beckmann (CMU SCS), Daniel Sanchez (MIT CSAIL) [2017]
- M. H. Lipasti, C. B. Wilkerson, and J. P. Shen, "Value locality and load value prediction," [1996]
- C3D: Mitigating the NUMA Bottleneck via Coherent DRAM Caches, Cheng-Chieh Huang (University of Edinburgh), Rakesh Kumar (University of Edinburgh), Marco Elver (University of Edinburgh), Boris Grot (University of Edinburgh), Vijay Nagarajan (University of Edinburgh) [2016]
- HARE: Hardware Accelerator for Regular Expressions, Vaibhav Gogte (University of Michigan), Aasheesh Kolli (University of Michigan), Michael J. Cafarella (University of Michigan), Loris D'Antoni (University of Wisconsin-Madison), Thomas F. Wenisch (University of Michigan) [2016]
- 90 (S) Jiajun Wang, Reena Panda and Lizy John. SeISMaP: A Selective Stride Masking Prefetching Scheme [2017]