Hojas de datos
Ciclos acceso a Memorias

- Hojas de datos de circuitos integrados
  - Maximum ratings, Operation conditions, DC characteristics.
  - AC characteristics:
    - Requerimientos (p. ej. tiempos de setup y hold)
    - Switching characteristics (p. ej. Retardos)

- Requerimientos y retardos en memorias
  - Cicos lectura y escritura

Hojas de datos

- Absolute Maximum Ratings
  - Niveles (tensión, corriente, temp.) que si se exceden dañan el chip.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	– 0.3 to 7.0	V
V_{IN}	Input Voltage	– 0.3* to 7.0	V
$V_{I/O}$	Input/Output Voltage	– 0.5* to V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6 **	W
Tsolder	Soldering Temperature (10 s)	260	°C
Tstrg	Storage Temperature	– 55 to 150	°C
Topr	Operating Temperature	0 to 70	°C

* – 3.0 V when measured at a pulse width of 50 ns
** SOP

Hojas de datos

- Recommended Operating Conditions
  - Condiciones dentro de las cuales el fabricante garantiza que el dispositivo funciona de acuerdo a lo especificado.
  - Deben ser respetadas por el ambiente y el circuito externo.

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	– 0.3*	–	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* – 3.0 V when measured at a pulse width of 50 ns

Hojas de datos

- Electrical Characteristics o DC Characteristics
  - Niveles dentro de los que se mantienen las tensiones y corrientes del chip si se respetan las condiciones de operación recomendadas.

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		-0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA	3.5		V

Hojas de datos

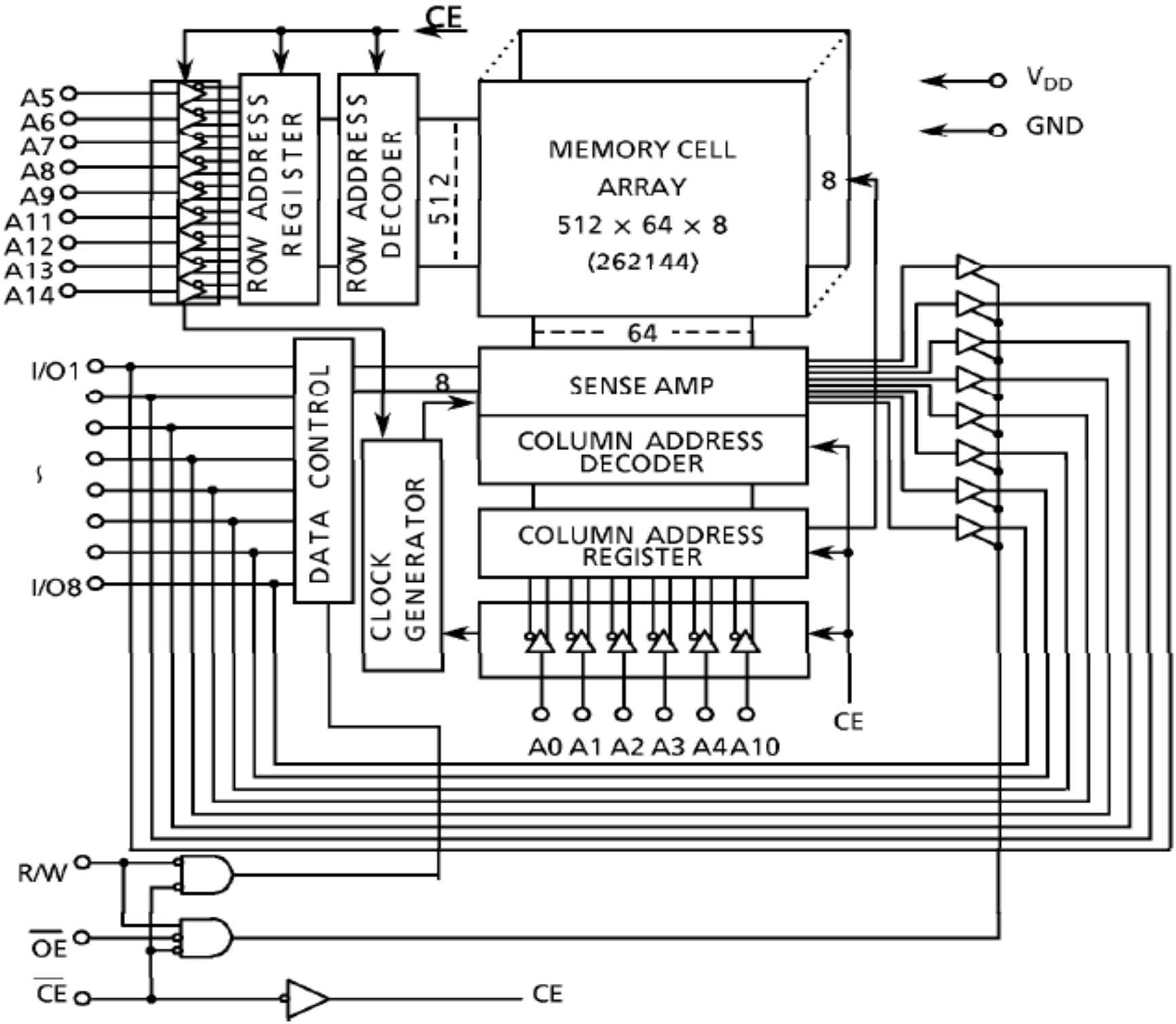
- AC Characteristics
  - Todo lo que tiene que ver con temporización, clasificado en dos categorías
  - Timing Requirements
    - Condiciones que deben ser respetadas por el circuito externo para que el chip funcione como se espera
    - P. ej. tiempo de setup en una entrada.
  - Switching Characteristics
    - Qué tan rápido responden las salidas del chip a cambios en las entradas.
    - Suponiendo que se respetan los requerimientos de tiempo y las condiciones de operación recomendadas.

Referencias

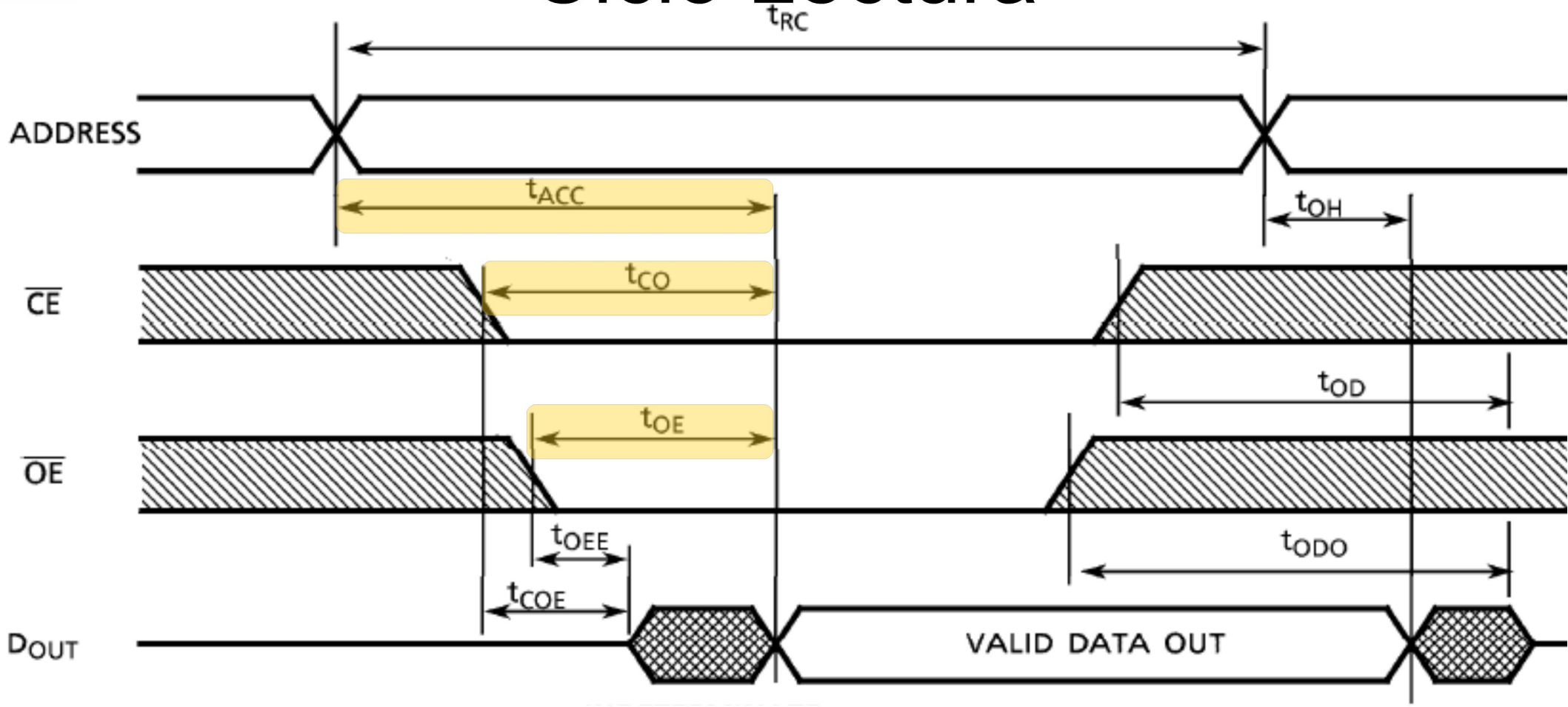
- Stephen M. Nolan and Jose M. Soltero, “Understanding and Interpreting Standard-Logic Data Sheets”, Application Report SZZA036B, Texas Instruments, May 2003.
  - ABSTRACT: Texas Instruments (TI) standard-logic products data sheets include descriptions of functionality and electrical specifications for the devices. Each specification includes acronyms, numerical limits, and test conditions that may be foreign to the user. The proper understanding and interpretation of the direct, and sometimes implied, meanings of these specifications is essential to correct product selection and associated circuit design. This application report explains each data-sheet parameter in detail, how it affects the device, and, more important, how it impacts the application. This will enable component and system-design engineers to derive the maximum benefit from TI logic devices.
  - http://www.ti.com/lit/an/szza036b/szza036b.pdf

Requerimientos y retardos en Memorias

- Ciclo lectura
  - Address, /CS, /OE → Dout: valor seleccionado
- Ciclo escritura
  - Address, Din, /CS, /WE → memoriza Din


CE
A5
A6
A7
A8
A9
A11
A12
A13
A14
ROW ADDRESS REGISTER
ROW ADDRESS DECODER
512
MEMORY CELL ARRAY
512 × 64 × 8
(262144)
8
VDD
GND
64
I/O1
I/O8
DATA CONTROL
8
SENSE AMP
COLUMN ADDRESS DECODER
CLOCK GENERATOR
COLUMN ADDRESS REGISTER
CE
A0 A1 A2 A3 A4 A10
R/W
OE
CE
CE

Ciclo Lectura



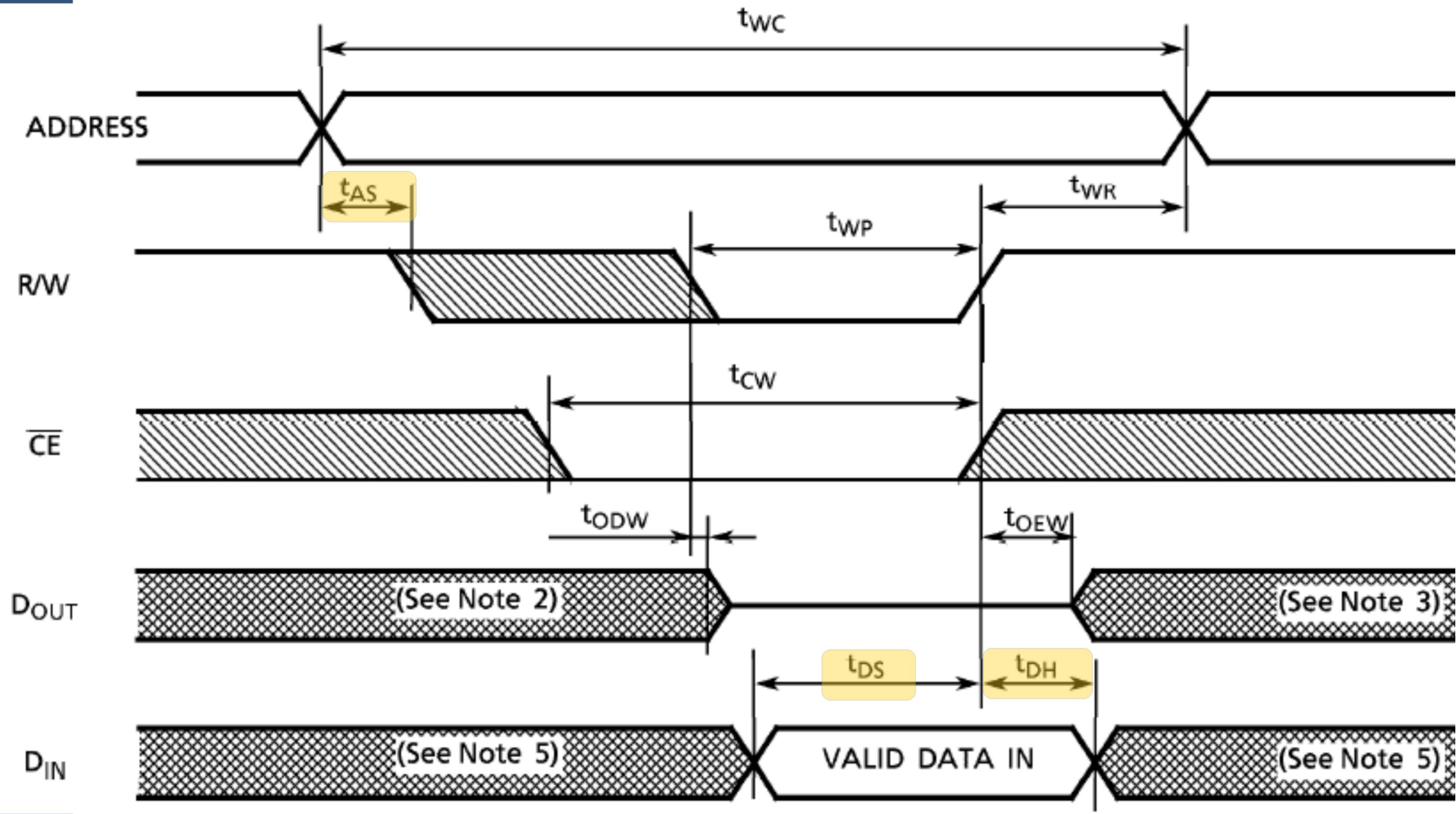
SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL/DTRL					
		-55L		-70L		-85L	
		MIN	MAX	MIN	MAX	MIN	MAX
t_{RC}	Read Cycle Time	55	–	70	–	85	–
t_{ACC}	Address Access Time	–	55	–	70	–	85
t_{CO}	Chip Enable Access Time	–	55	–	70	–	85
t_{OE}	Output Enable Access Time	–	30	–	35	–	45

Ciclo de Lectura

READ CYCLE

SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL/DTRL						UNIT
		-55L		-70L		-85L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	55	–	70	–	85	–	ns
t_{ACC}	Address Access Time	–	55	–	70	–	85	
t_{CO}	Chip Enable Access Time	–	55	–	70	–	85	
t_{OE}	Output Enable Access Time	–	30	–	35	–	45	
t_{COE}	Chip Enable Low to Output Active	10	–	10	–	10	–	
t_{OEE}	Output Enable Low to Output Active	5	–	5	–	5	–	
t_{OD}	Chip Enable High to Output High-Z	–	20	–	25	–	30	
t_{ODO}	Output Enable High to Output High-Z	–	20	–	25	–	30	
t_{OH}	Output Data Hold Time	10	–	10	–	10	–	

Ciclo Escritura



t_{DS}	Data Setup Time	25	–	30	–	40	–
t_{DH}	Data Hold Time	0	–	0	–	0	–

Ciclo de escritura

WRITE CYCLE

SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL/DTRL						UNIT
		-55L		-70L		-85L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	55	–	70	–	85	–	ns
t_{WP}	Write Pulse Width	45	–	50	–	60	–	
t_{CW}	Chip Enable to End of Write	50	–	60	–	65	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{ODW}	R/W Low to Output High-Z	–	20	–	25	–	30	
t_{OEW}	R/W High to Output Active	5	–	5	–	5	–	
t_{DS}	Data Setup Time	25	–	30	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

AC TEST CONDITIONS

Output load: 30 pF + one TTL gate (-55L)
100 pF + one TTL gate (-70L, -85L)
Input pulse level: 0.6 V, 2.4 V
Timing measurements: 1.5 V
Reference level: 1.5 V
t_R, t_F: 5 ns