# Práctica N° 1
# Convertidor Flyback
# Instructivo

## 1 Objetivos:

- Analizar el funcionamiento de un convertidor DC-DC aislado.
- Comprender cómo afecta al funcionamiento del convertidor la inductancia de fugas del transformador. Aprender a simular esta no idealidad.
- Comprender qué variables afectan y cómo a la tensión de salida y al modo de funcionamiento del convertidor.

## 2 Materiales:

- Planta física del convertidor
- Fuente de alimentación
- Osciloscopio
- Punta de osciloscopio de efecto hall y su amplificador asociado.
- Voltímetro

Software de simulación: Spice (LTSpice o NgSpice, por ejemplo)

## 3 Descripción de la planta física:

La planta física se representa en la Figura 1:

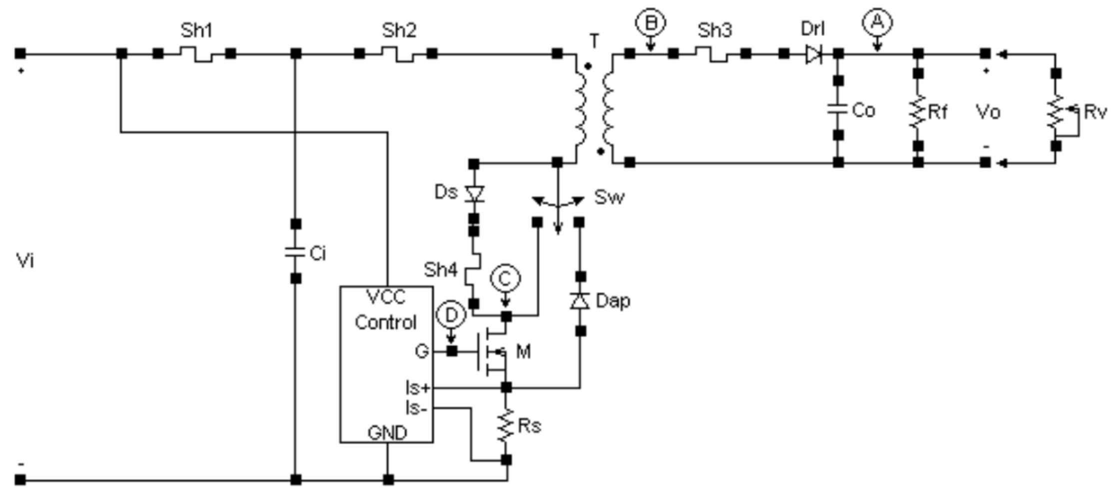



Figura 1

Donde:

Vi: fuente de alimentación continua, 12.5V.
Ci: condensador de entrada.
M: MOSFET IRF640, del cual se adjuntan las hojas de datos.

T: transformador con núcleo de ferrita, n=1, L=40μHy.
Control: bloque de comando. Basado en el circuito integrado TL494, del cual se adjuntan las hojas de datos.
Rf: resistencia de carga fija, 470Ω.
Rv: resistencia de carga variable. ( 0..60Ω)
Rs: resistencia de sensado de la corriente.
Drl: diodo BY229-600, del cual se adjuntan hojas de datos.
Ds: diodo serie, BY229-600.
Dap, diodo antiparalelo, BY229-600.
Sw, llave de bypass de los diodos Ds y Dap.
Co, capacitor de salida, 10μF
$Sh_1$, $Sh_2$, $Sh_3$, $Sh_4$, puntos para medición de corriente con punta hall.
A, B, C, D, puntos para medición de tensión.

Nota: se llamará Ro el paralelo de Rv y Rf.

La Figura 2 es un esquemático simplificado del bloque de control, donde Ct=1000pF, Rt=10K, y E, F, G y H son puntos para medición de tensión.

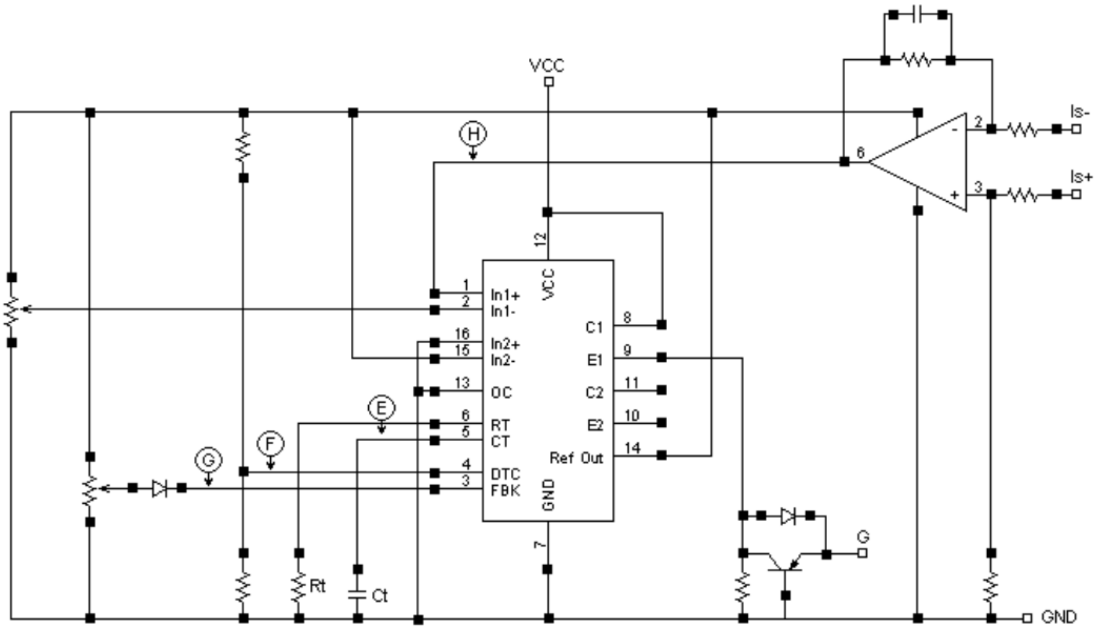



Figura 2

La Figura 3 muestra la ubicación de los distintos componente en la placa.

## 4 Desarrollo de la práctica:

Al llegar al laboratorio, el estudiante debe conocer el funcionamiento del convertidor, la distinción entre los modos de conducción continua y discontinua y el funcionamiento a grandes rasgos del TL494. Influencia de la inductancia de fugas del transformador en el comportamiento del convertidor.

## 4.1 Preinforme.

a – Hallar en forma teórica la ecuación que fija el voltaje de salida del convertidor en conducción continua y discontinua.

b – Hallar la ecuación que determina el valor de la carga que hace pasar al convertidor de funcionamiento en conducción continua a discontinua. Calcular la resistencia crítica. ¿De que otras formas es posible variar el modo de funcionamiento del convertidor?

c – Simular el circuito de potencia con Ro=470Ω. ¿En que modo de funcionamiento se encuentra el convertidor?. Presentar las formas de onda de la corriente por el MOSFET (Ids), por el diodo Drl (Id), la tensión sobre los mismos (Vds y Vd), y la tensión en la salida del convertidor (Vo). Verificar si las tensiones y corrientes máximas coinciden con las calculadas y si el comportamiento es el esperado teóricamente.

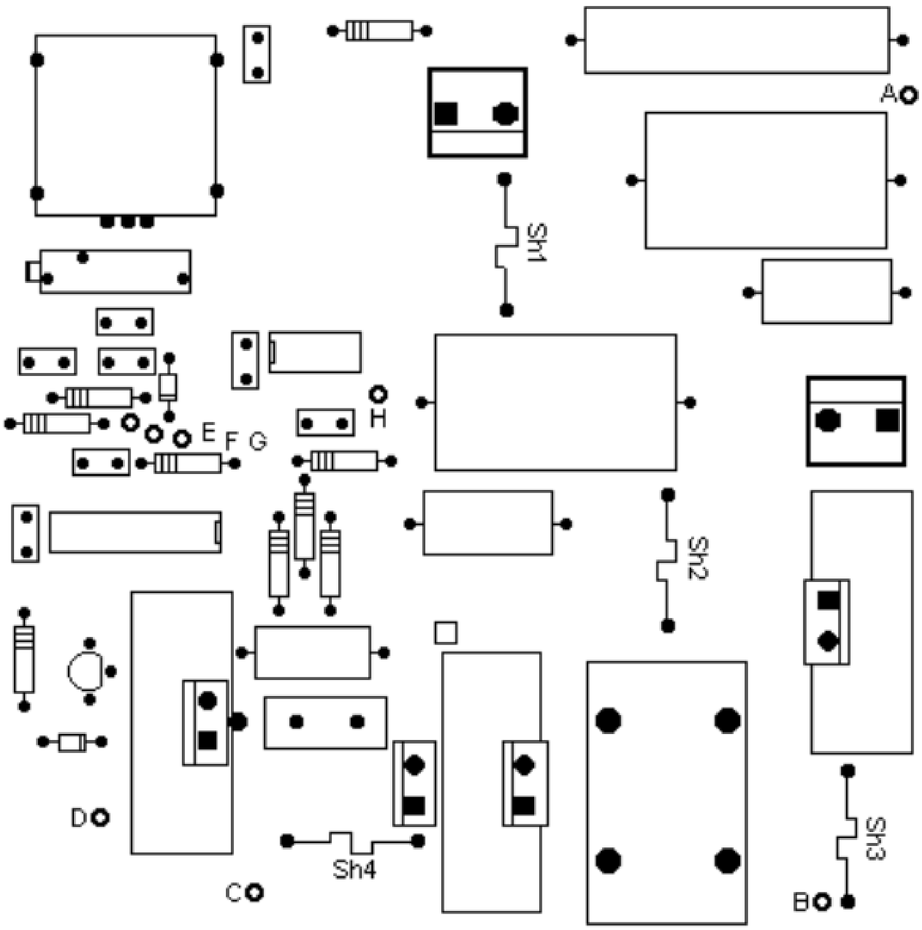



Figura 3

d – Simular el circuito en el umbral de conducción continua. Presentar las formas de onda simuladas de Ids, Vds, Id, Vd y Vo. Verificar con los cálculos teóricos.

e – Considerar la influencia de las inductancias de fugas del transformador. Volver a simular el circuito de la parte c, considerando que la inductancia de las fugas es el 5 % de la magnetizante. Observar como varían Ids, Vds, Id y Vd.

f – En modo de conducción discontinua, analizar qué consecuencias puede traer la recuperación inversa del diodo Drl. Dibuje la corriente por el MOSFET y por Drl.

g – Realizar un plan de medidas, con las señales a observar en el osciloscopio y los puntos de medida a utilizar.

*Notas*:

1. Adjuntar al preinforme los archivos simulados.
2. Para todas las simulaciones se ignorarán los diodos serie y antiparalelo del MOSFET.
3. Para las simulaciones se utilizará un ciclo de trabajo del 50%. Se empleará como modelo del MOSFET y del diodo Drl a los disponibles en la web del curso.
4. Para simular el transformador pueden utilizarse dos enfoques:
   - Representar el circuito de salida en el primario.
   - Modelarlo por dos inductancias acopladas con un coeficiente k, así:

| | | | |
|---|---|---|---|
| Lp | Nodo_p1 | Nodo_p2 | Valor |
| Ls | Nodo_s1 | Nodo_s2 | Valor |
| Kps | Lp | Ls | k |

   Si k=1 el acoplamiento es perfecto.
   El primer nodo de los inductores identifica el comienzo del arrollamiento.
   Recordar que para la simulación los circuitos primario y secundario deben estar conectados.

## 4.2 Laboratorio.

Precaución: la temperatura alcanzada por los elementos resistivos puede ser elevada.

Observar el circuito e identificar sus partes.

**Comportamiento del circuito**

Colocar la llave de bypass de forma que los diodos Ds y Dap queden en funcionamiento. Colocar en funcionamiento el circuito en la configuración de la parte *c*. Medir la frecuencia y verificar que el ciclo de trabajo del MOSFET sea el adecuado.
Medir las tensiones de entrada y salida del flyback. Relevar las formas de onda simuladas.

**Efecto de los diodos Ds y Dap**

Coloque la llave de bypass de modo de eliminar los diodos Ds y Dap. Observe la corriente por el primario y en el diodo del secundario. Aprecie el transitorio de

apagado del diodo del secundario. ¿Como se ve reflejado dicho transitorio en el primario?
Colocar nuevamente la llave de bypass de modo que los diodo Ds y Dap queden en funcionamiento. Observe la tensión en el MOSFET y las corrientes por los diodos Ds y Dap. Relevar las formas de onda de interés

**Pérdidas en el MOSFET**

Cargue el circuito con Ro=50Ω. Tome los datos necesarios como para calcular las pérdidas en el MOSFET.

**Efecto de la variación de la carga**

Varíe la carga del convertidor, relevando la forma de onda de las corrientes por el primario y por el secundario, y la tensión del Gate, de forma de visualizar el cambio de comportamiento entre los modos de conducción continua y discontinua. Mida las tensiones de entrada y salida del convertidor, así como la carga aplicada para las distintas situaciones.

**Efecto de la variación del ciclo de trabajo**

Vuelva a cargar el circuito con Ro=50 Ω. Observe las corrientes por el primario y por el secundario. Varíe el punto de funcionamiento del circuito de forma de visualizar el cambio de comportamiento entre ambos modos.

## 4.3 Informe.

1. Analizar y comparar las formas de onda relevadas en el laboratorio con los resultados obtenidos en las simulaciones.
2. ¿Qué utilidad tienen el diodo en serie y el en antiparalelo con el MOSFET?. Justifique.
3. Calcule las pérdidas del MOSFET con Ro=50Ω
4. Analice las medidas realizadas al variar la carga y la transferencia del convertidor.
5. Analice las formas de ondas obtenidas al variar el ciclo de trabajo.
6. Resumen

Notas:
1. En todos los casos se verificarán los valores calculados en el preinforme y de ser necesario se recalcularán de acuerdo a los datos medidos durante la práctica.
2. Respecto al resumen solicitado en el punto 6 del informe, el mismo deberá enumerar y describir someramente las enseñanzas y conceptos aprendidos. El mismo será de aproximadamente 300 palabras.

Order this document by TL494/D

MOTOROLA

# TL494

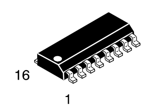
# SWITCHMODE™ Pulse Width Modulation Control Circuit

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for SWITCHMODE power supply control.

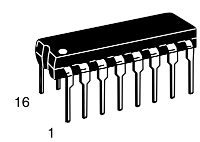
- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push–Pull or Single–Ended Operation
- Undervoltage Lockout

**SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT**

**SEMICONDUCTOR TECHNICAL DATA**

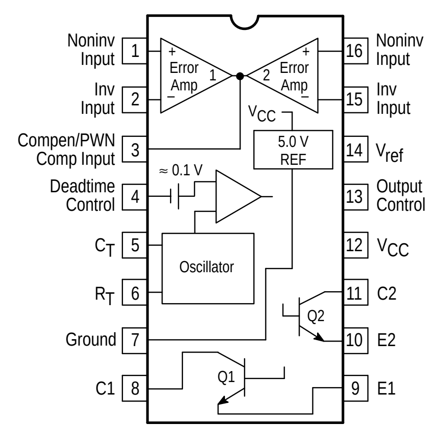



**D SUFFIX**
PLASTIC PACKAGE
CASE 751B
(SO–16)




**N SUFFIX**
PLASTIC PACKAGE
CASE 648

**PIN CONNECTIONS**




(Top View)

**MAXIMUM RATINGS** (Full operating ambient temperature range applies, unless otherwise noted.)

| Rating | Symbol | TL494C | TL494I | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 42 | | V |
| Collector Output Voltage | $V_{C1}$, $V_{C2}$ | 42 | | V |
| Collector Output Current (Each transistor) (Note 1) | $I_{C1}$, $I_{C2}$ | 500 | | mA |
| Amplifier Input Voltage Range | $V_{IR}$ | –0.3 to +42 | | V |
| Power Dissipation @ $T_A \le 45°C$ | $P_D$ | 1000 | | mW |
| Thermal Resistance, Junction–to–Ambient | $R_{\theta JA}$ | 80 | | °C/W |
| Operating Junction Temperature | $T_J$ | 125 | | °C |
| Storage Temperature Range | $T_{stg}$ | –55 to +125 | | °C |
| Operating Ambient Temperature Range<br>TL494C<br>TL494I | $T_A$ | <br>0 to +70<br>–25 to +85 | | °C |
| Derating Ambient Temperature | $T_A$ | 45 | | °C |

**NOTE:** 1. Maximum thermal limits must be observed.

## ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
|---|---|---|
| TL494CD | $T_A$ = 0° to +70°C | SO–16 |
| TL494CN | | Plastic |
| TL494IN | $T_A$ = – 25° to +85°C | Plastic |

## RECOMMENDED OPERATING CONDITIONS

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 7.0 | 15 | 40 | V |
| Collector Output Voltage | $V_{C1}$, $V_{C2}$ | – | 30 | 40 | V |
| Collector Output Current (Each transistor) | $I_{C1}$, $I_{C2}$ | – | – | 200 | mA |
| Amplified Input Voltage | $V_{in}$ | –0.3 | – | $V_{CC}$ – 2.0 | V |
| Current Into Feedback Terminal | $I_{fb}$ | – | – | 0.3 | mA |
| Reference Output Current | $I_{ref}$ | – | – | 10 | mA |
| Timing Resistor | $R_T$ | 1.8 | 30 | 500 | kΩ |
| Timing Capacitor | $C_T$ | 0.0047 | 0.001 | 10 | μF |
| Oscillator Frequency | $f_{osc}$ | 1.0 | 40 | 200 | kHz |

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 15 V, $C_T$ = 0.01 μF, $R_T$ = 12 kΩ, unless otherwise noted.)

For typical values $T_A$ = 25°C, for min/max values $T_A$ is the operating ambient temperature range that applies, unless otherwise noted.

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **REFERENCE SECTION** | | | | | |
| Reference Voltage ($I_O$ = 1.0 mA) | $V_{ref}$ | 4.75 | 5.0 | 5.25 | V |
| Line Regulation ($V_{CC}$ = 7.0 V to 40 V) | $Reg_{line}$ | – | 2.0 | 25 | mV |
| Load Regulation ($I_O$ = 1.0 mA to 10 mA) | $Reg_{load}$ | – | 3.0 | 15 | mV |
| Short Circuit Output Current ($V_{ref}$ = 0 V) | $I_{SC}$ | 15 | 35 | 75 | mA |
| **OUTPUT SECTION** | | | | | |
| Collector Off–State Current ($V_{CC}$ = 40 V, $V_{CE}$ = 40 V) | $I_{C(off)}$ | – | 2.0 | 100 | μA |
| Emitter Off–State Current $V_{CC}$ = 40 V, $V_C$ = 40 V, $V_E$ = 0 V) | $I_{E(off)}$ | – | – | –100 | μA |
| Collector–Emitter Saturation Voltage (Note 2) | | | | | V |
| Common–Emitter ($V_E$ = 0 V, $I_C$ = 200 mA) | $V_{sat(C)}$ | – | 1.1 | 1.3 | |
| Emitter–Follower ($V_C$ = 15 V, $I_E$ = –200 mA) | $V_{sat(E)}$ | – | 1.5 | 2.5 | |
| Output Control Pin Current | | | | | |
| Low State ($V_{OC}$ ≤ 0.4 V) | $I_{OCL}$ | – | 10 | – | μA |
| High State ($V_{OC}$ = $V_{ref}$) | $I_{OCH}$ | – | 0.2 | 3.5 | mA |
| Output Voltage Rise Time | $t_r$ | | | | ns |
| Common–Emitter (See Figure 12) | | – | 100 | 200 | |
| Emitter–Follower (See Figure 13) | | – | 100 | 200 | |
| Output Voltage Fall Time | $t_f$ | | | | ns |
| Common–Emitter (See Figure 12) | | – | 25 | 100 | |
| Emitter–Follower (See Figure 13) | | – | 40 | 100 | |

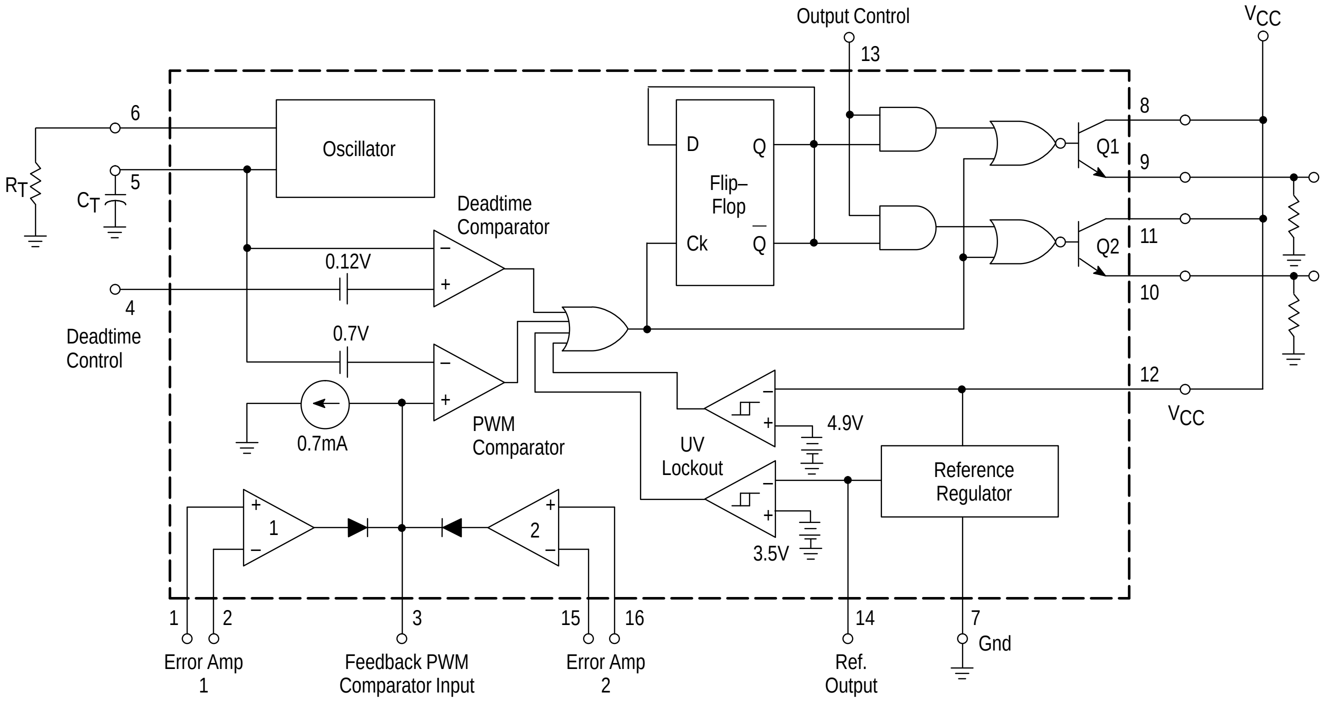
**NOTE:** 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $C_T$ = 0.01 µF, $R_T$ = 12 kΩ, unless otherwise noted.)
For typical values $T_A$ = 25°C, for min/max values $T_A$ is the operating ambient temperature range that applies, unless otherwise noted.

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **ERROR AMPLIFIER SECTION** | | | | | |
| Input Offset Voltage ($V_{O\ (Pin\ 3)}$ = 2.5 V) | $V_{IO}$ | – | 2.0 | 10 | mV |
| Input Offset Current ($V_{O\ (Pin\ 3)}$ = 2.5 V) | $I_{IO}$ | – | 5.0 | 250 | nA |
| Input Bias Current ($V_{O\ (Pin\ 3)}$ = 2.5 V) | $I_{IB}$ | – | –0.1 | –1.0 | µA |
| Input Common Mode Voltage Range ($V_{CC}$ = 40 V, $T_A$ = 25°C) | $V_{ICR}$ | –0.3 to $V_{CC}$–2.0 | | | V |
| Open Loop Voltage Gain ($\Delta V_O$ = 3.0 V, $V_O$ = 0.5 V to 3.5 V, $R_L$ = 2.0 kΩ) | $A_{VOL}$ | 70 | 95 | – | dB |
| Unity–Gain Crossover Frequency ($V_O$ = 0.5 V to 3.5 V, $R_L$ = 2.0 kΩ) | $f_{C-}$ | – | 350 | – | kHz |
| Phase Margin at Unity–Gain ($V_O$ = 0.5 V to 3.5 V, $R_L$ = 2.0 kΩ) | $\phi_m$ | – | 65 | – | deg. |
| Common Mode Rejection Ratio ($V_{CC}$ = 40 V) | CMRR | 65 | 90 | – | dB |
| Power Supply Rejection Ratio ($\Delta V_{CC}$ = 33 V, $V_O$ = 2.5 V, $R_L$ = 2.0 kΩ) | PSRR | – | 100 | – | dB |
| Output Sink Current ($V_{O\ (Pin\ 3)}$ = 0.7 V) | $I_{O-}$ | 0.3 | 0.7 | – | mA |
| Output Source Current ($V_{O\ (Pin\ 3)}$ = 3.5 V) | $I_{O+}$ | 2.0 | –4.0 | – | mA |
| **PWM COMPARATOR SECTION** (Test Circuit Figure 11) | | | | | |
| Input Threshold Voltage (Zero Duty Cycle) | $V_{TH}$ | – | 2.5 | 4.5 | V |
| Input Sink Current ($V_{(Pin\ 3)}$ = 0.7 V) | $I_{I-}$ | 0.3 | 0.7 | – | mA |
| **DEADTIME CONTROL SECTION** (Test Circuit Figure 11) | | | | | |
| Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 V to 5.25 V) | $I_{IB\ (DT)}$ | – | –2.0 | –10 | µA |
| Maximum Duty Cycle, Each Output, Push–Pull Mode<br>($V_{Pin\ 4}$ = 0 V, $C_T$ = 0.01 µF, $R_T$ = 12 kΩ)<br>($V_{Pin\ 4}$ = 0 V, $C_T$ = 0.001 µF, $R_T$ = 30 kΩ) | $DC_{max}$ | <br>45<br>– | <br>48<br>45 | <br>50<br>50 | % |
| Input Threshold Voltage (Pin 4)<br>(Zero Duty Cycle)<br>(Maximum Duty Cycle) | $V_{th}$ | <br>–<br>0 | <br>2.8<br>– | <br>3.3<br>– | V |
| **OSCILLATOR SECTION** | | | | | |
| Frequency ($C_T$ = 0.001 µF, $R_T$ = 30 kΩ) | $f_{osc}$ | – | 40 | – | kHz |
| Standard Deviation of Frequency* ($C_T$ = 0.001 µF, $R_T$ = 30 kΩ) | $\sigma f_{osc}$ | – | 3.0 | – | % |
| Frequency Change with Voltage ($V_{CC}$ = 7.0 V to 40 V, $T_A$ = 25°C) | $\Delta f_{osc}$ ($\Delta V$) | – | 0.1 | – | % |
| Frequency Change with Temperature ($\Delta T_A$ = $T_{low}$ to $T_{high}$)<br>($C_T$ = 0.01 µF, $R_T$ = 12 kΩ) | $\Delta f_{osc}$ ($\Delta T$) | – | – | 12 | % |
| **UNDERVOLTAGE LOCKOUT SECTION** | | | | | |
| Turn–On Threshold ($V_{CC}$ increasing, $I_{ref}$ = 1.0 mA) | $V_{th}$ | 5.5 | 6.43 | 7.0 | V |
| **TOTAL DEVICE** | | | | | |
| Standby Supply Current (Pin 6 at $V_{ref}$, All other inputs and outputs open)<br>($V_{CC}$ = 15 V)<br>($V_{CC}$ = 40 V) | $I_{CC}$ | <br>–<br>– | <br>5.5<br>7.0 | <br>10<br>15 | mA |
| Average Supply Current<br>($C_T$ = 0.01 µF, $R_T$ = 12 kΩ, $V_{(Pin\ 4)}$ = 2.0 V)<br>($V_{CC}$ = 15 V) (See Figure 12) | | – | 7.0 | – | mA |

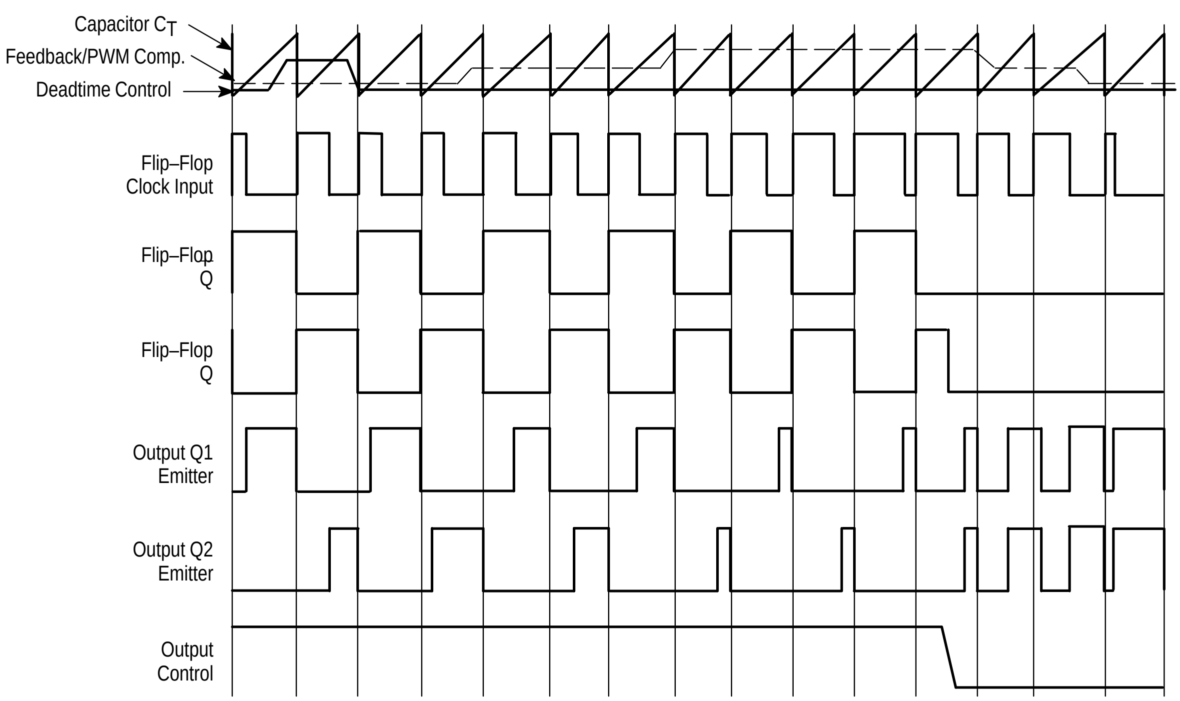
* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}$

**Figure 1. Representative Block Diagram**




This device contains 46 active transistors.

**Figure 2. Timing Diagram**



## APPLICATIONS INFORMATION

### Description

The TL494 is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal–linear sawtooth oscillator is frequency–programmable by two external components, $R_T$ and $C_T$. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor $C_T$ to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip–flop clock–input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime–control input to a fixed voltage, ranging between 0 V to 3.3 V.

**Functional Table**

| Input/Output Controls | Output Function | $\frac{f_{out}}{f_{osc}}$ = |
|---|---|---|
| Grounded | Single–ended PWM @ Q1 and Q2 | 1.0 |
| @ $V_{ref}$ | Push–pull Operation | 0.5 |

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on–time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from –0.3 V to ($V_{CC}$ – 2V), and may be used to sense power–supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor $C_T$ is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse–steering flip–flop and inhibits the output transistors, Q1 and Q2. With the output–control connected to the reference line, the pulse–steering flip–flop directs the modulated pulses to each of the two output transistors alternately for push–pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single–ended operation with a maximum on–time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output–drive currents are required for single–ended operation, Q1 and Q2 may be connected in parallel, and the output–mode pin must be tied to ground to disable the flip–flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±5.0% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.

**Figure 3. Oscillator Frequency versus Timing Resistance**

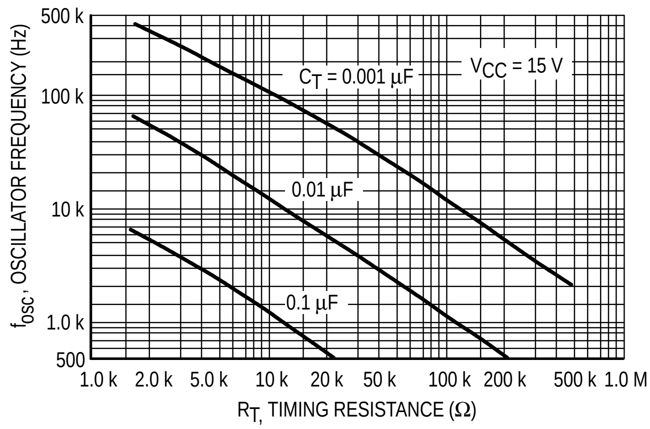


**Figure 4. Open Loop Voltage Gain and Phase versus Frequency**

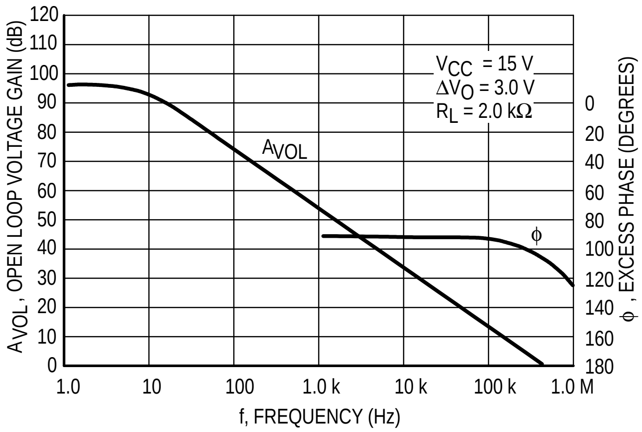



**Figure 5. Percent Deadtime versus Oscillator Frequency**

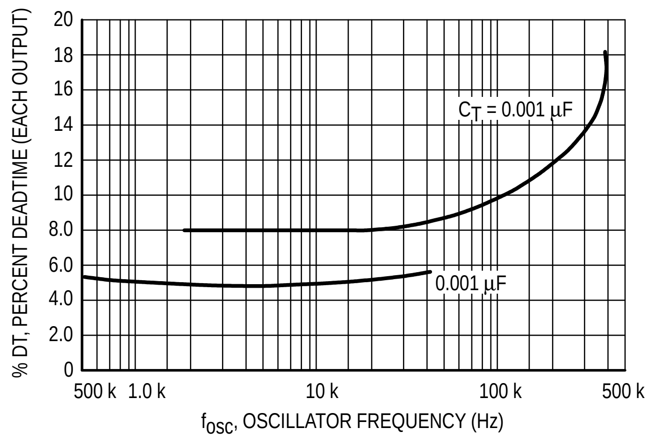



**Figure 6. Percent Duty Cycle versus Deadtime Control Voltage**

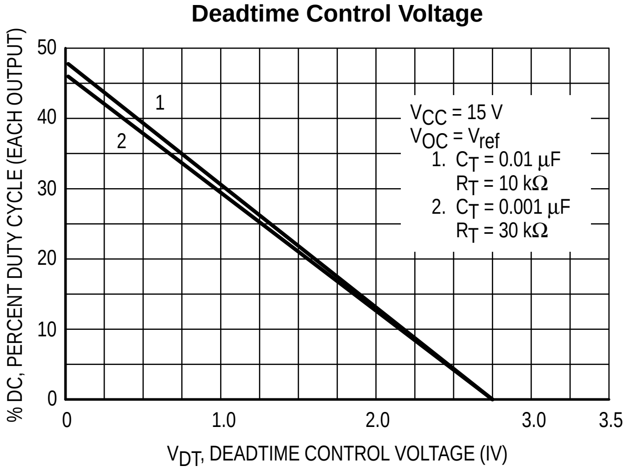



**Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current**

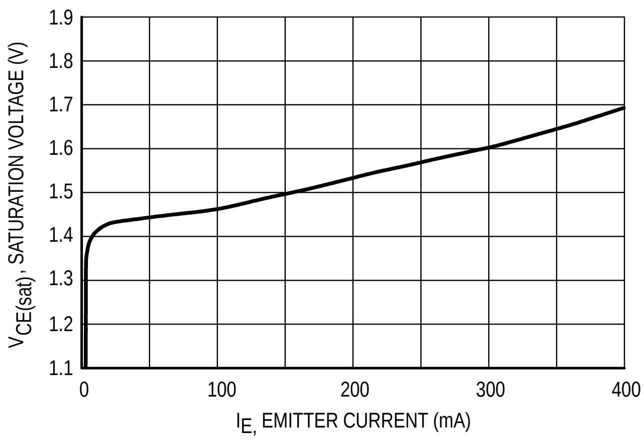



**Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current**

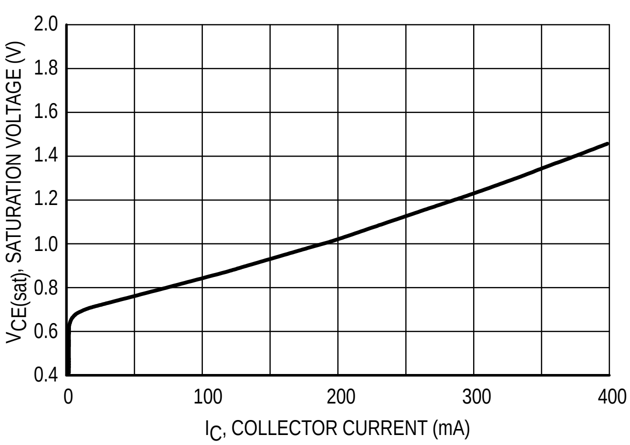



**Figure 9. Standby Supply Current versus Supply Voltage**

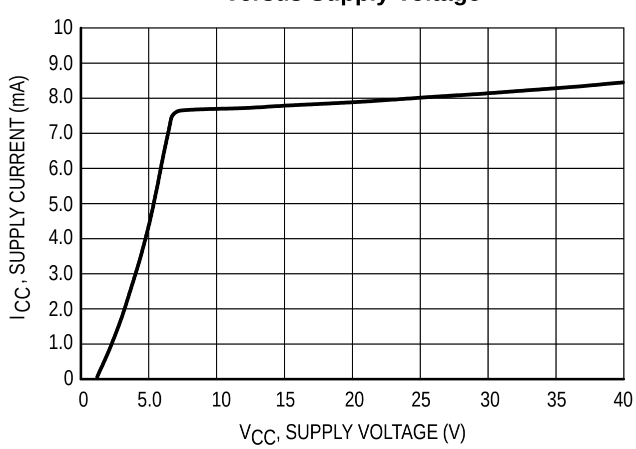


**Figure 10. Error–Amplifier Characteristics**

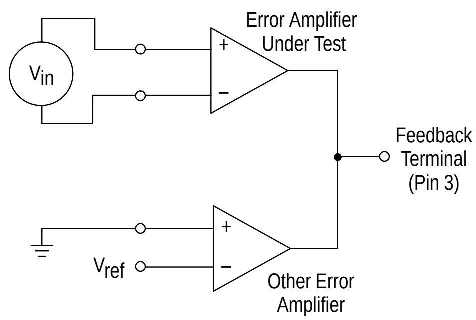



**Figure 11. Deadtime and Feedback Control Circuit**

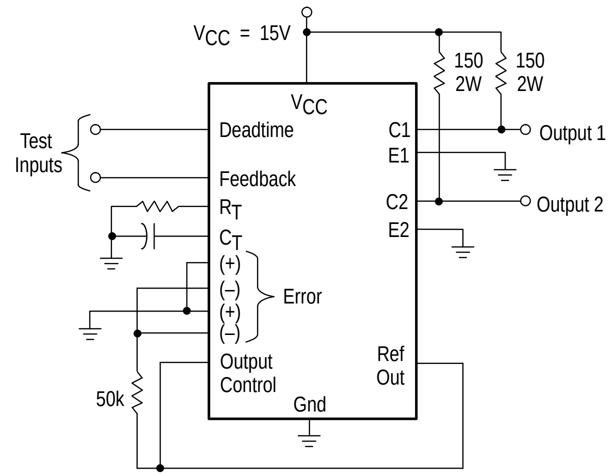



**Figure 12. Common–Emitter Configuration Test Circuit and Waveform**

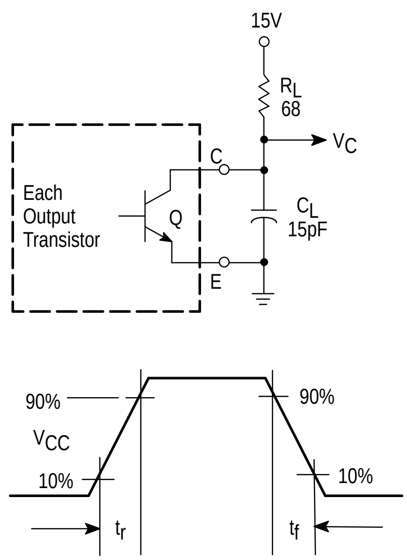



**Figure 13. Emitter–Follower Configuration Test Circuit and Waveform**

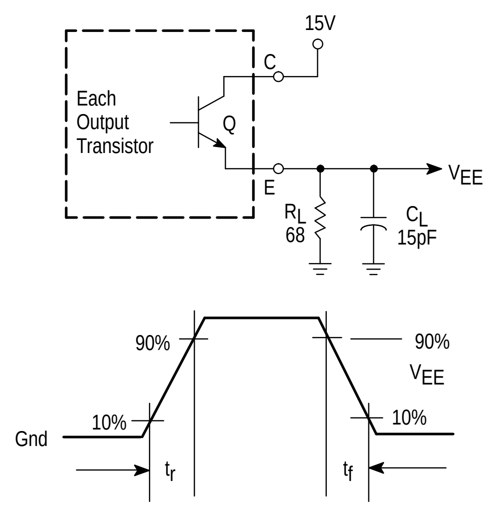


**Figure 14. Error–Amplifier Sensing Techniques**

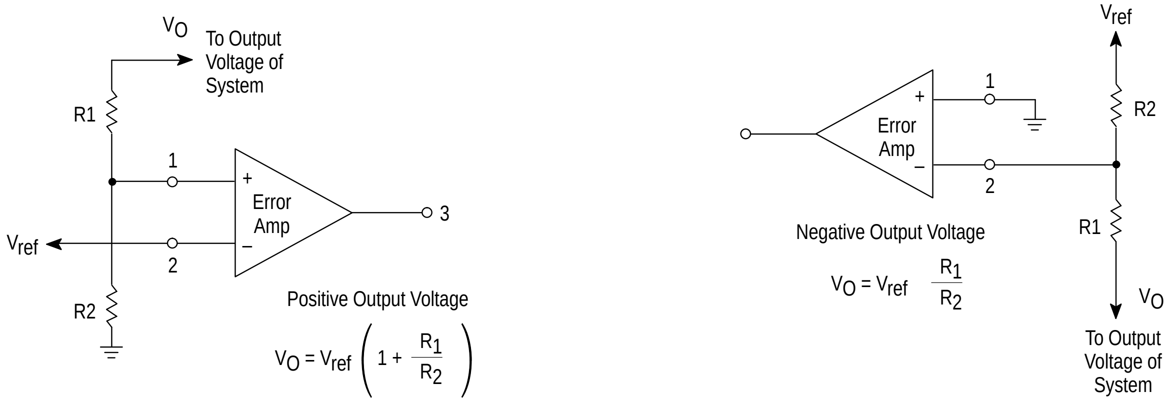



**Figure 15. Deadtime Control Circuit**

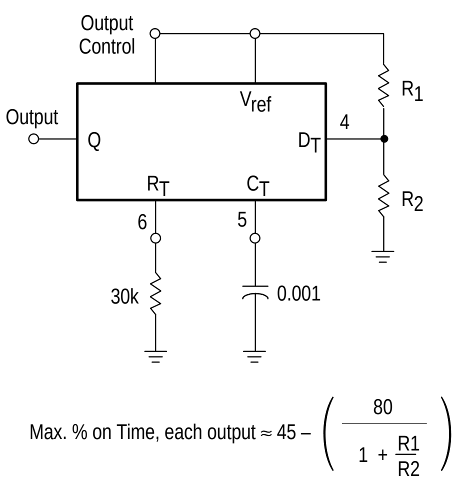



**Figure 16. Soft–Start Circuit**

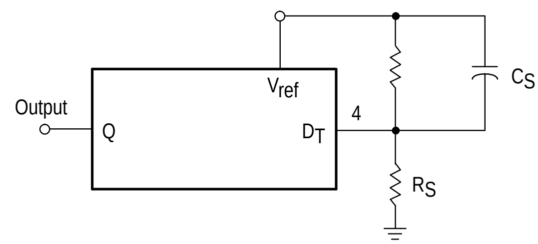



**Figure 17. Output Connections for Single–Ended and Push–Pull Configurations**

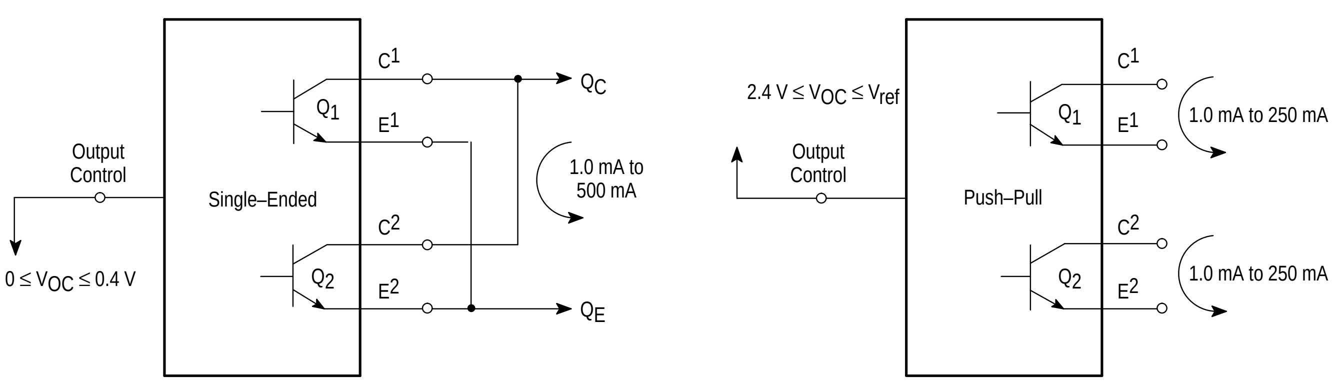


**Figure 18. Slaving Two or More Control Circuits**

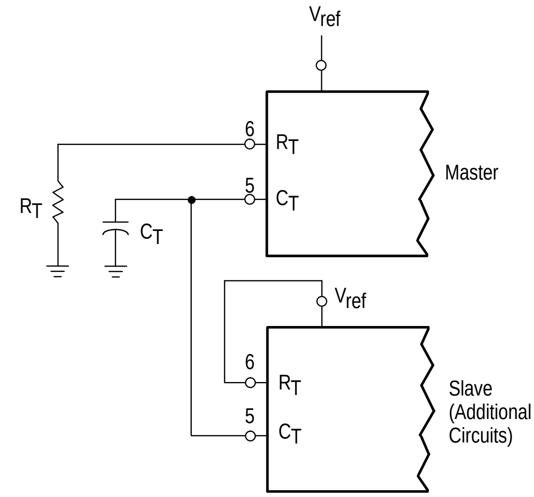



**Figure 19. Operation with $V_{in}$ > 40 V Using External Zener**

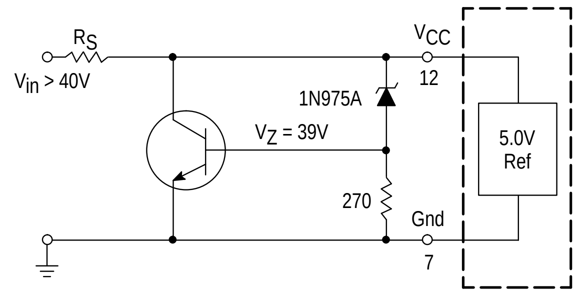
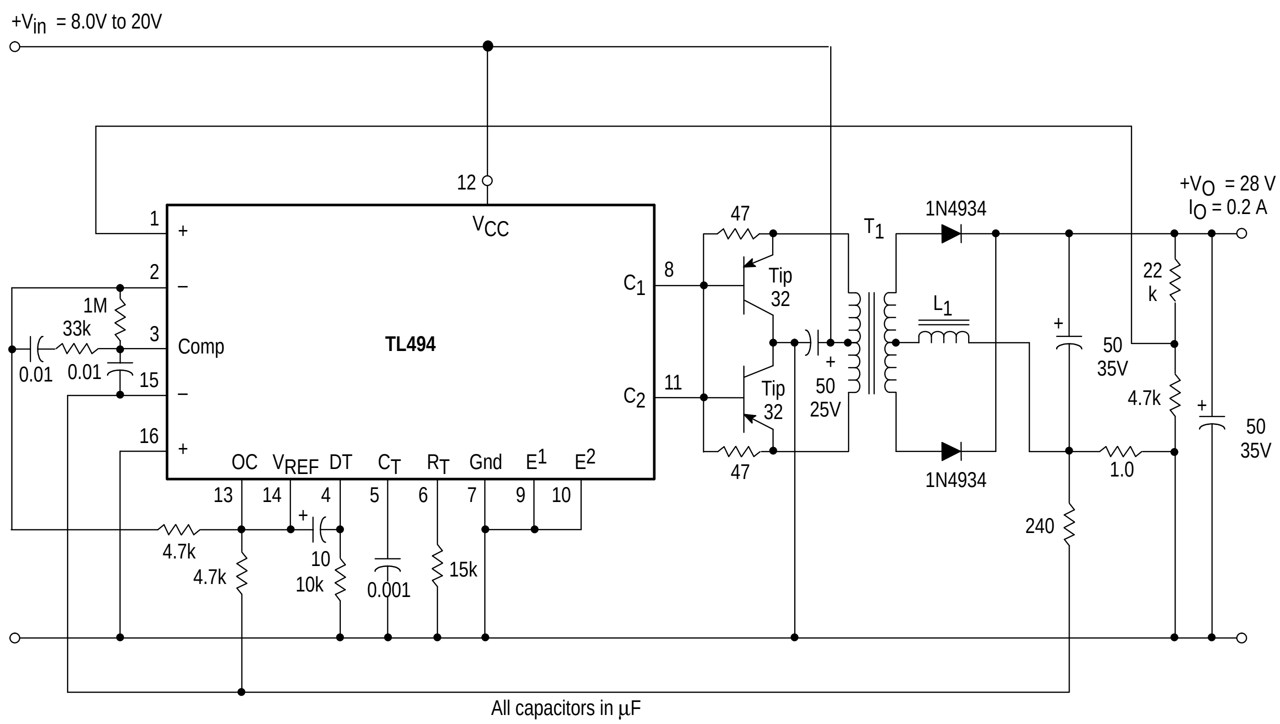


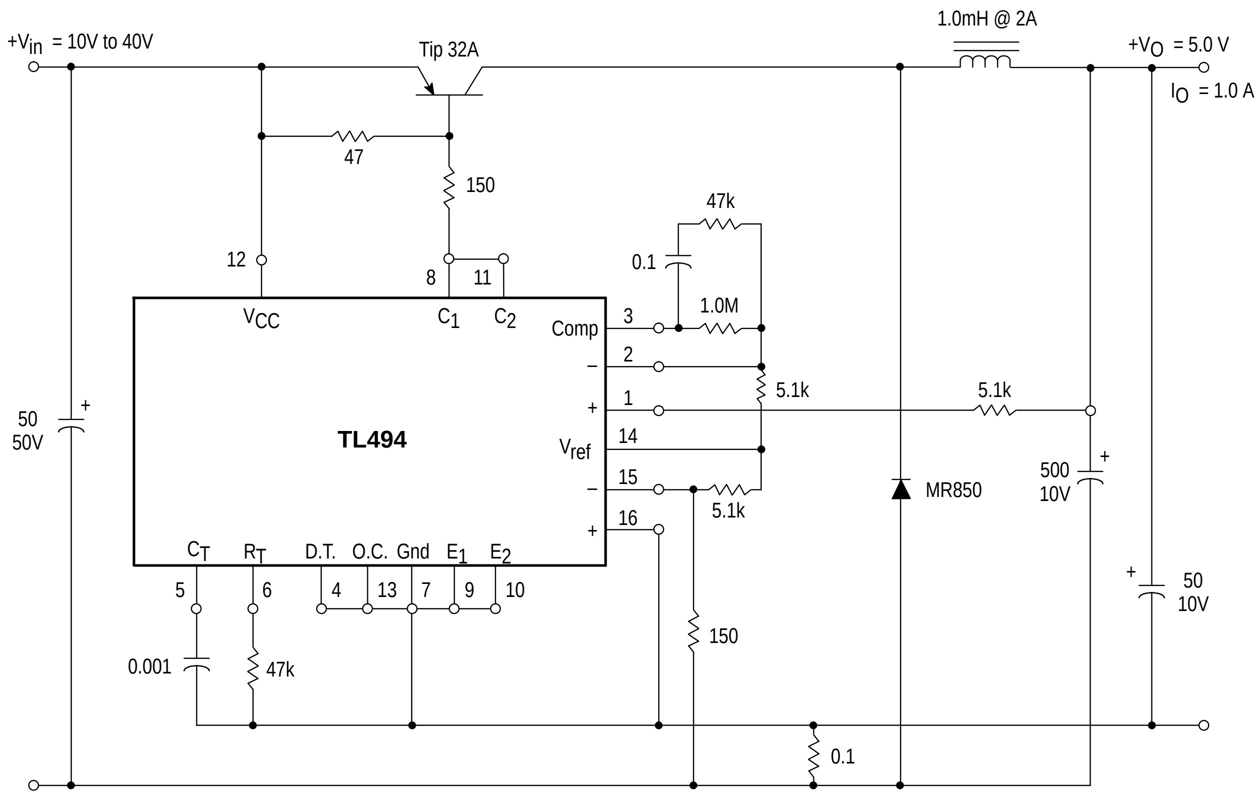

**Figure 20. Pulse Width Modulated Push–Pull Converter**




| Test | Conditions | Results |
|---|---|---|
| Line Regulation | $V_{in}$ = 10 V to 40 V | 14 mV  0.28% |
| Load Regulation | $V_{in}$ = 28 V, $I_O$ = 1.0 mA to 1.0 A | 3.0 mV  0.06% |
| Output Ripple | $V_{in}$ = 28 V, $I_O$ = 1.0 A | 65 mV pp  P.A.R.D. |
| Short Circuit Current | $V_{in}$ = 28 V, $R_L$ = 0.1 Ω | 1.6 A |
| Efficiency | $V_{in}$ = 28 V, $I_O$ = 1.0 A | 71% |

L1 – 3.5 mH @ 0.3 A
T1 – Primary: 20T C.T. #28 AWG
Secondary: 12OT C.T. #36 AWG
Core: Ferroxcube 1408P–L00–3CB

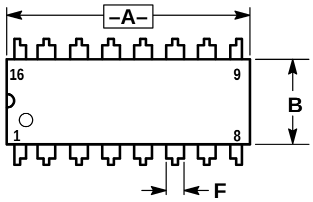
**Figure 21. Pulse Width Modulated Step–Down Converter**

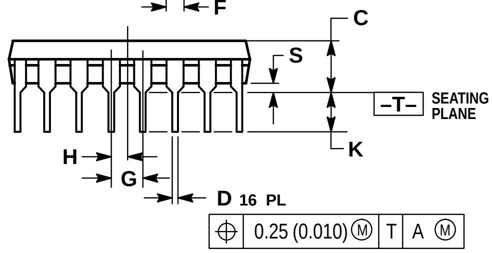


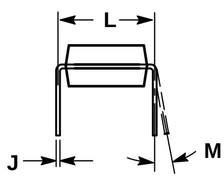

| Test | Conditions | Results | |
|---|---|---|---|
| Line Regulation | $V_{in}$ = 8.0 V to 40 V | 3.0 mV | 0.01% |
| Load Regulation | $V_{in}$ = 12.6 V, $I_O$ = 0.2 mA to 200 mA | 5.0 mV | 0.02% |
| Output Ripple | $V_{in}$ = 12.6 V, $I_O$ = 200 mA | 40 mV pp | P.A.R.D. |
| Short Circuit Current | $V_{in}$ = 12.6 V, $R_L$ = 0.1 Ω | 250 mA | |
| Efficiency | $V_{in}$ = 12.6 V, $I_O$ = 200 mA | 72% | |

## OUTLINE DIMENSIONS

**N SUFFIX**
PLASTIC PACKAGE
CASE 648–08
ISSUE R



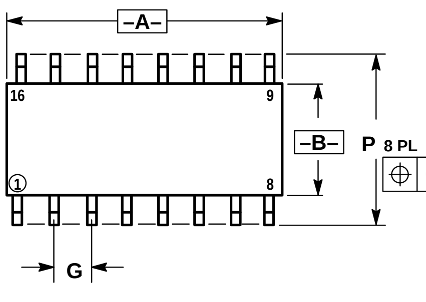



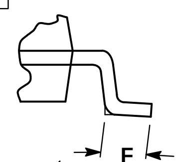



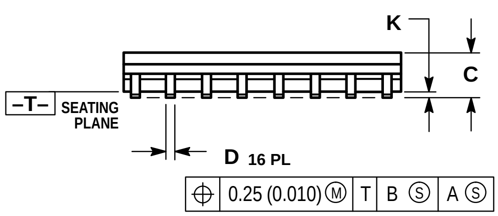

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

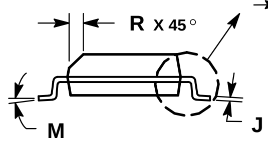
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

**D SUFFIX**
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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**MFAX**: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
**INTERNET**: http://Design–NET.com

**JAPAN**: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

**ASIA / PACIFIC**: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

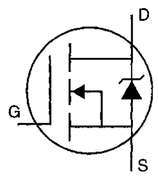
# International Rectifier

PD-9.374G

# IRF640

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements




$V_{DSS}$ = 200V

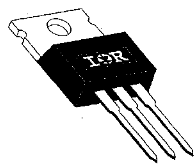
$R_{DS(on)}$ = 0.18Ω

$I_D$ = 18A

## Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.




TO-220AB



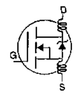
## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10 V | 18 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10 V | 11 | |
| $I_{DM}$ | Pulsed Drain Current ① | 72 | |
| $P_D$ @ $T_C$ = 25°C | Power Dissipation | 125 | W |
| | Linear Derating Factor | 1.0 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 580 | mJ |
| $I_{AR}$ | Avalanche Current ① | 18 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 13 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 5.0 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to +150 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting Torque, 6-32 or M3 screw | 10 lbf•in (1.1 N•m) | |

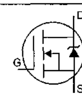
## Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | — | — | 1.0 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | — | 0.50 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | — | 62 | |

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 200 | — | — | V | $V_{GS}$=0V, $I_D$= 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.29 | — | V/°C | Reference to 25°C, $I_D$= 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.18 | Ω | $V_{GS}$=10V, $I_D$=11A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$=$V_{GS}$, $I_D$= 250µA |
| $g_{fs}$ | Forward Transconductance | 6.7 | — | — | S | $V_{DS}$=50V, $I_D$=11A ④ |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 25 | µA | $V_{DS}$=200V, $V_{GS}$=0V |
| | | — | — | 250 | | $V_{DS}$=160V, $V_{GS}$=0V, $T_J$=125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$=20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$=-20V |
| $Q_g$ | Total Gate Charge | — | — | 70 | nC | $I_D$=18A |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 13 | | $V_{DS}$=160V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | — | 39 | | $V_{GS}$=10V See Fig. 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 14 | — | ns | $V_{DD}$=100V |
| $t_r$ | Rise Time | — | 51 | — | | $I_D$=18A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 45 | — | | $R_G$=9.1Ω |
| $t_f$ | Fall Time | — | 36 | — | | $R_D$=5.4Ω See Figure 10 ④ |
| $L_D$ | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6 mm (0.25in.) from package and center of die contact  |
| $L_S$ | Internal Source Inductance | — | 7.5 | — | | |
| $C_{iss}$ | Input Capacitance | — | 1300 | — | pF | $V_{GS}$=0V |
| $C_{oss}$ | Output Capacitance | — | 430 | — | | $V_{DS}$=25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 130 | — | | $f$=1.0MHz See Figure 5 |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 18 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | — | 72 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 2.0 | V | $T_J$=25°C, $I_S$=18A, $V_{GS}$=0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | 300 | 610 | ns | $T_J$=25°C, $I_F$=18A |
| $Q_{rr}$ | Reverse Recovery Charge | — | 3.4 | 7.1 | µC | di/dt=100A/µs ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is neglegible (turn-on is dominated by $L_S$+$L_D$) | | | | |

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② $V_{DD}$=50V, starting $T_J$=25°C, L=2.7mH $R_G$=25Ω, $I_{AS}$=18A (See Figure 12)

③ $I_{SD}$≤18A, di/dt≤150A/µs, $V_{DD}$≤$V_{(BR)DSS}$, $T_J$≤150°C

④ Pulse width ≤ 300 µs; duty cycle ≤2%.

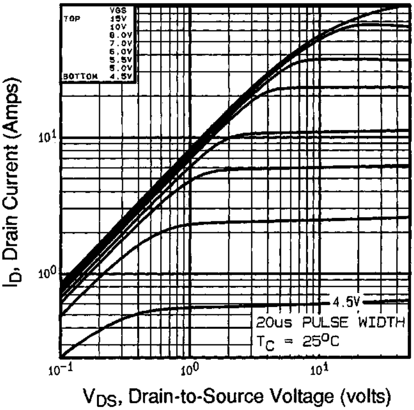



**Fig 1.** Typical Output Characteristics, TC=25°C

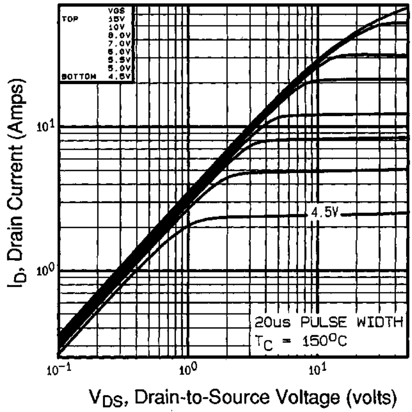



**Fig 2.** Typical Output Characteristics, TC=150°C

DATA SHEETS

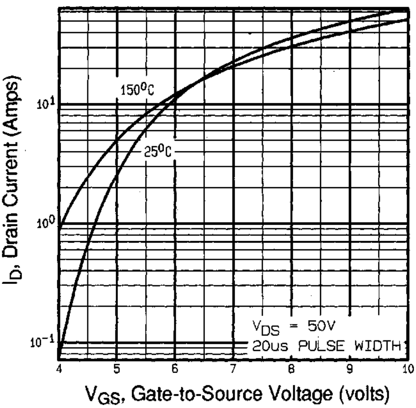



**Fig 3.** Typical Transfer Characteristics

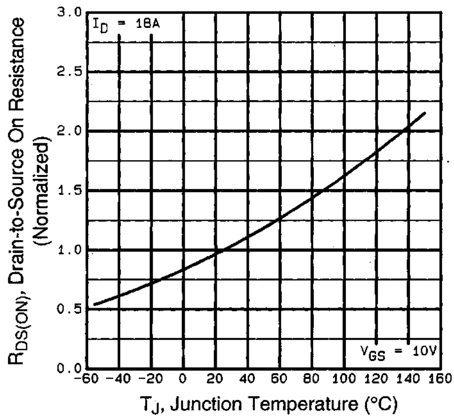



**Fig 4.** Normalized On-Resistance Vs. Temperature

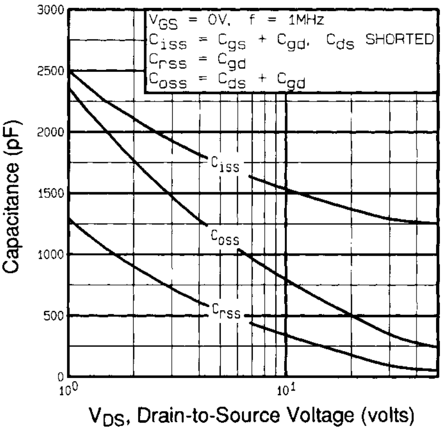



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

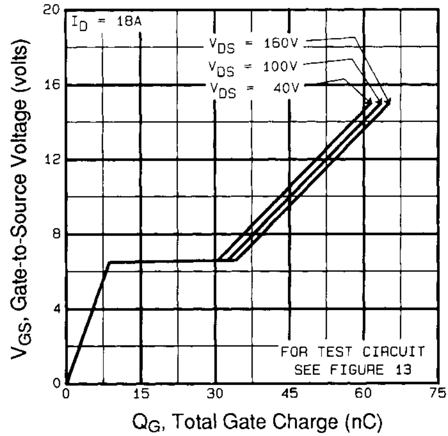



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

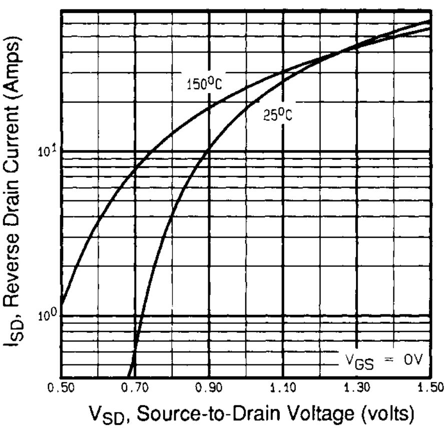



**Fig 7.** Typical Source-Drain Diode Forward Voltage

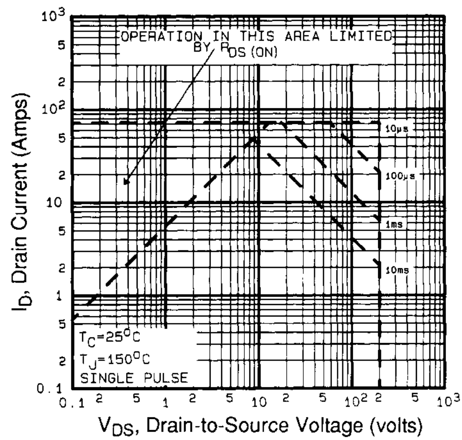



**Fig 8.** Maximum Safe Operating Area

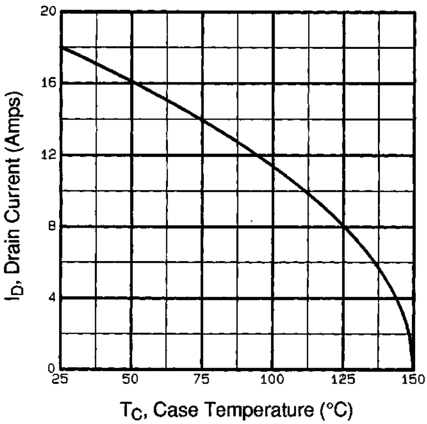



**Fig 9.** Maximum Drain Current Vs. Case Temperature

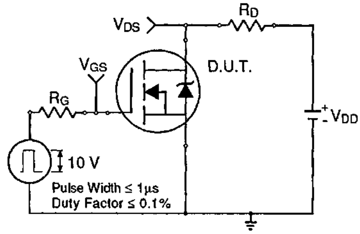



**Fig 10a.** Switching Time Test Circuit

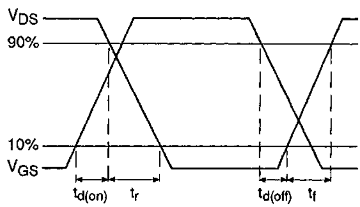



**Fig 10b.** Switching Time Waveforms

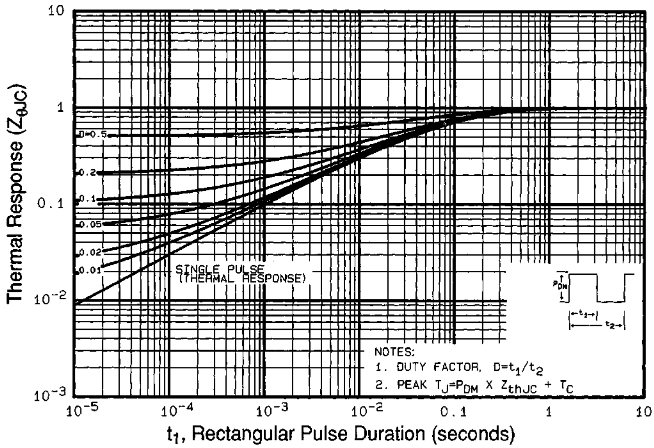



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

DATA SHEETS

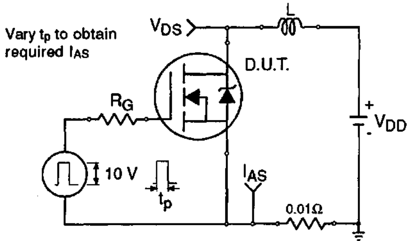



**Fig 12a.** Unclamped Inductive Test Circuit

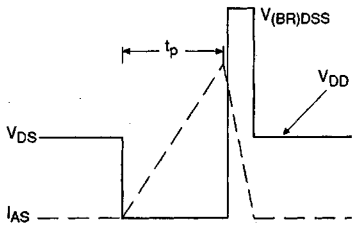



**Fig 12b.** Unclamped Inductive Waveforms

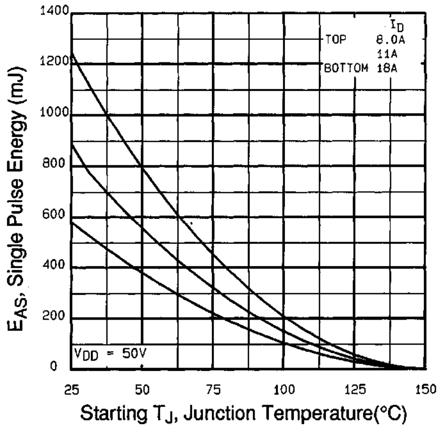



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

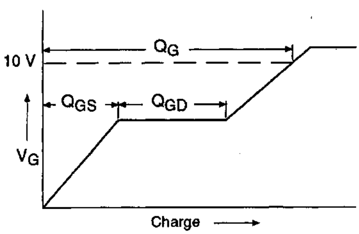



**Fig 13a.** Basic Gate Charge Waveform

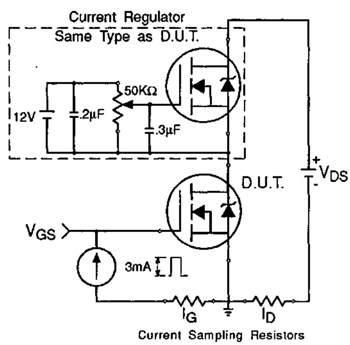



**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1509

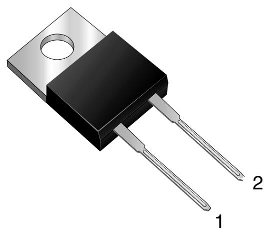
**Appendix C:** Part Marking Information – See page 1516

**Appendix E:** Optional Leadforms – See page 1525

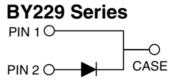
International
IOR Rectifier

# Fast Switching Plastic Rectifier

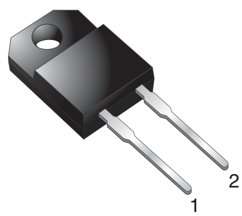
TO-220AC



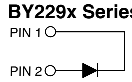

BY229 Series



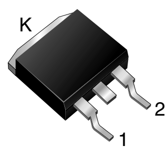

ITO-220AC



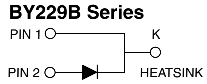

BY229x Series




TO-263AB




BY229B Series




| PRIMARY CHARACTERISTICS | |
|---|---|
| $I_{F(AV)}$ | 8.0 A |
| $V_{RRM}$ | 200 V to 800 V |
| $I_{FSM}$ | 100 A |
| $t_{rr}$ | 145 ns |
| $V_F$ | 1.85 V |
| $T_J$ max. | 150 °C |

## FEATURES

- Glass passivated chip junction
- Superfast recovery time for high efficiency
- Low leakage current
- High forward surge capability
- Meets MSL level 1, per J-STD-020, LF maximum peak of 245 °C (for TO-263AB package)
- Solder dip 260 °C, 40 s (for TO-220AC and ITO-220AC package)
- Component in accordance to RoHS 2002/95/EC and WEEE 2002/96/EC

## TYPICAL APPLICATIONS

For use in fast switching rectification of power supply, inverters, converters and freewheeling diodes application.

## MECHANICAL DATA

**Case:** TO-220AC, ITO-220AC, TO-263AB

Epoxy meets UL 94V-0 flammability rating

**Terminals:** Matte tin plated leads, solderable per J-STD-002 and JESD22-B102

E3 suffix for commercial grade, meets JESD 201 class 1A whiskter test, HE3 suffix for high reliability grade (AEC Q101 qualified), meets JESD 201 class 2 whisker test

**Polarity:** As marked

**Mounting Torque:** 10 in-lbs maximum

**MAXIMUM RATINGS** ($T_C$ = 25 °C unless otherwise noted)

| PARAMETER | SYMBOL | BY229-200 | BY229-400 | BY229-600 | BY229-800 | UNIT |
|---|---|---|---|---|---|---|
| Maximum recurrent peak reverse voltage | $V_{RRM}$ | 200 | 400 | 600 | 800 | V |
| Maximum RMS voltage | $V_{RMS}$ | 140 | 280 | 420 | 560 | V |
| Maximum DC blocking voltage | $V_{DC}$ | 200 | 400 | 600 | 800 | V |
| Maximum average forward rectified current at $T_C$ = 100 °C | $I_{F(AV)}$ | 8.0 | | | | A |
| Peak forward surge current 8.3 ms single half sine-wave superimposed on rated load | $I_{FSM}$ | 100 | | | | A |
| Maximum slope of reverse recovery current $I_F$ = 2.0 A, $V_R$ = 30 V, dI/dt = 20 µs | dI/dt | 60 | | | | A/µs |
| Operating junction and storage temperature range | $T_J$, $T_{STG}$ | - 40 to + 150 | | | | °C |
| Isolation voltage (ITO-220AC only) from terminal to heatsink t = 1 min | $V_{AC}$ | 1500 | | | | V |

| **ELECTRICAL CHARACTERISTICS** ($T_C$ = 25 °C unless otherwise noted) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS** | | **SYMBOL** | **BY229-200** | **BY229-400** | **BY229-600** | **BY229-800** | **UNIT** |
| Maximum instantaneous forward voltage (1) | 20 A | | $V_F$ | 1.85 | | | | V |
| Maximum DC reverse current at rated DC blocking voltage | | $T_J$ = 25 °C<br>$T_J$ = 125 °C | $I_R$ | 10<br>300 | | | | µA |
| Maximum reverse recovery time | $I_F$ = 1.0 A, $V_R$ = 30 V, dI/dt = 50 A/µs, $I_{rr}$ = 10 % $I_{RM}$ | | $t_{rr}$ | 145 | | | | ns |
| Maximum recovered stored charge | $I_F$ = 2.0 A, $V_R$ = 30 V, dI/dt = 20 A/µs | | $Q_{rr}$ | 700 | | | | nC |

**Note:**

(1) Pulse test: 300 µs pulse width, 1 % duty cycle

| **THERMAL CHARACTERISTICS** ($T_C$ = 25 °C unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **BY229** | **BY229X** | **BY229B** | **UNIT** |
| Typical thermal resistance from junction to case | $R_{\theta JC}$ | 2.0 | 4.8 | 2.0 | °C/W |
| Typical thermal resistance from junction to air | $R_{\theta JA}$ | 20 | - | 20 | °C/W |

| **ORDERING INFORMATION** (Example) | | | | | |
|---|---|---|---|---|---|
| **PACKAGE** | **PREFERRED P/N** | **UNIT WEIGHT (g)** | **PACKAGE CODE** | **BASE QUANTITY** | **DELIVERY MODE** |
| TO-220AC | BY229-200-E3/45 | 1.80 | 45 | 50/tube | Tube |
| ITO-220AC | BY229X-200-E3/45 | 1.95 | 45 | 50/tube | Tube |
| TO-263AB | BY229B-200-E3/45 | 1.77 | 45 | 50/tube | Tube |
| TO-263AB | BY229B-200-E3/81 | 1.77 | 81 | 800/reel | Tape reel |
| TO-220AC | BY229-200HE3/45 (1) | 1.80 | 45 | 50/tube | Tube |
| ITO-220AC | BY229X-200HE3/45 (1) | 1.95 | 45 | 50/tube | Tube |
| TO-263AB | BY229B-200HE3/45 (1) | 1.77 | 45 | 50/tube | Tube |
| TO-263AB | BY229B-200HE3/81 (1) | 1.77 | 81 | 800/reel | Tape reel |

**Note:**

(1) Automotive grade AEC Q101 qualified

## RATINGS AND CHARACTERISTICS CURVES

($T_A$ = 25 °C unless otherwise noted)

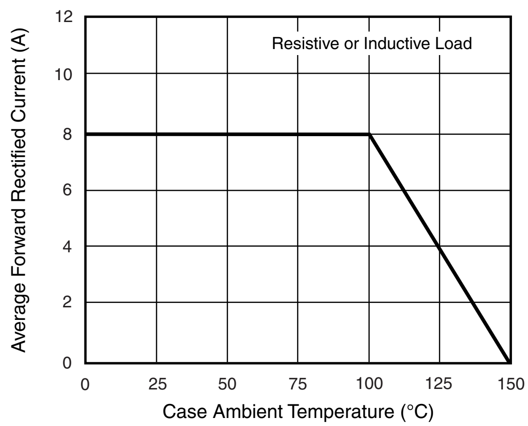



Figure 1. Forward Current Derating Curve

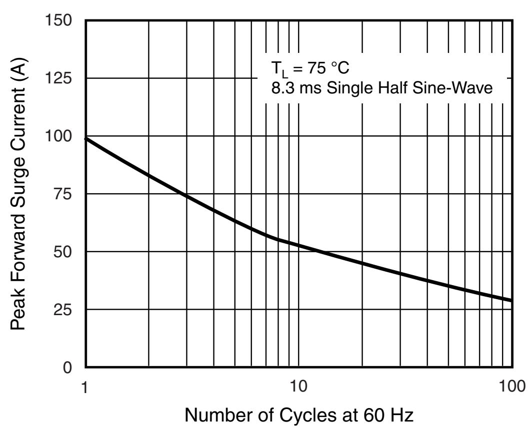



Figure 2. Maximum Non-Repetitive Peak Forward Surge Current

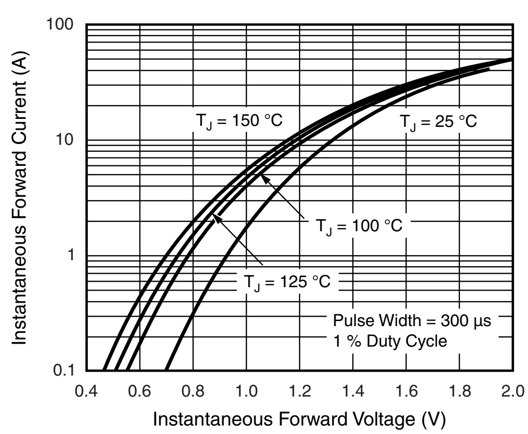



Figure 3. Typical Instantaneous Forward Characteristics

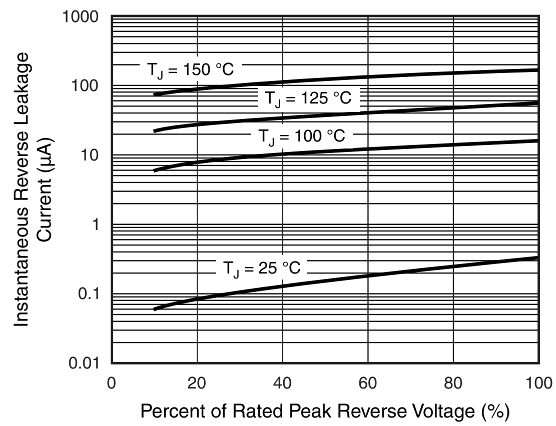



Figure 4. Typical Reverse Leakage Characteristics

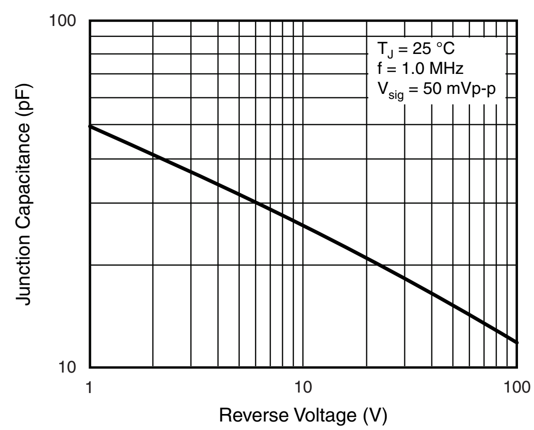
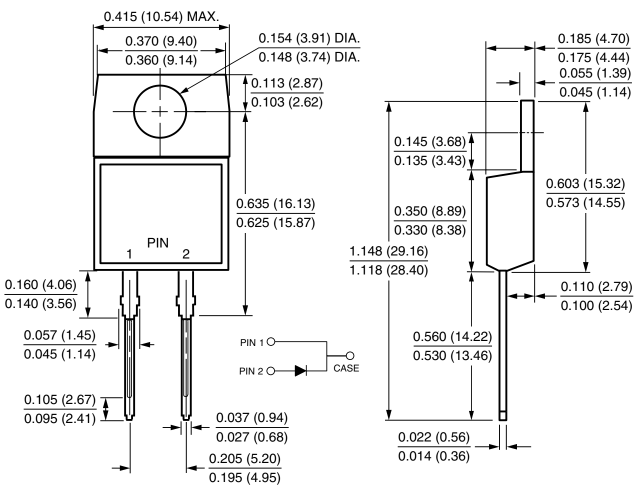


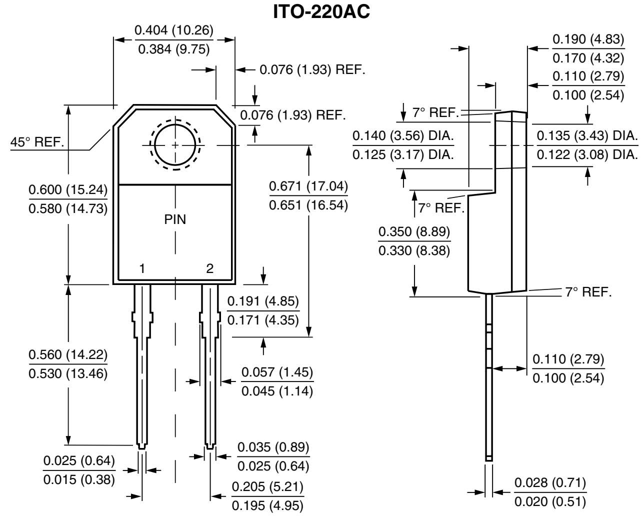

Figure 5. Typical Junction Capacitance

## PACKAGE OUTLINE DIMENSIONS in inches (millimeters)

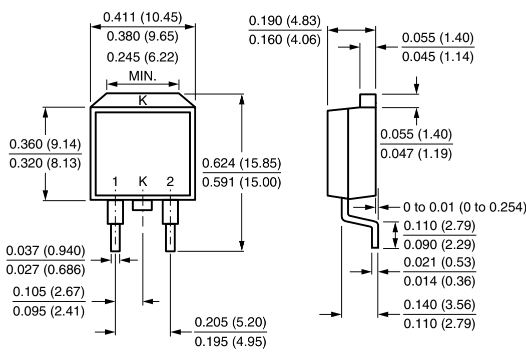
**TO-220AC**



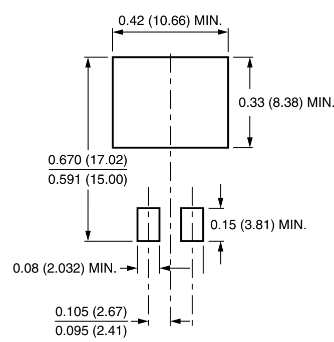

**ITO-220AC**




**TO-263AB**




Mounting Pad Layout



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