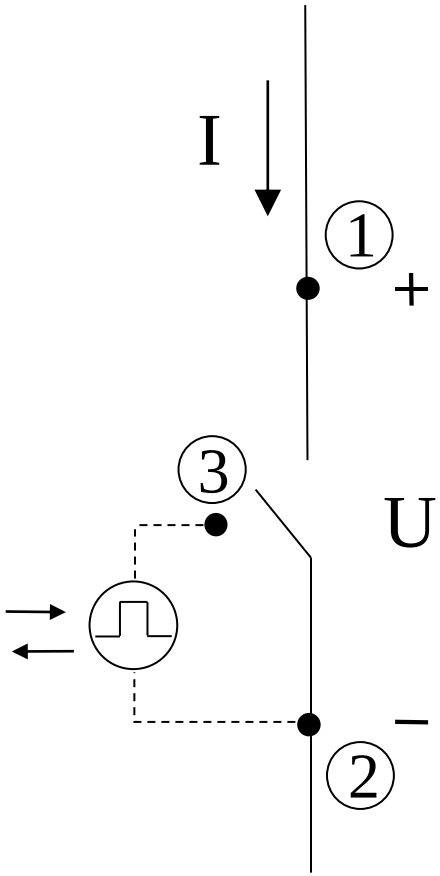
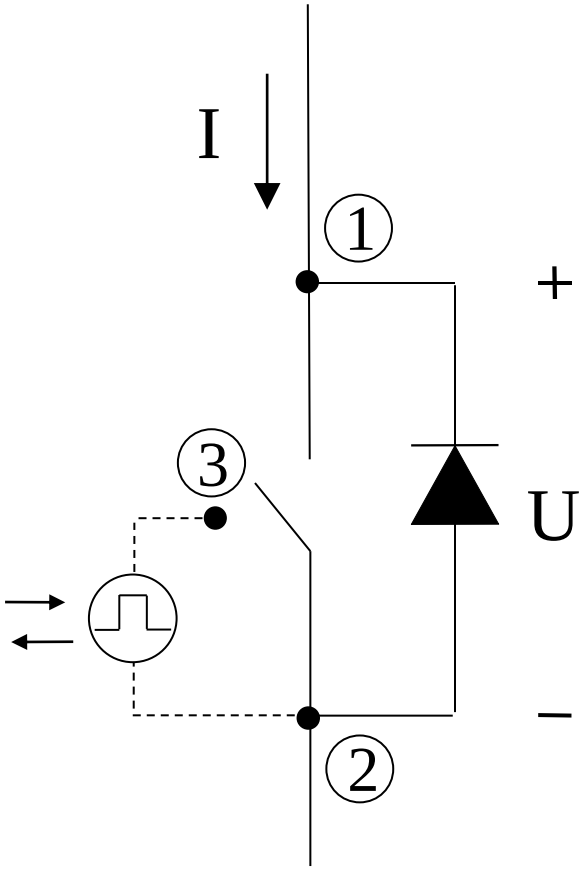
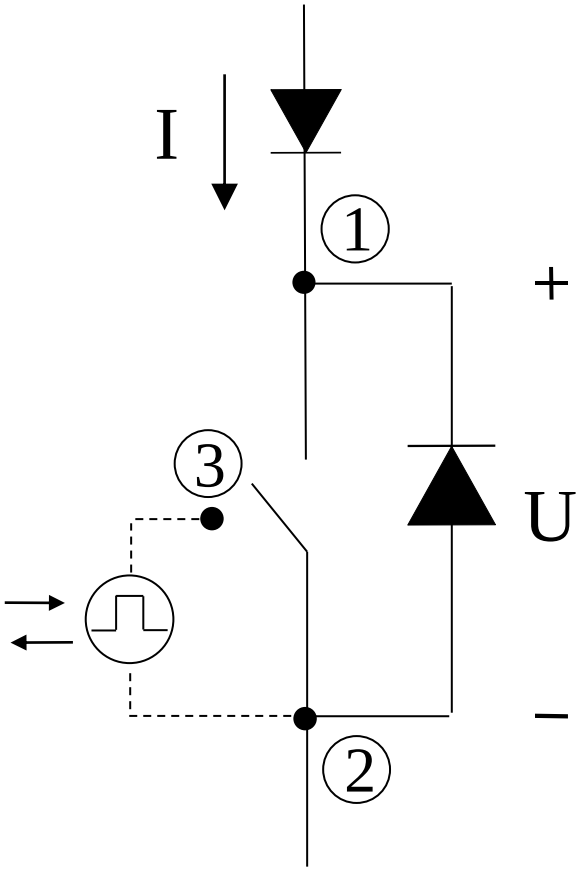


a) Bloqueo inverso intrínseco



b) Conducción inversa no controlada

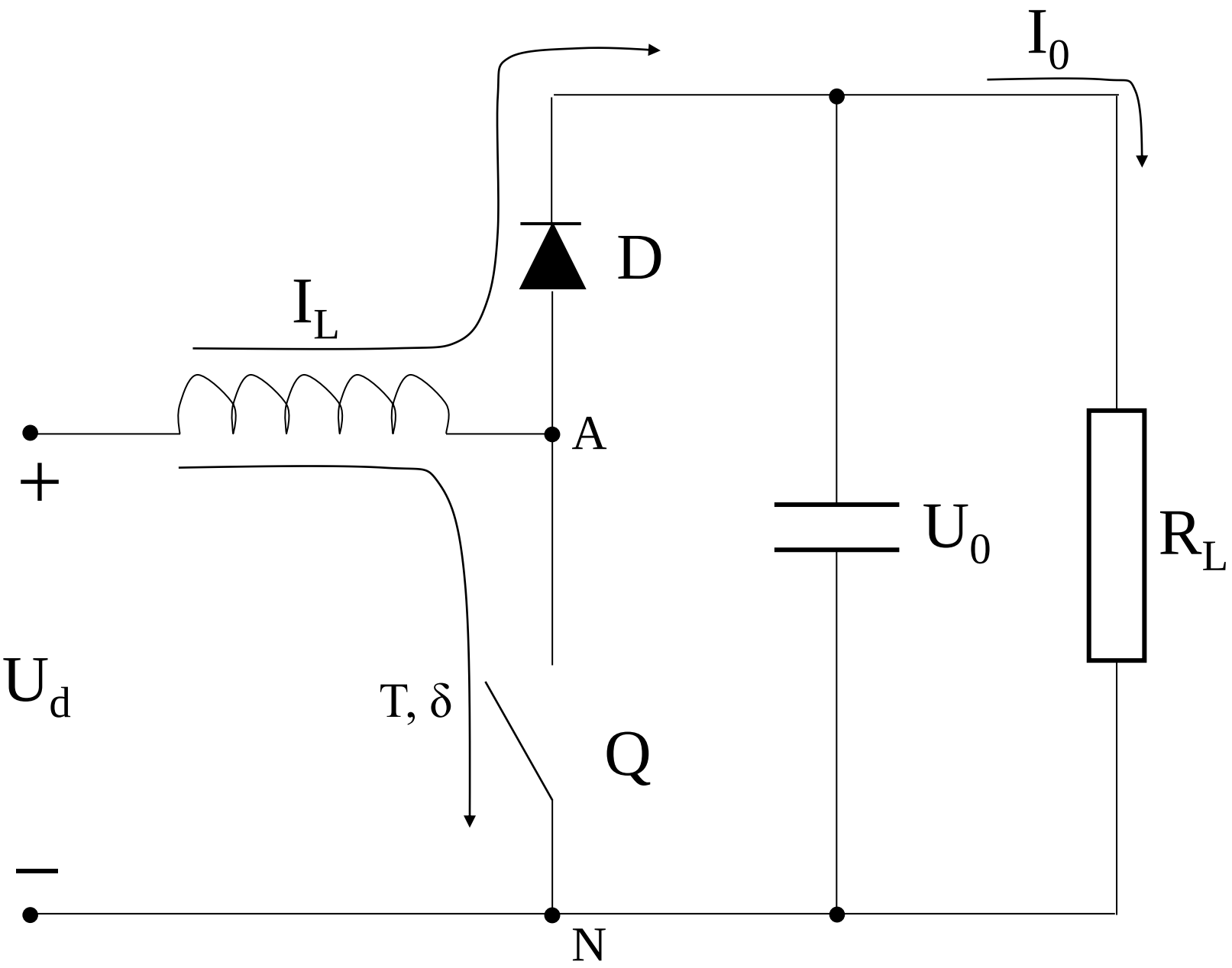


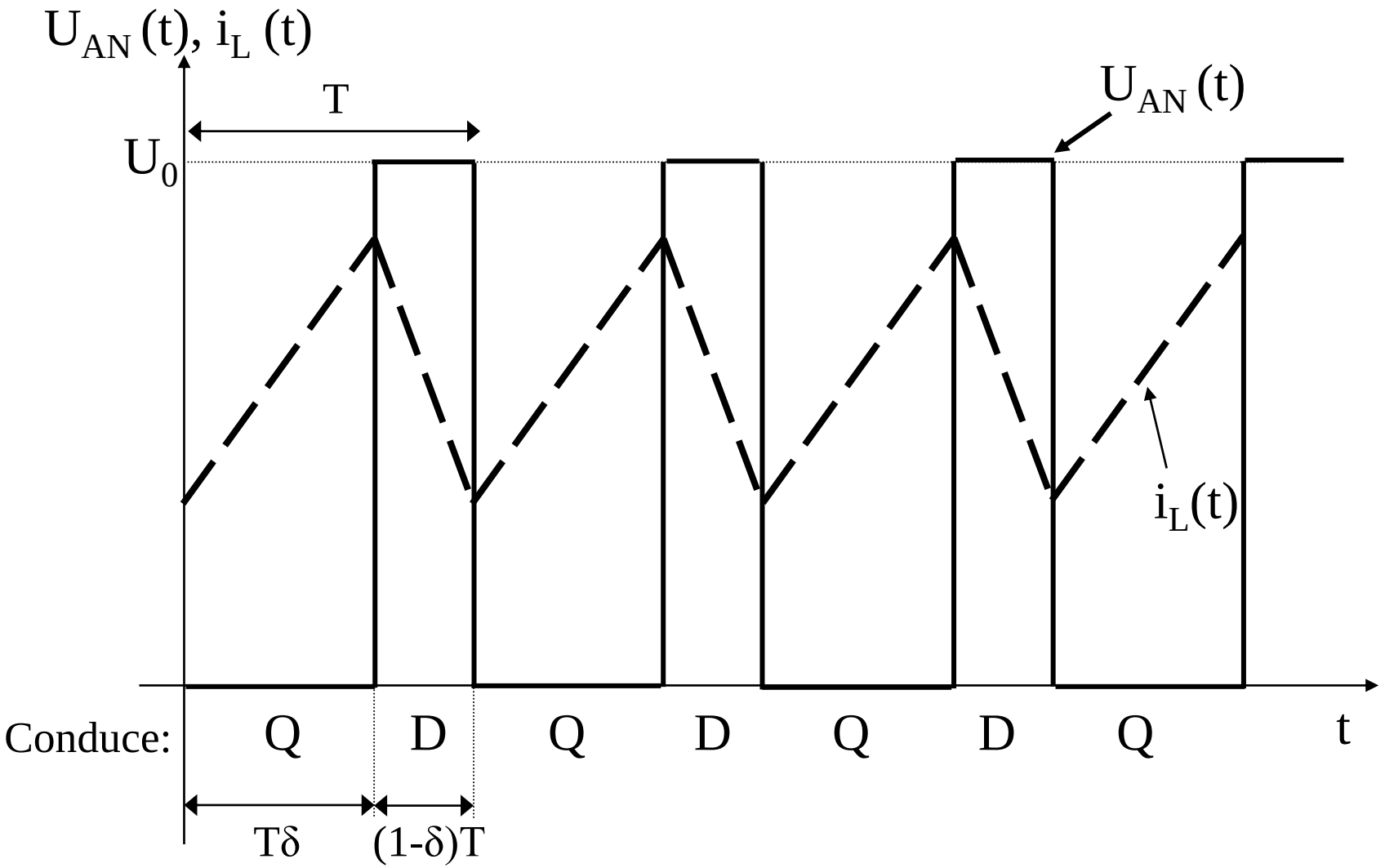
c) Bloqueo inverso con diodo serie

① Electrodo de potencia positivo

② Electrodo de potencia negativo

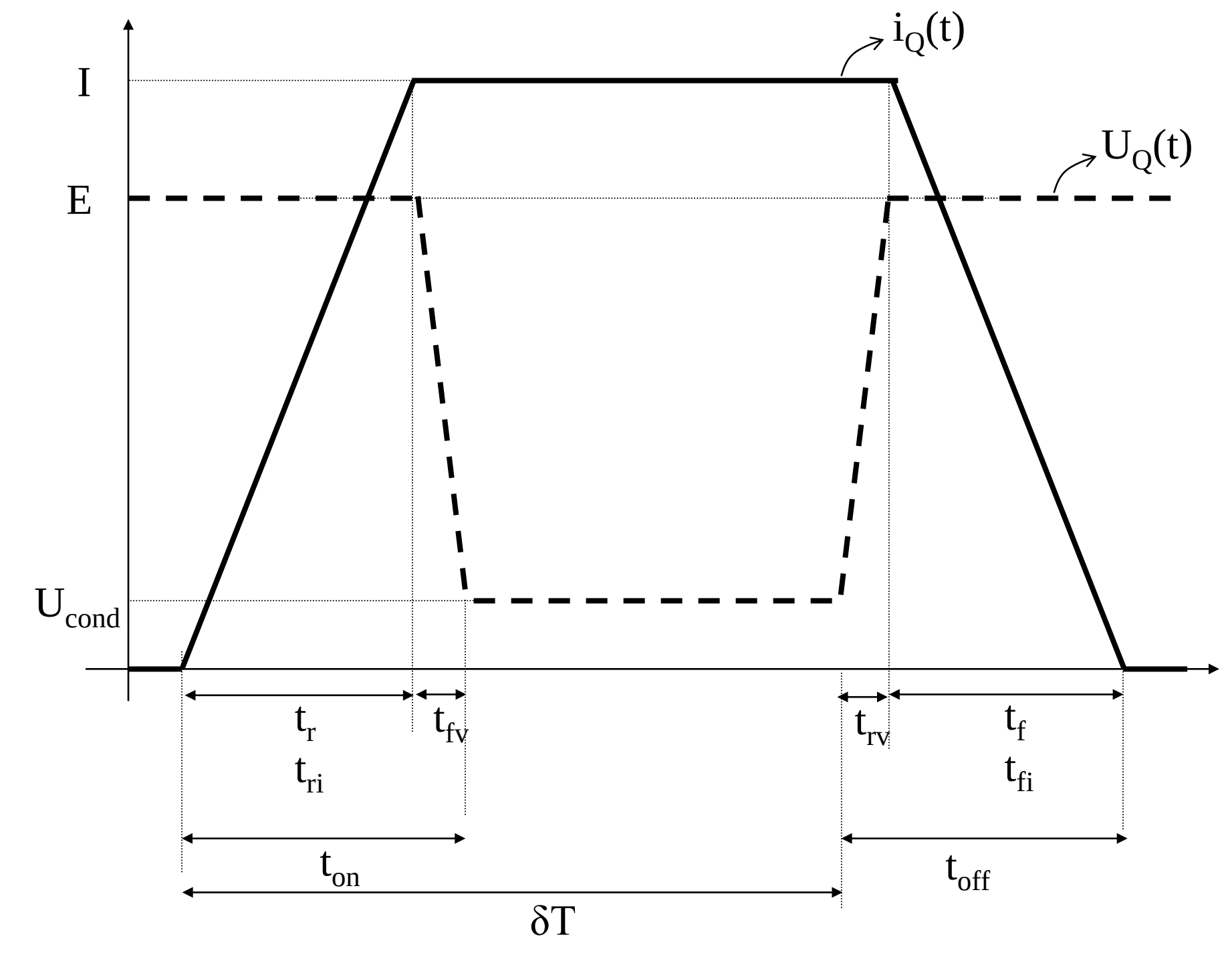
③ Electrodo de comando

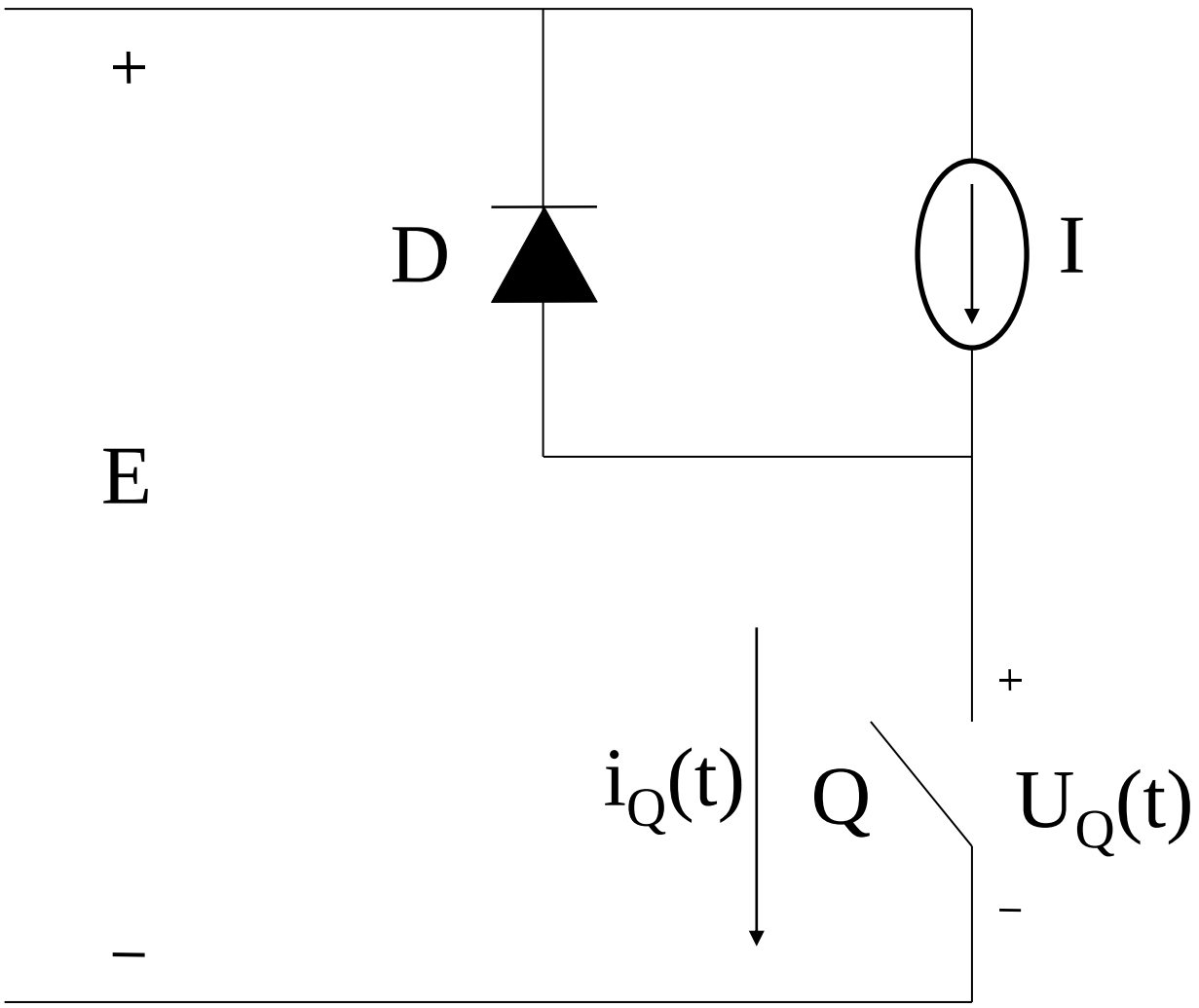

I0
D
IL
A
+
U0
RL
Ud
T, δ
Q
–
N



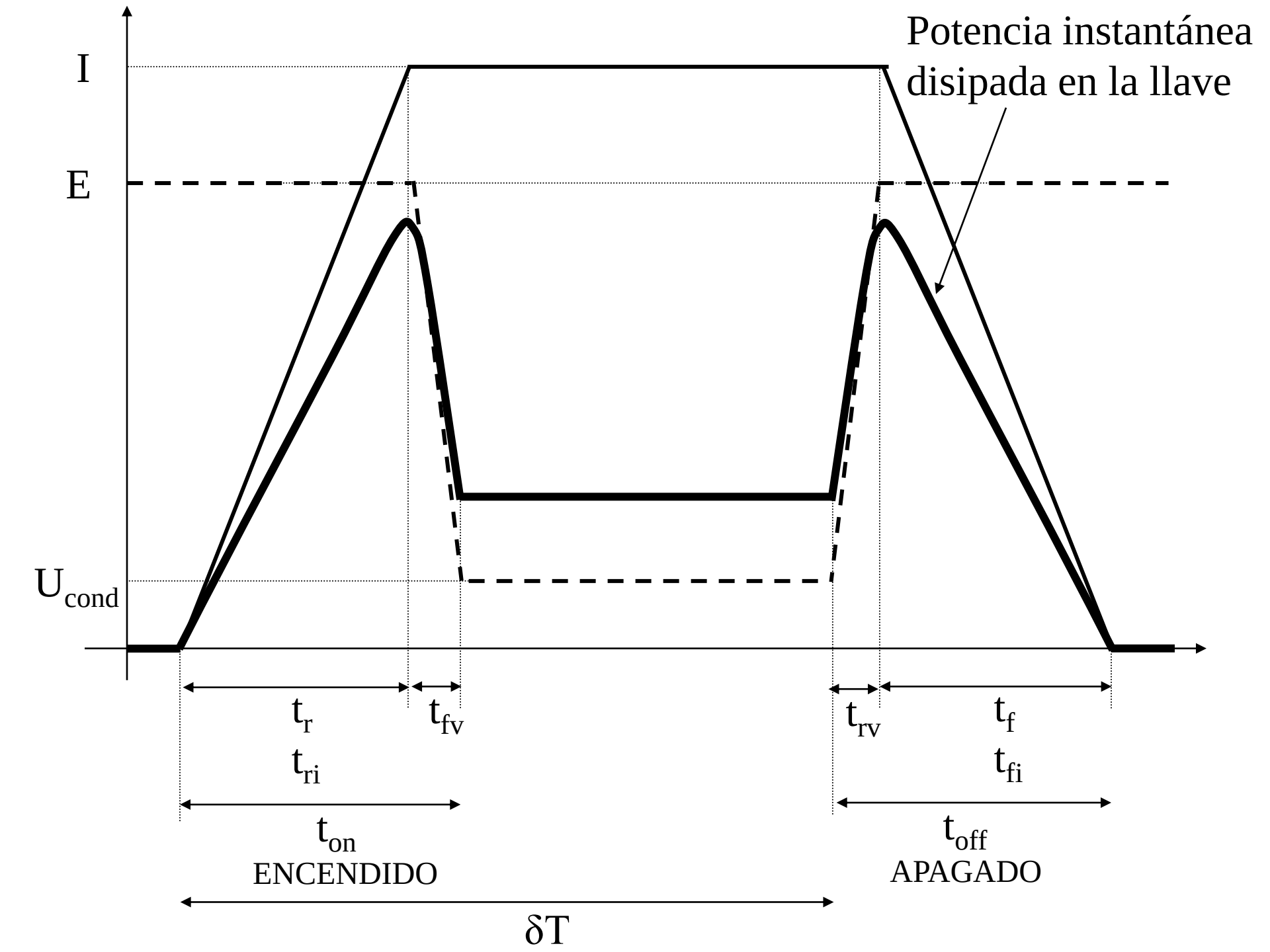
De la gráfica: $$\Delta I = \frac{U_d}{L}\delta T = \frac{U_0 - U_d}{L}(1-\delta)T$$

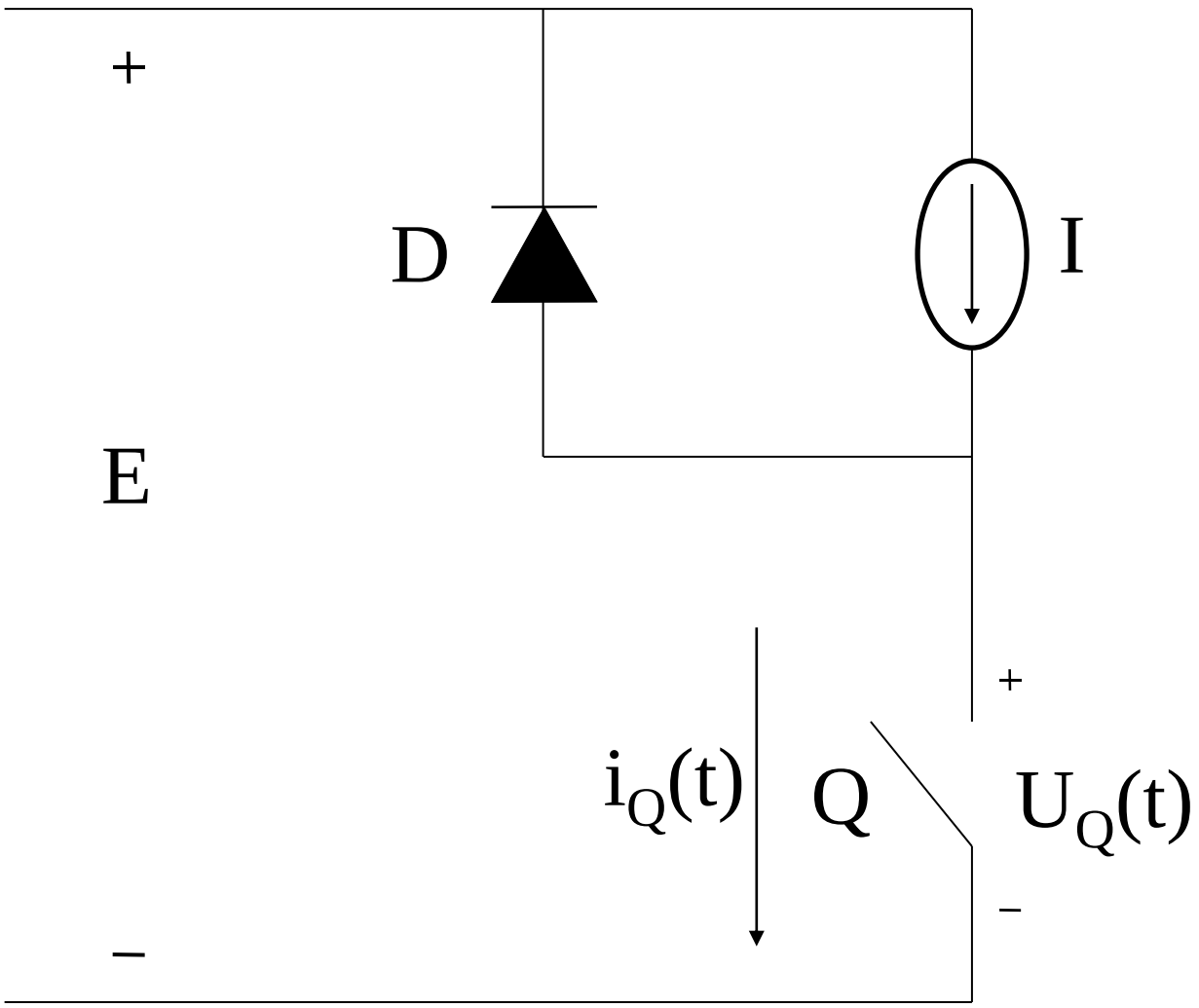
$$U_d\delta = (1-\delta)(U_0 - U_d) \quad \Rightarrow \quad U_0 = \frac{U_d}{1-\delta}$$


I
E
U_{cond}
$i_Q(t)$
$U_Q(t)$
t_r
t_{ri}
t_{fv}
t_{rv}
t_f
t_{fi}
t_{on}
t_{off}
δT



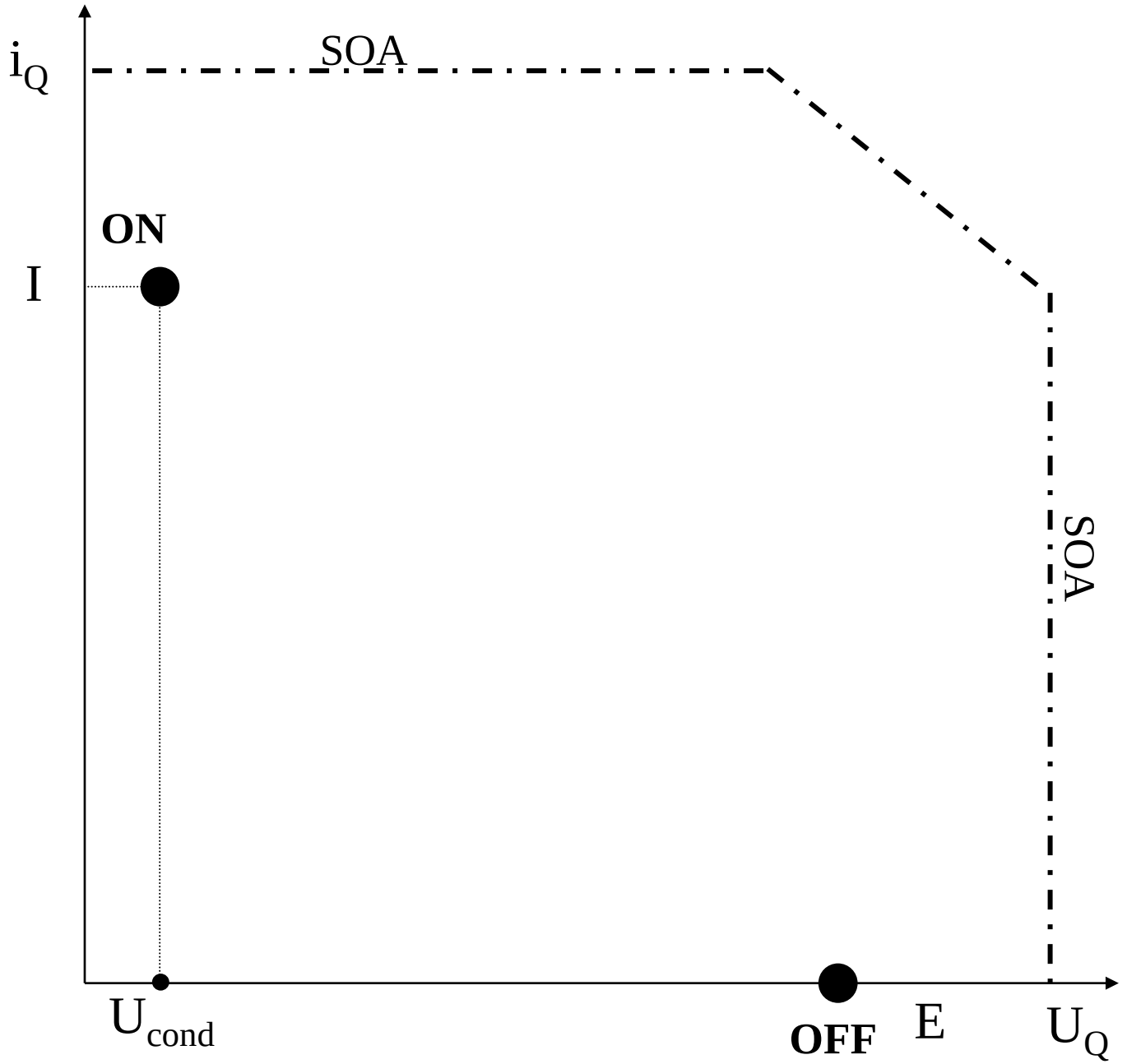
Clamp inductive load
Carga inductiva “clampeada”

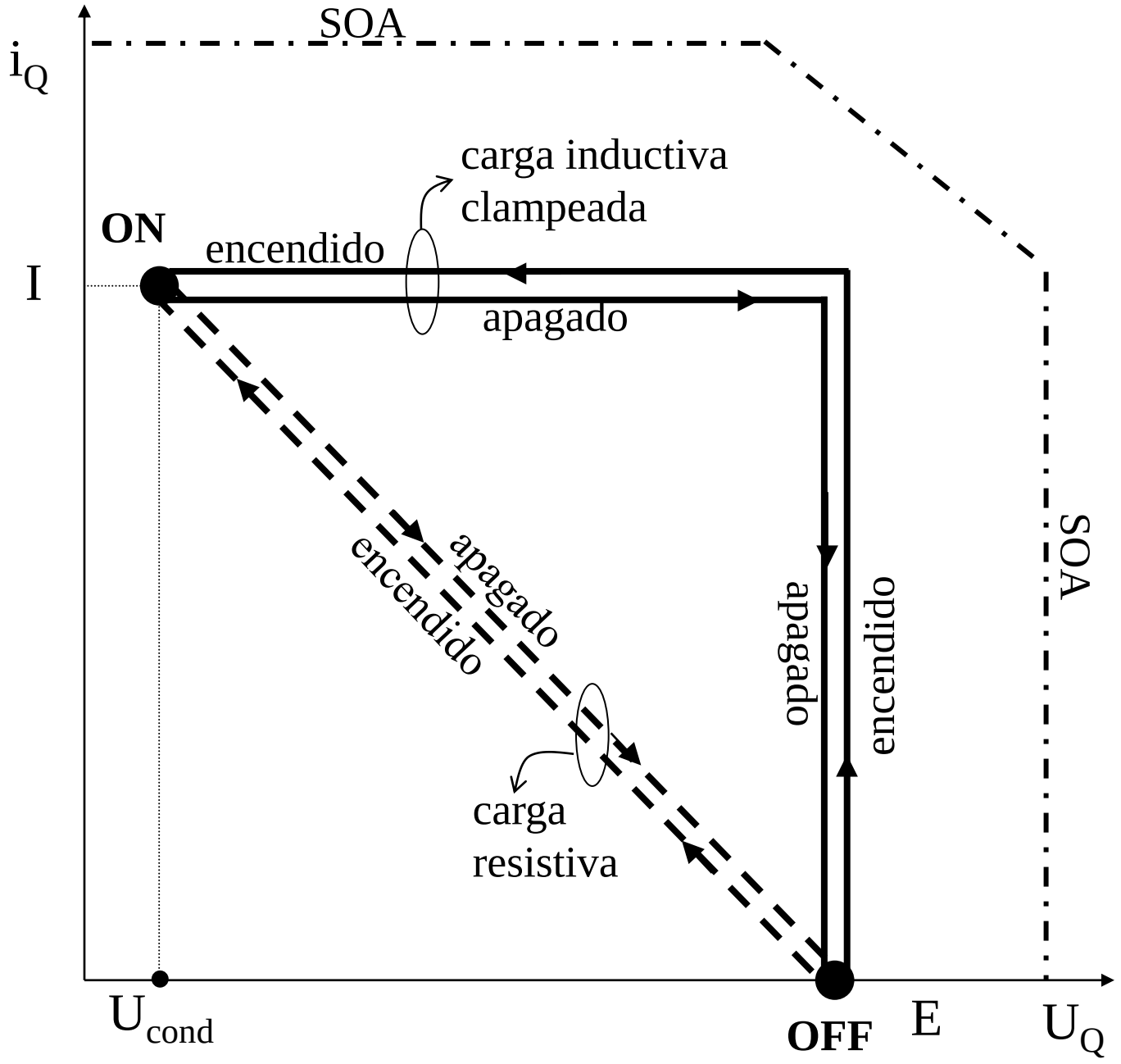

Potencia instantánea
disipada en la llave
I
E
U_{cond}
t_r
t_{fv}
t_{ri}
t_{on}
ENCENDIDO
t_{rv}
t_f
t_{fi}
t_{off}
APAGADO
δT



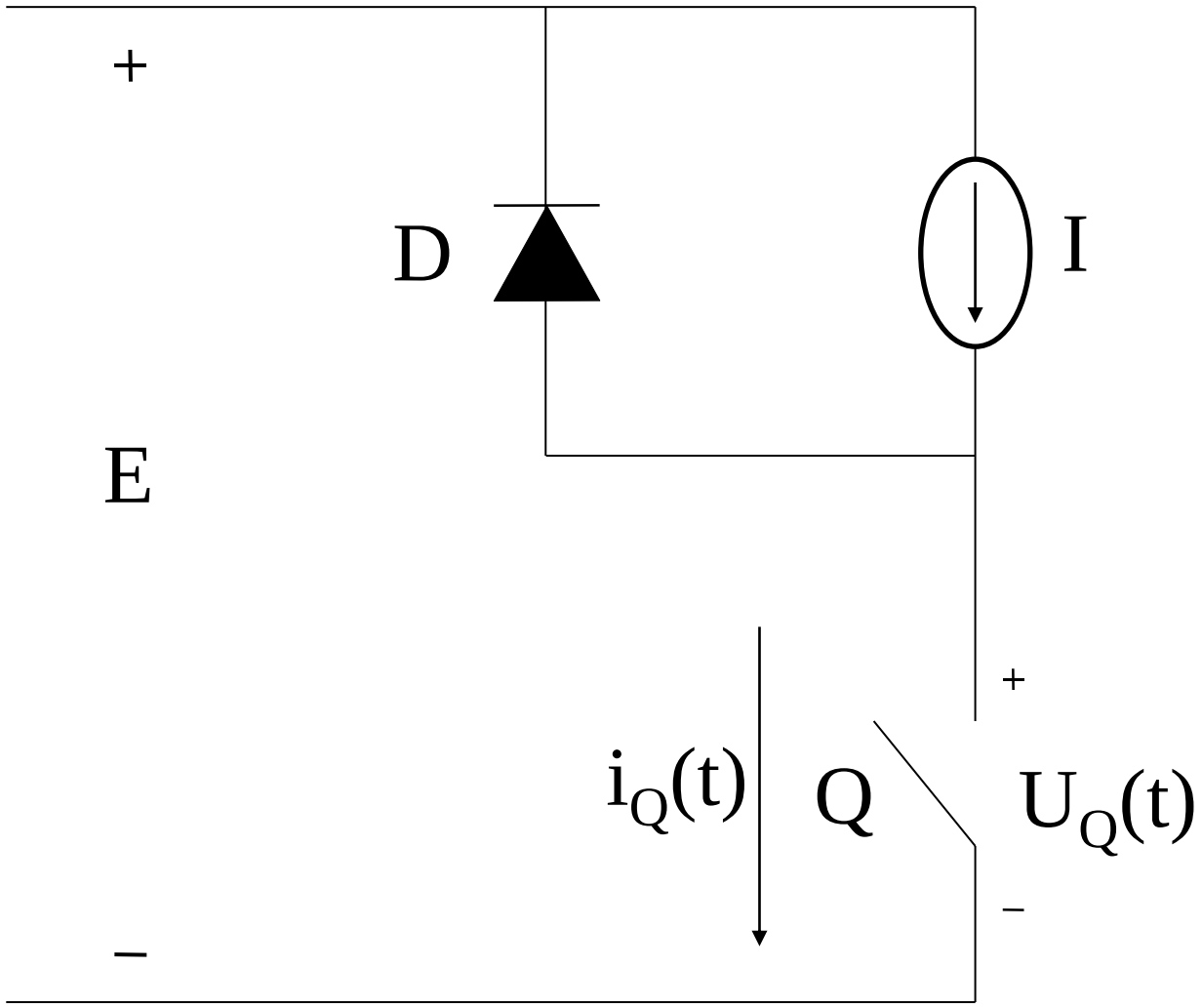
Clamp inductive load
Carga inductiva “clampeada”

Trayectorias de encendido y apagado

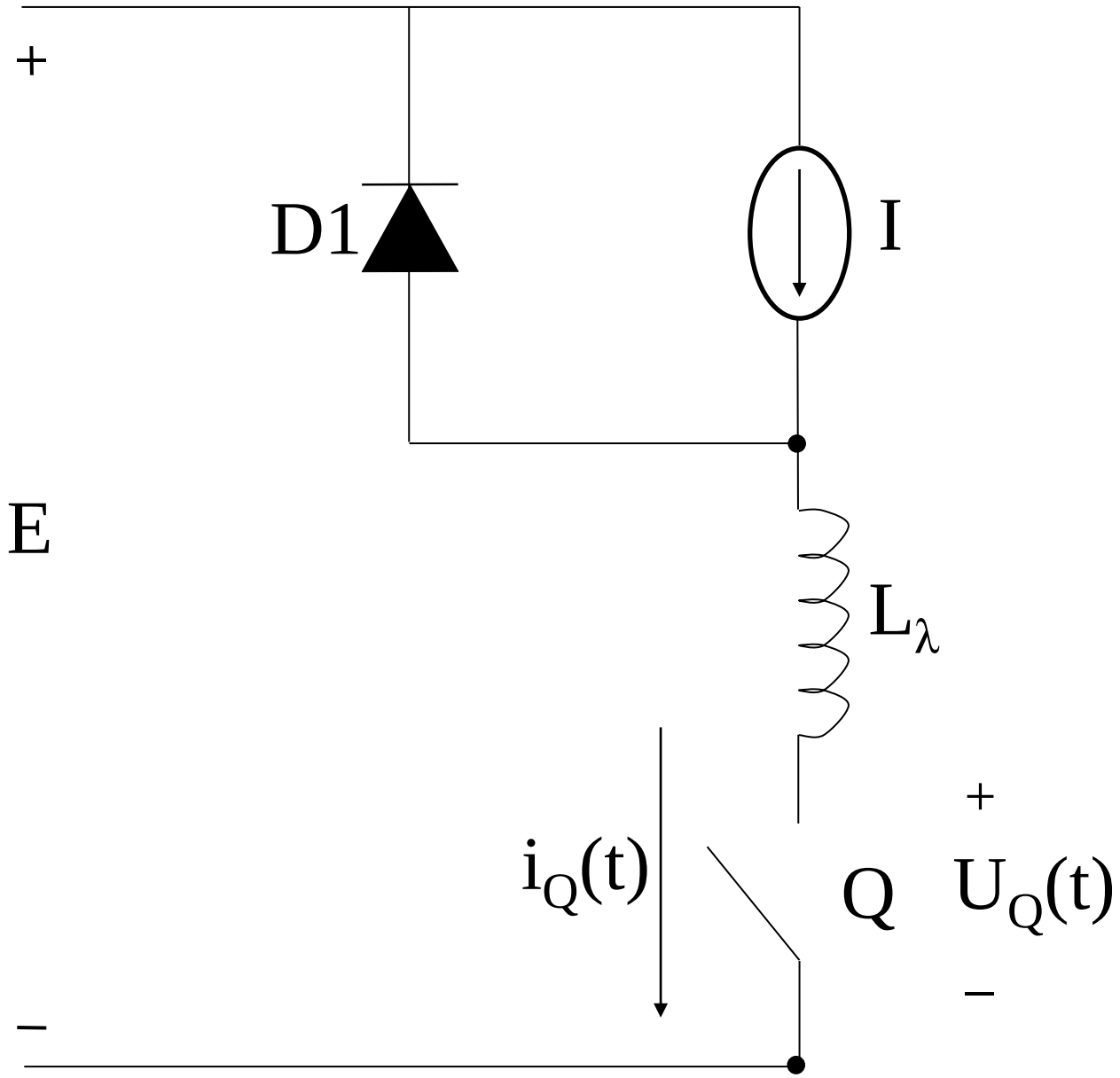


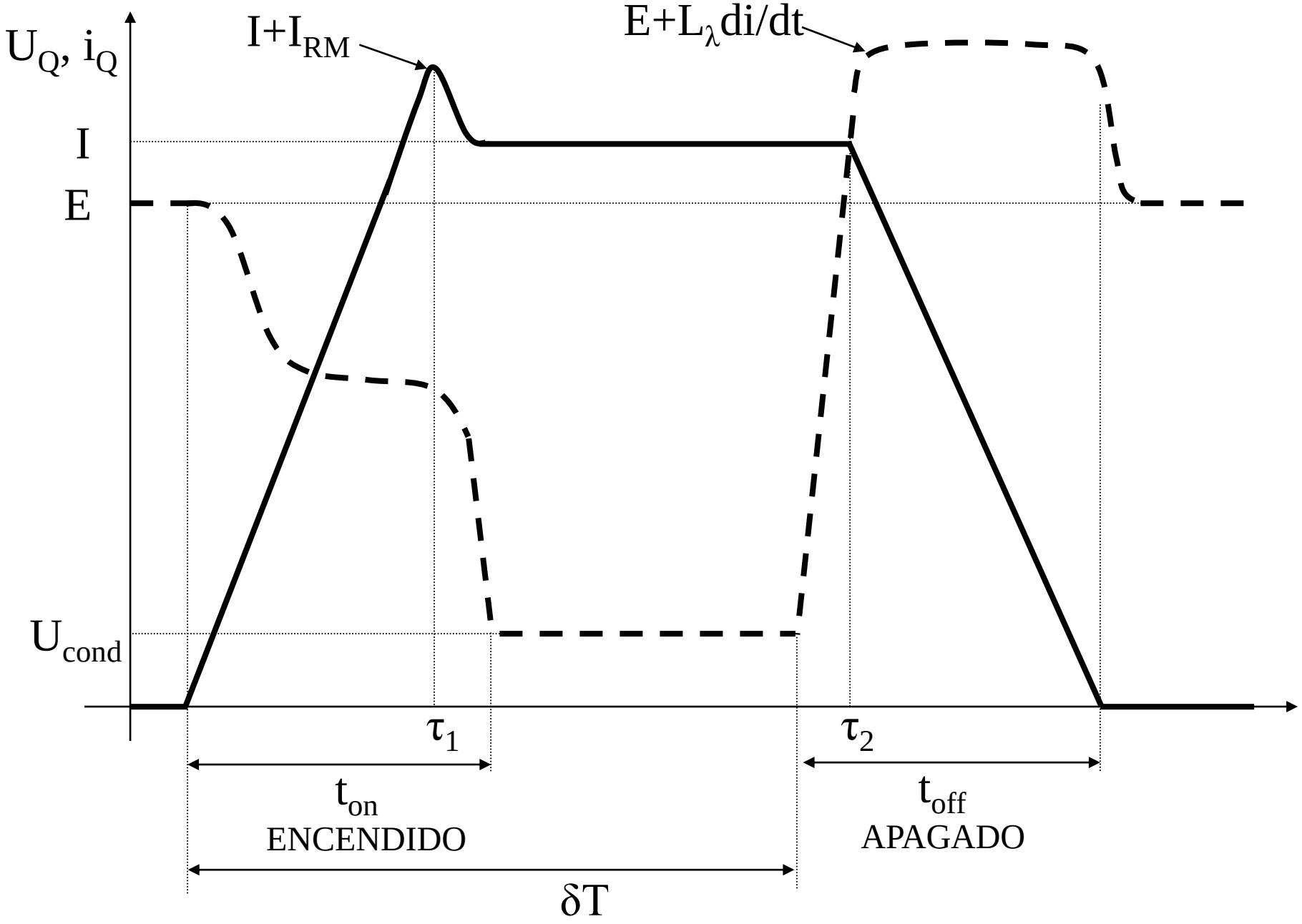

SOA
i_Q
carga inductiva
clampeada
ON
encendido
I
apagado
apagado
encendido
SOA
apagado
encendido
carga
resistiva
U_{cond}
OFF
E
U_Q

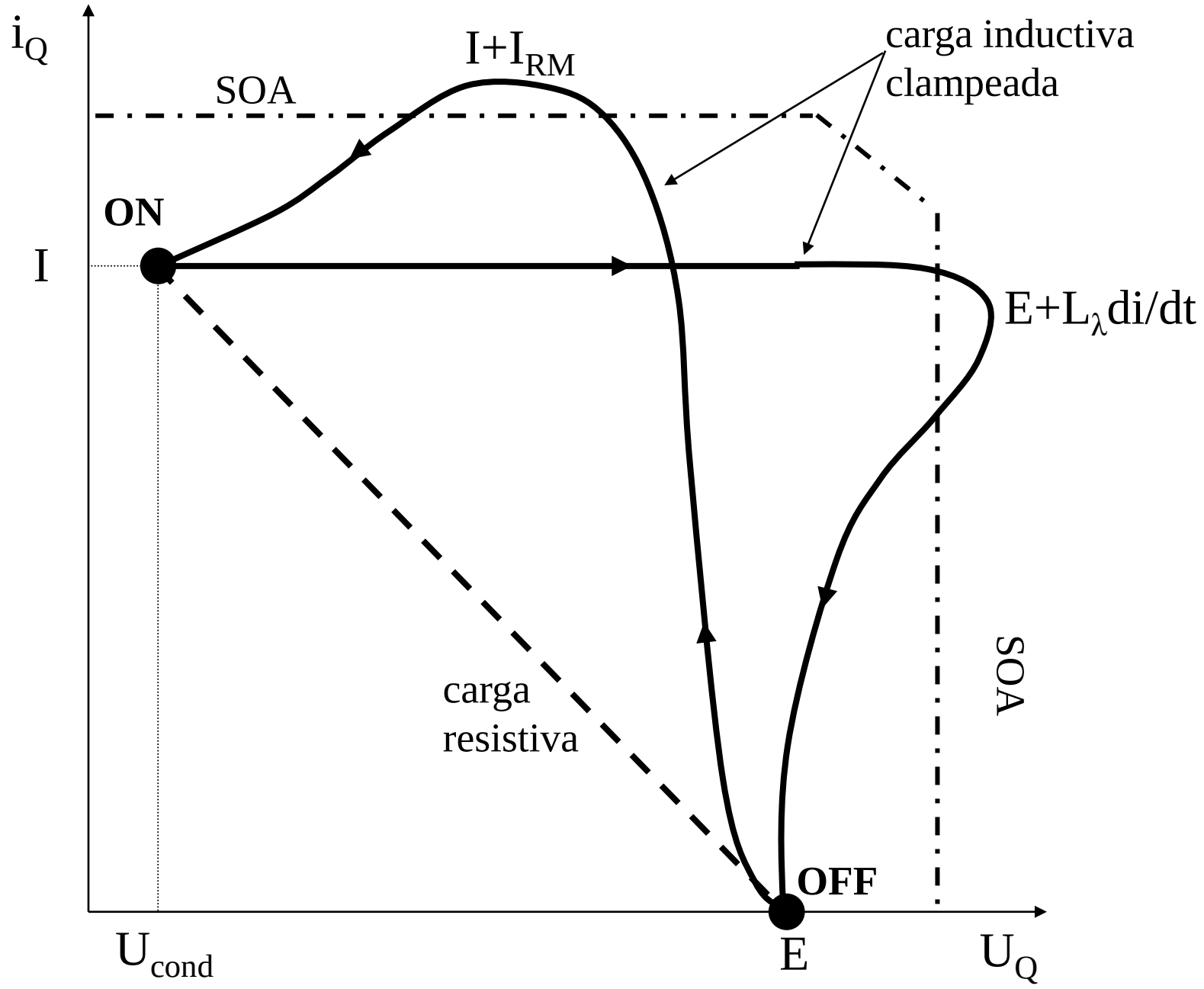
Sobrecorriente en el encendido



Sobretensión en el apagado




U_Q, i_Q
$I+I_{RM}$
$E+L_\lambda di/dt$
I
E
U_{cond}
τ_1
τ_2
t_{on}
ENCENDIDO
t_{off}
APAGADO
δT

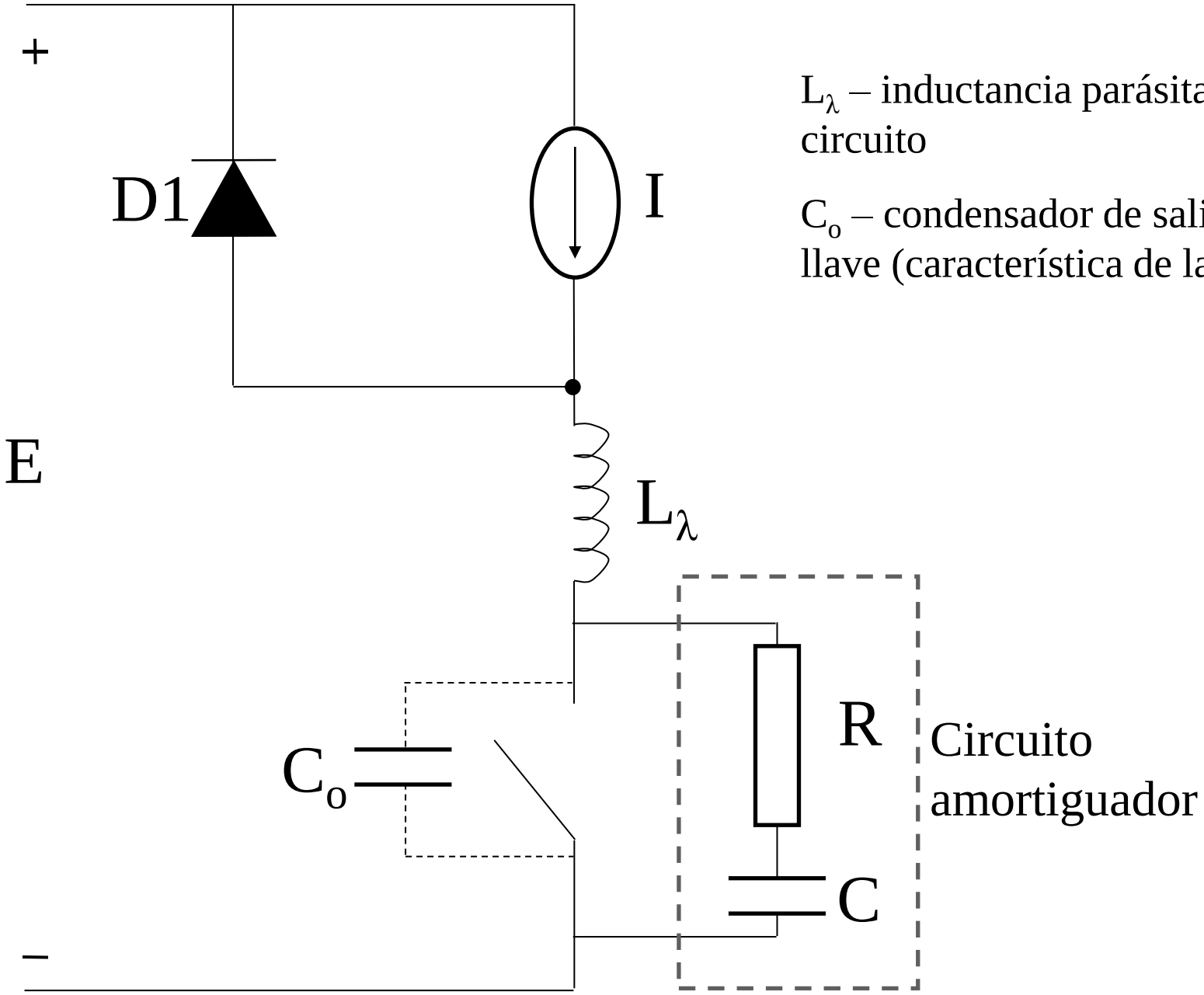

i_Q
$I+I_{RM}$
SOA
carga inductiva
clampeada
ON
I
$E+L_\lambda di/dt$
carga
resistiva
SOA
OFF
U_{cond}
E
U_Q

Circuitos de ayuda a la conmutación – “snubbers”

4 tipos básicos:

1) Amortiguador de oscilaciones
2) Snubber de encendido
3) Clamp de tensión
4) Snubber de apagado

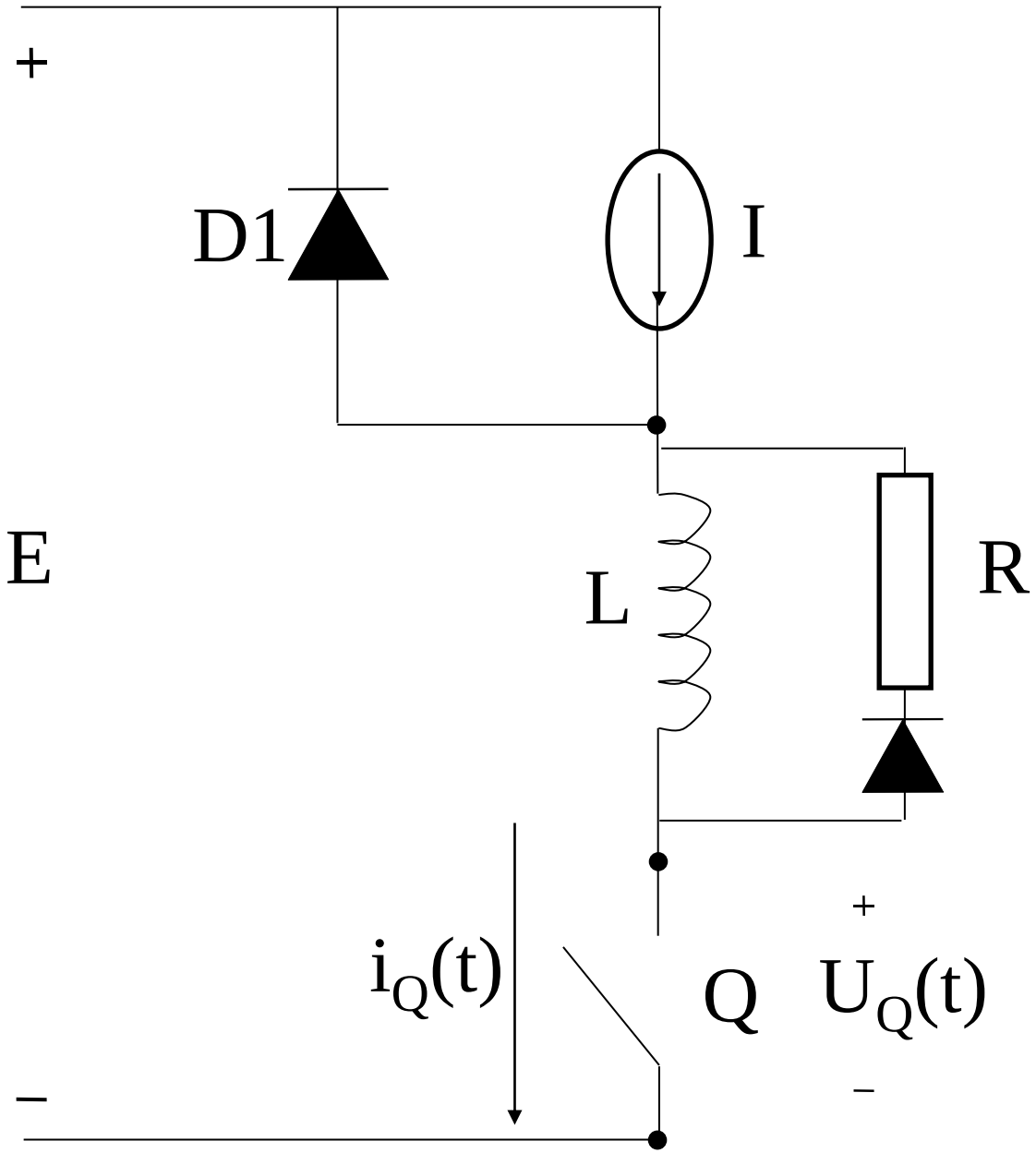
1) Amortiguador de oscilaciones

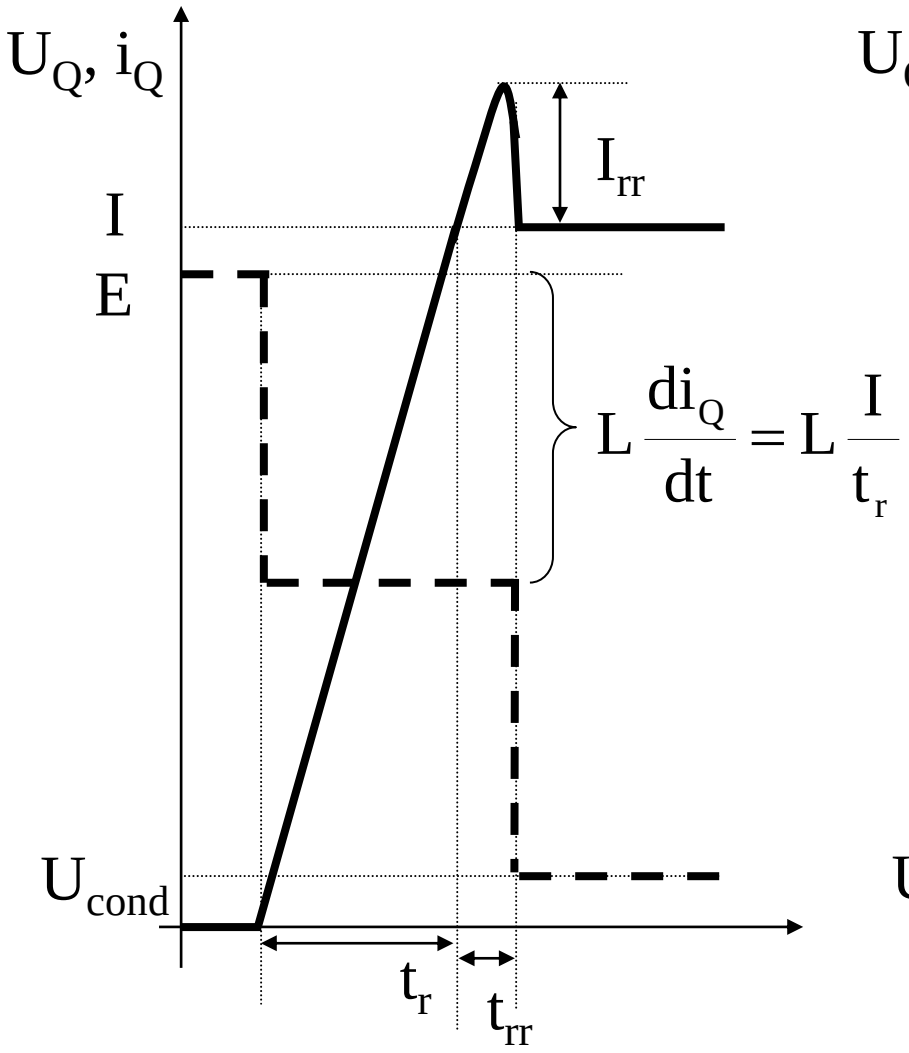


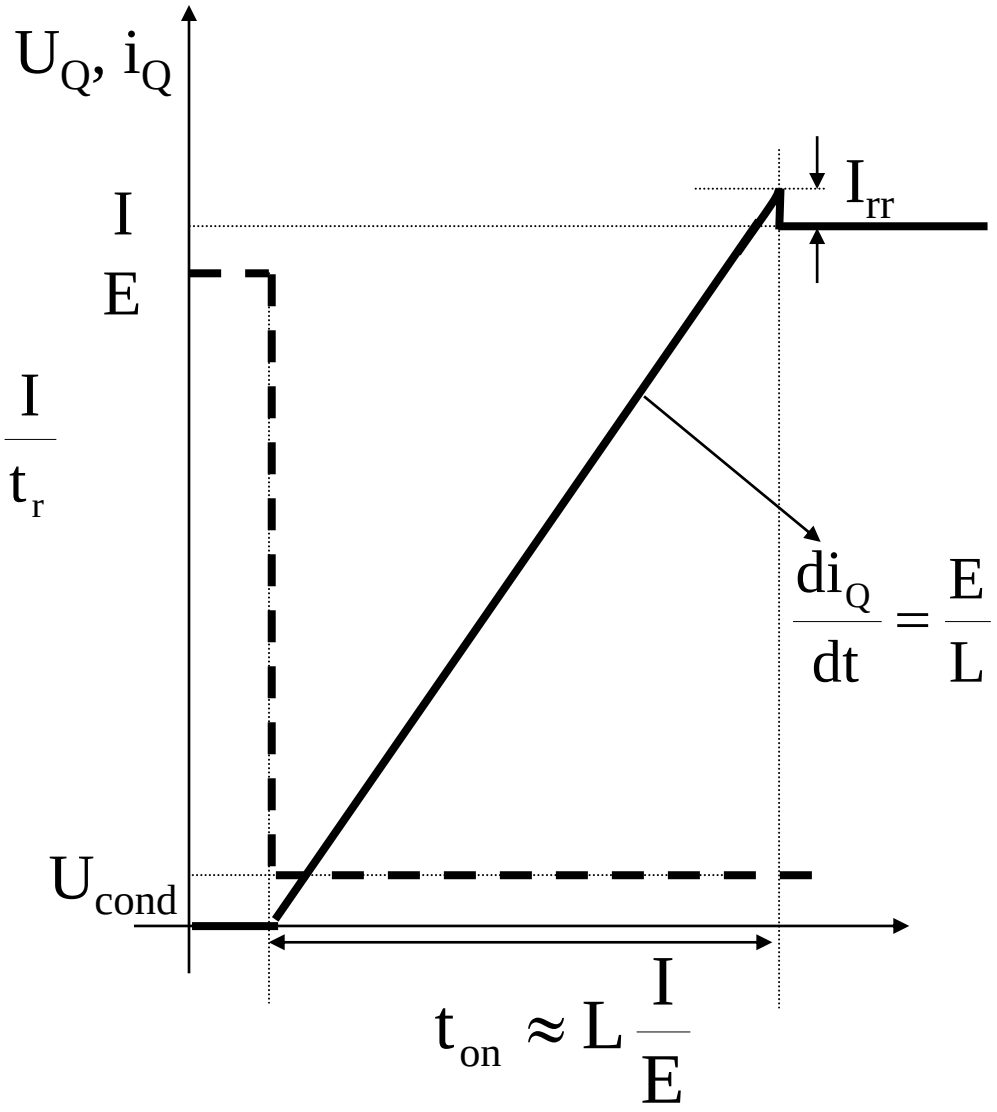
L_λ – inductancia parásita del circuito

C_o – condensador de salida de la llave (característica de la llave)

2) Circuito de ayuda al encendido – Turn-on snubber

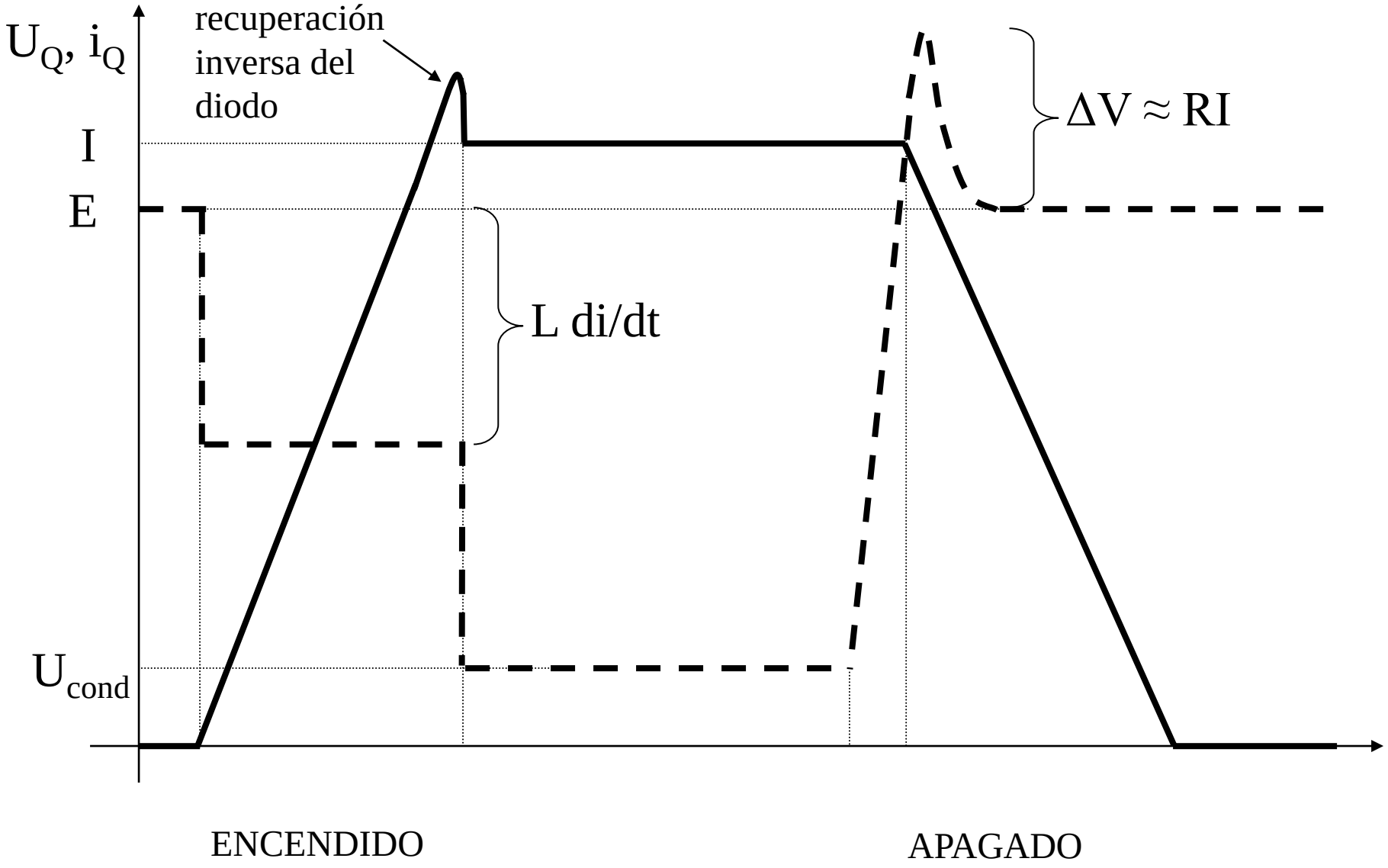


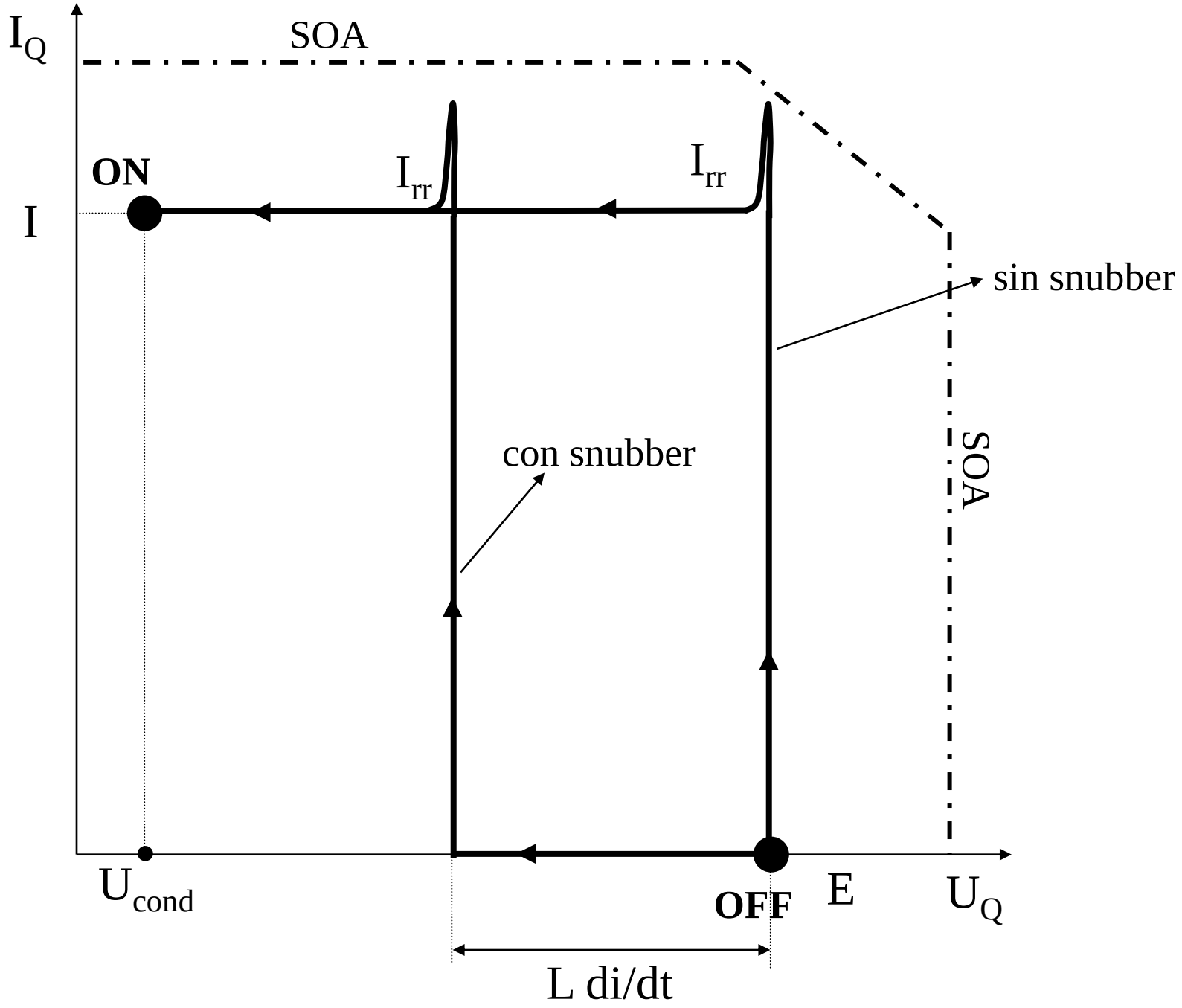




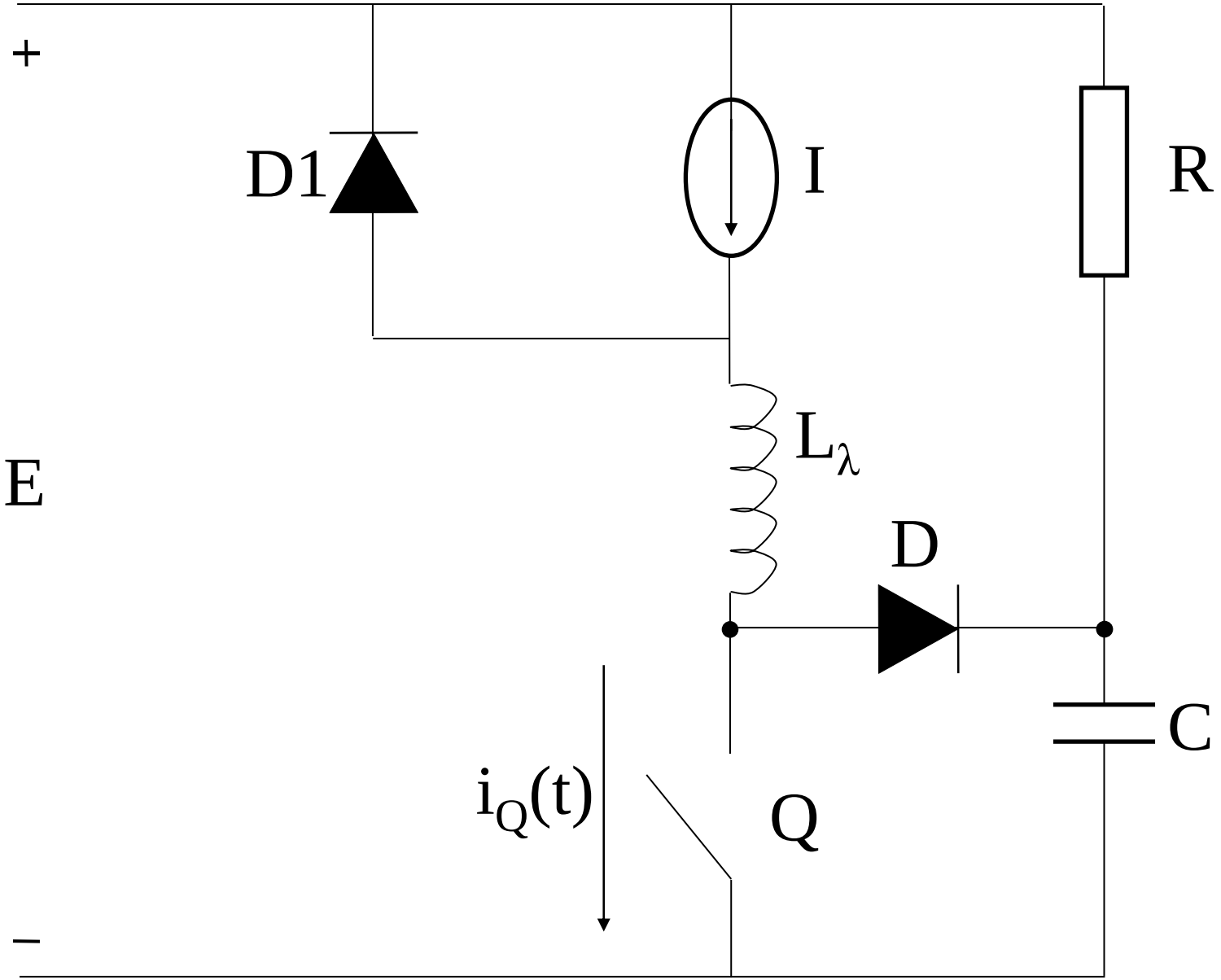
a) $L < \frac{E * t_r}{I}$

b) $L > \frac{E * t_r}{I}$

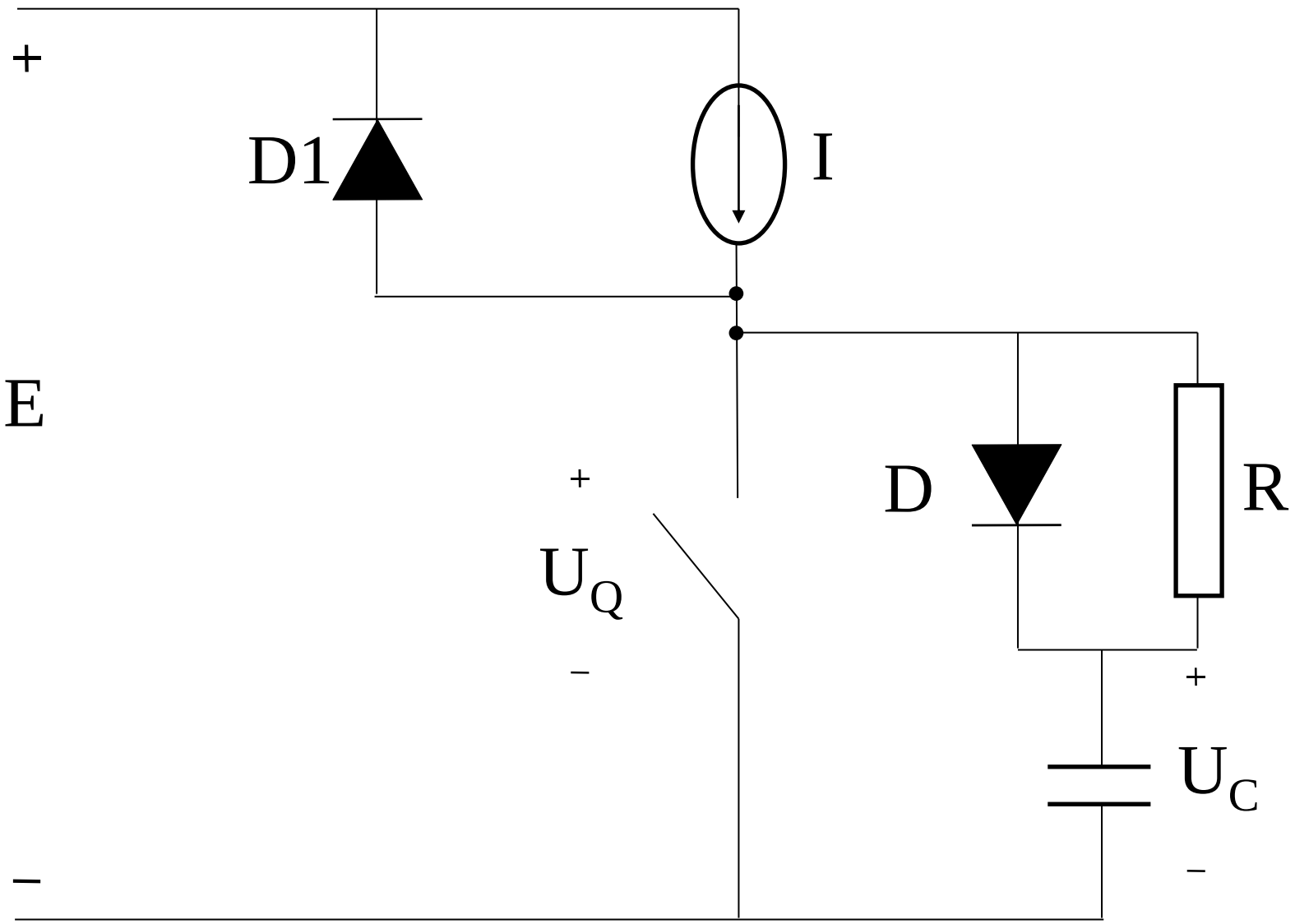

U_Q, i_Q
recuperación inversa del diodo
I
E
L di/dt
ΔV ≈ RI
U_{cond}
ENCENDIDO
APAGADO

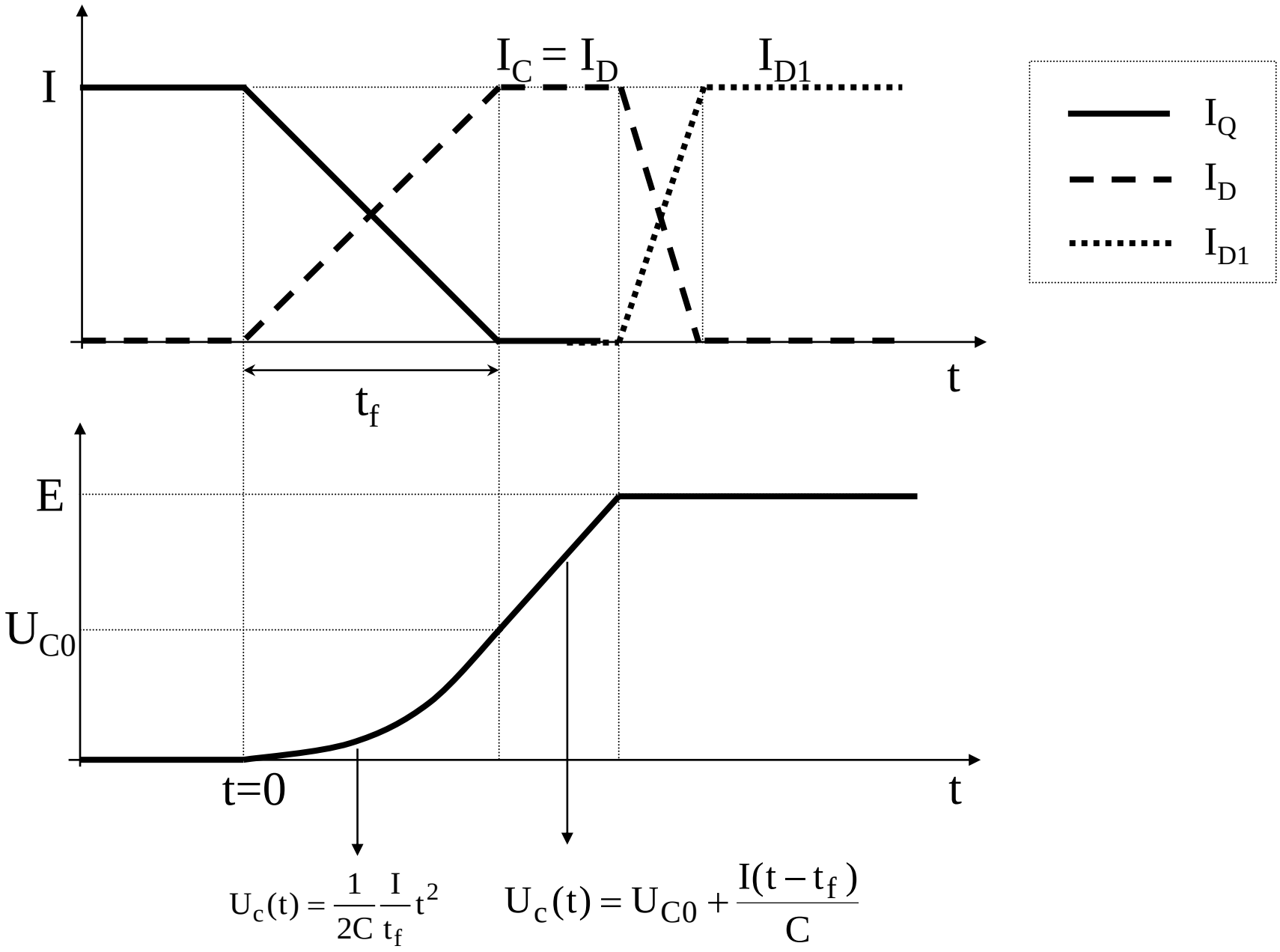

I_Q
SOA
ON
I
I_{rr}
I_{rr}
sin snubber
con snubber
SOA
U_{cond}
OFF
E
U_Q
L di/dt

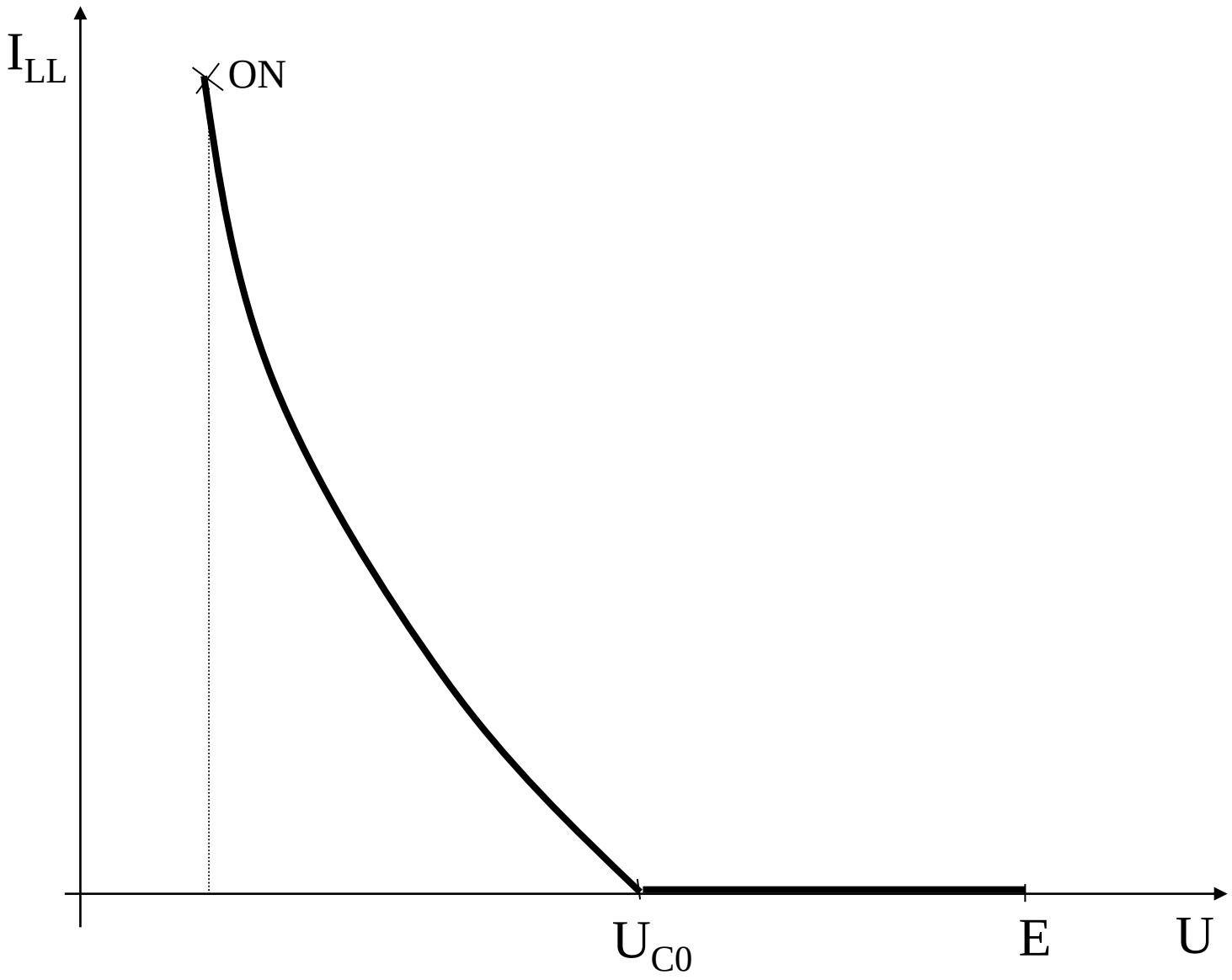
3) Circuito limitador de sobretensión – Clamp de sobretensión

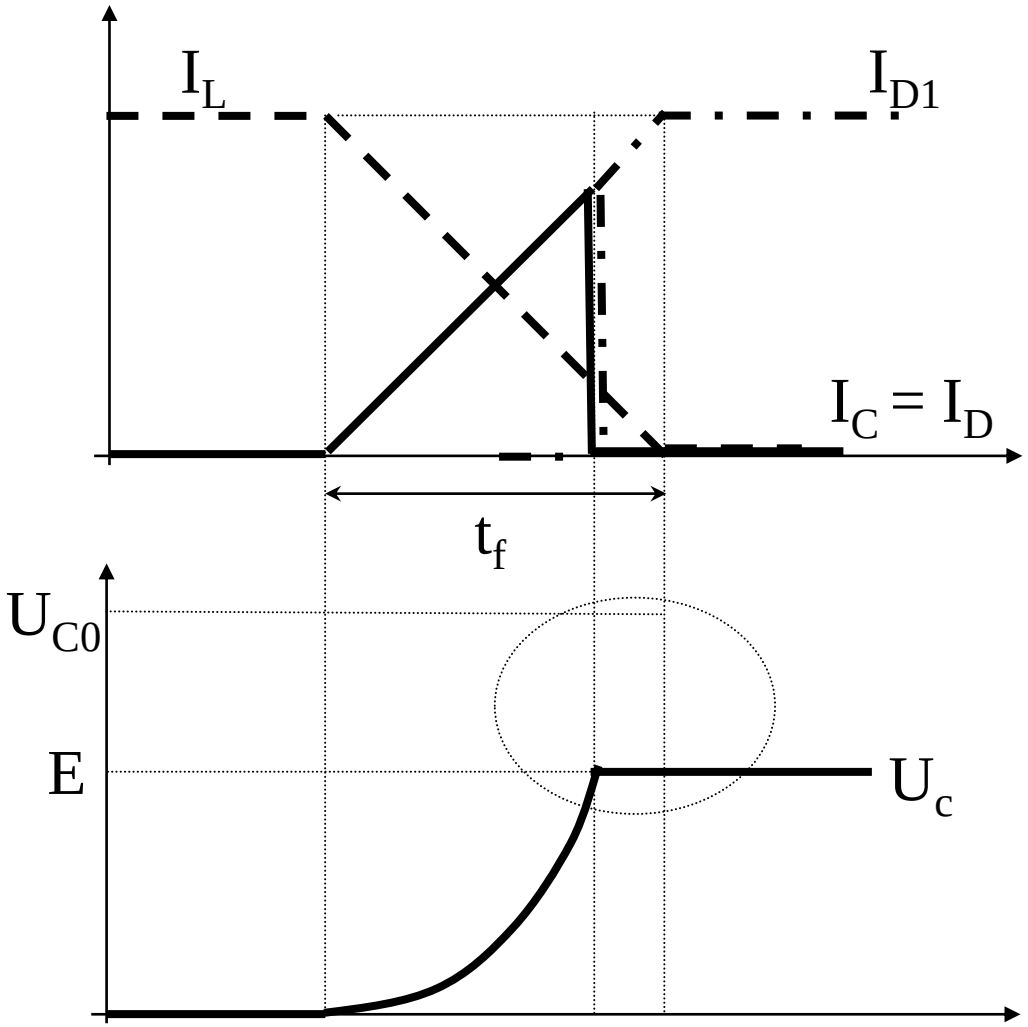


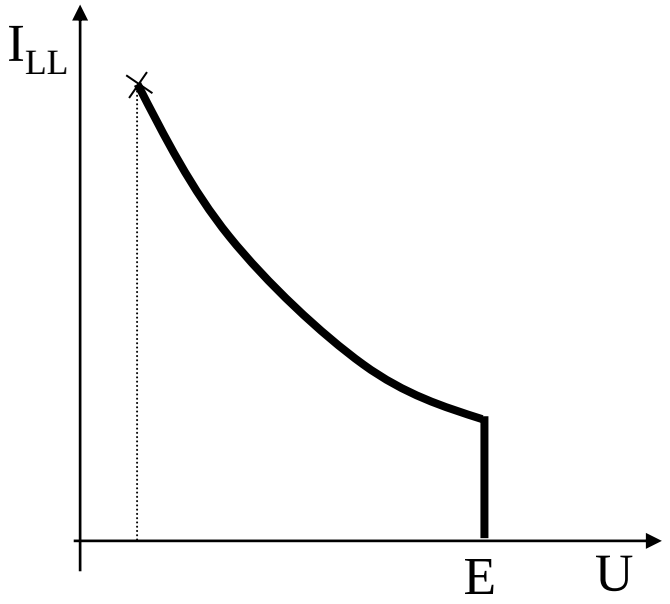
4) Circuito de ayuda al apagado - Snubber de apagado

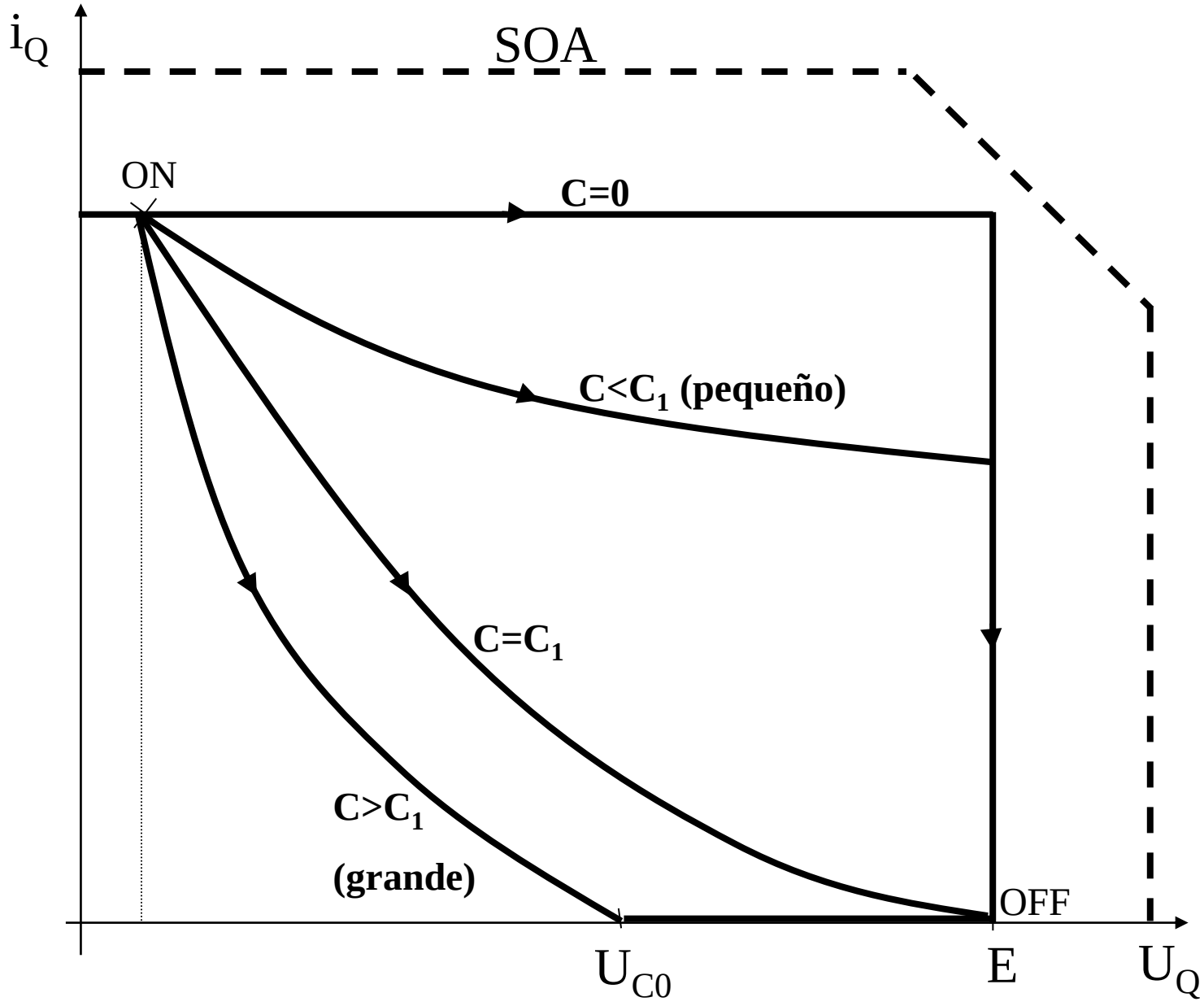


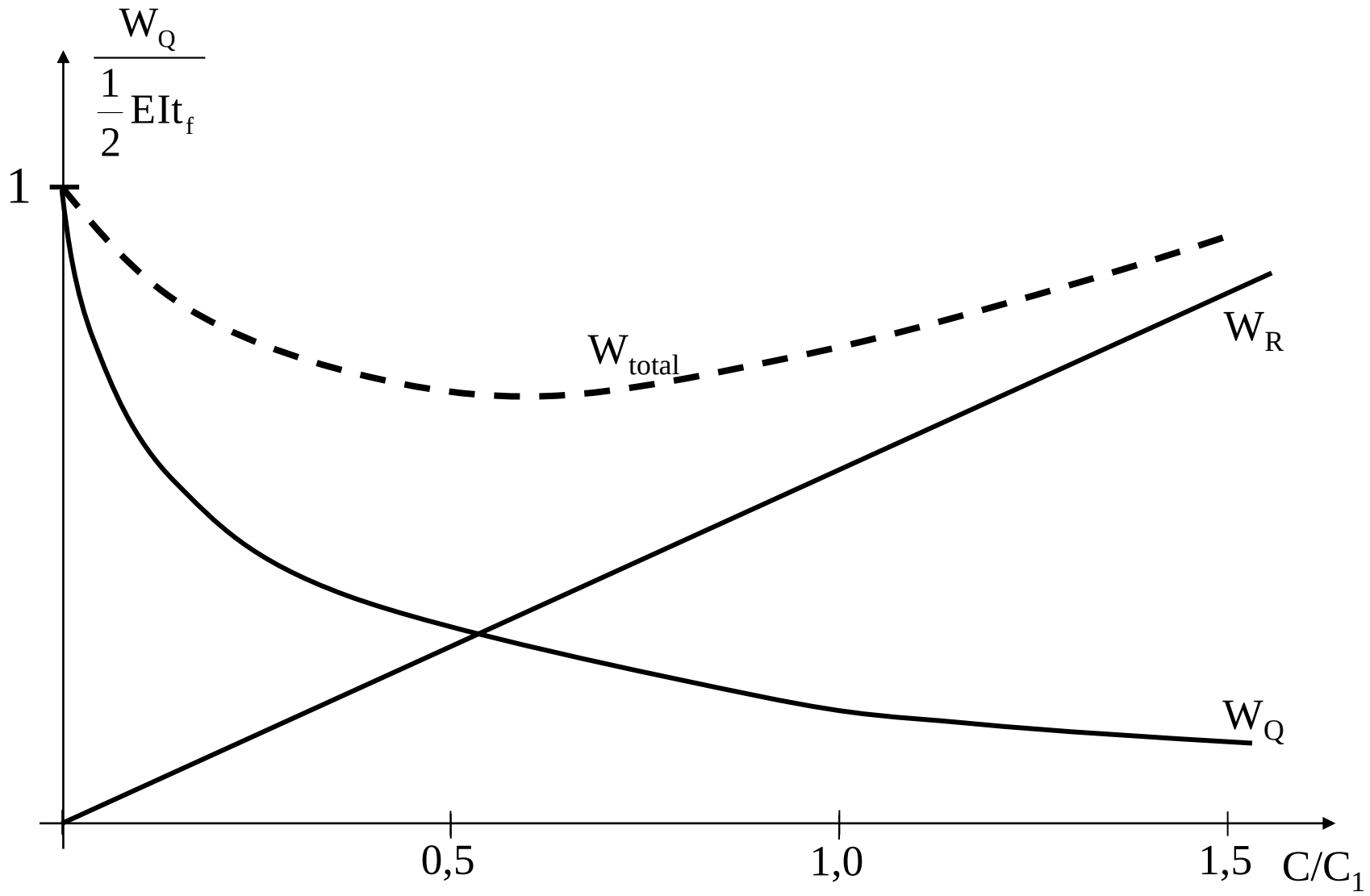

I
$I_C = I_D$
I_{D1}
t
t_f
E
U_{C0}
t=0
t
I_Q
I_D
I_{D1}
$U_c(t) = \frac{1}{2C}\frac{I}{t_f}t^2$
$U_c(t) = U_{C0} + \frac{I(t - t_f)}{C}$


I_{LL}
ON
U_{C0}
E
U


I_L
I_{D1}
$I_C = I_D$
t_f
U_{C0}
E
U_c


I_{LL}
E
U


i_Q
SOA
ON
C=0
C<C1 (pequeño)
C=C1
C>C1
(grande)
OFF
UC0
E
UQ

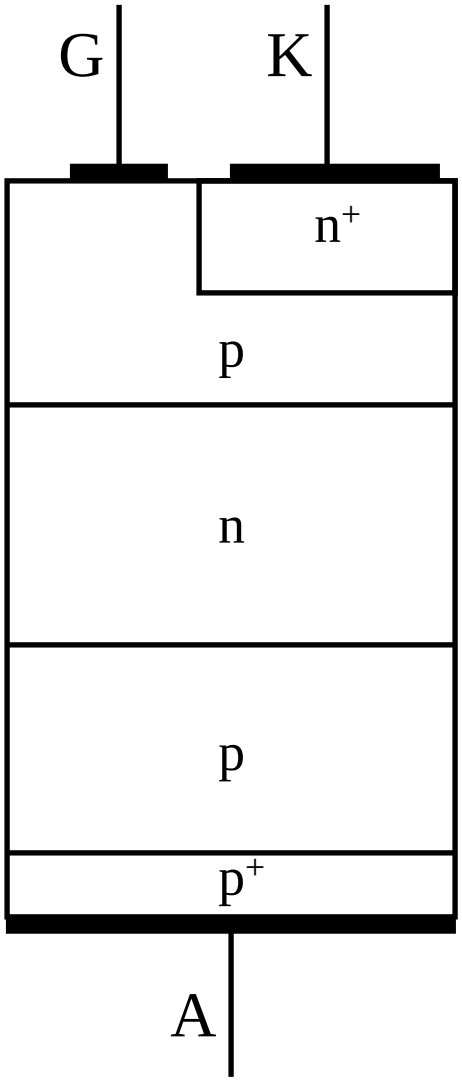


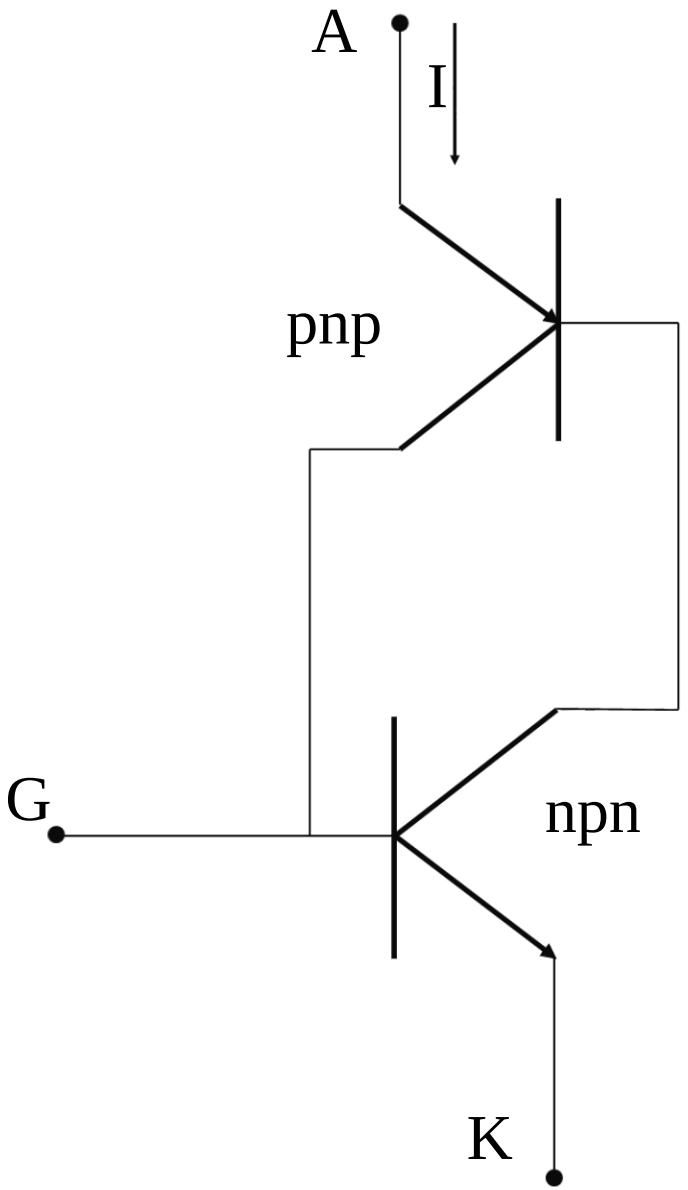
W_Q = Energía disipada en el apagado de la llave

W_R = Energía disipada en la resistencia del snubber

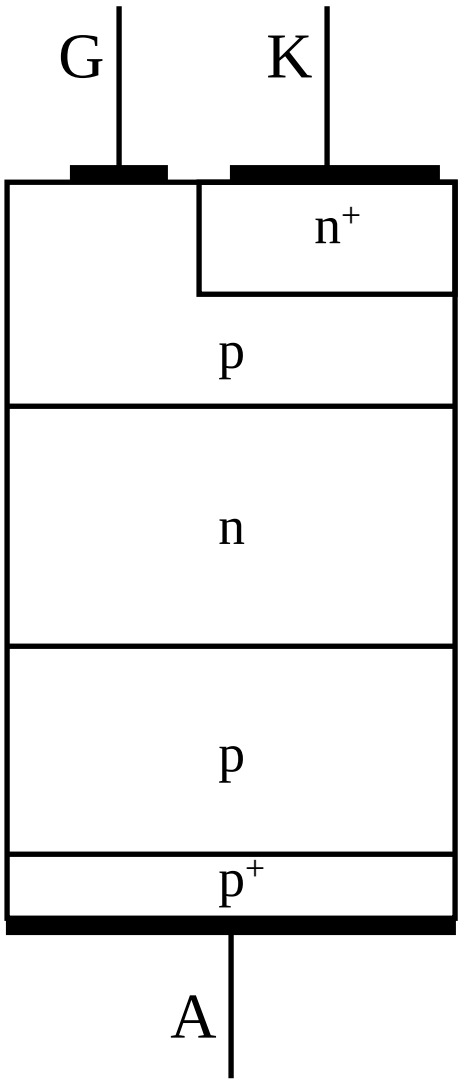
ESTRUCTURAS DE POTENCIA

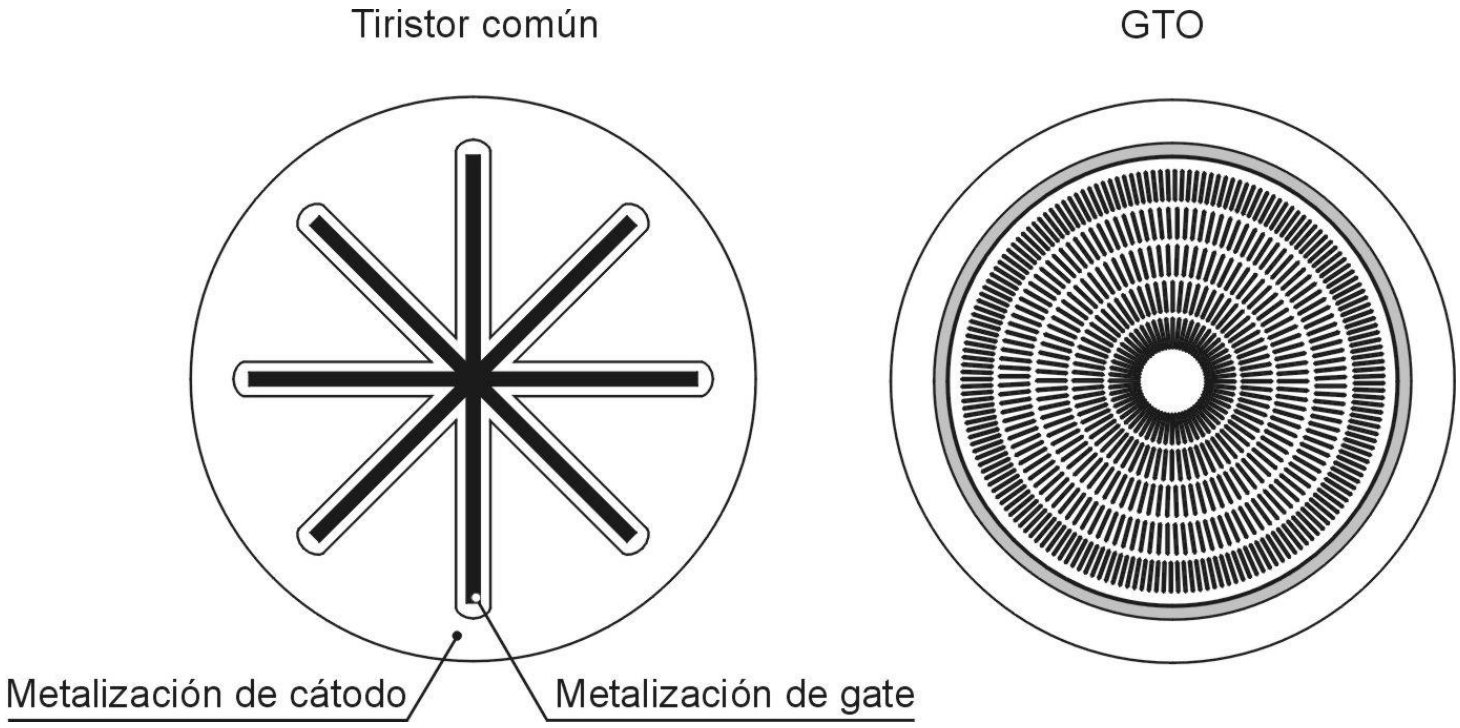
TIRISTOR

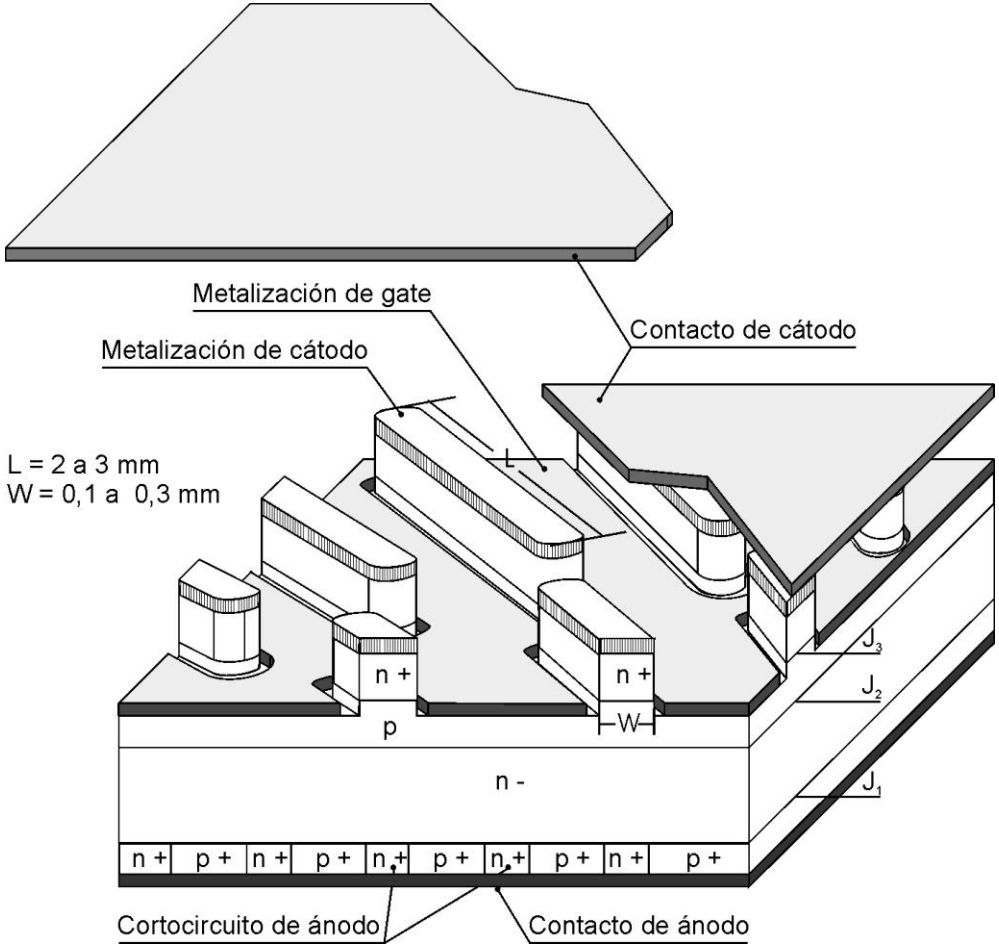


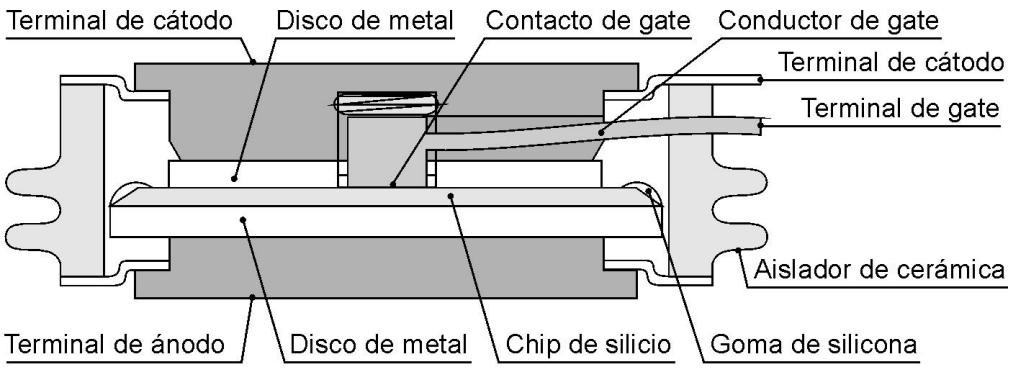


GTO

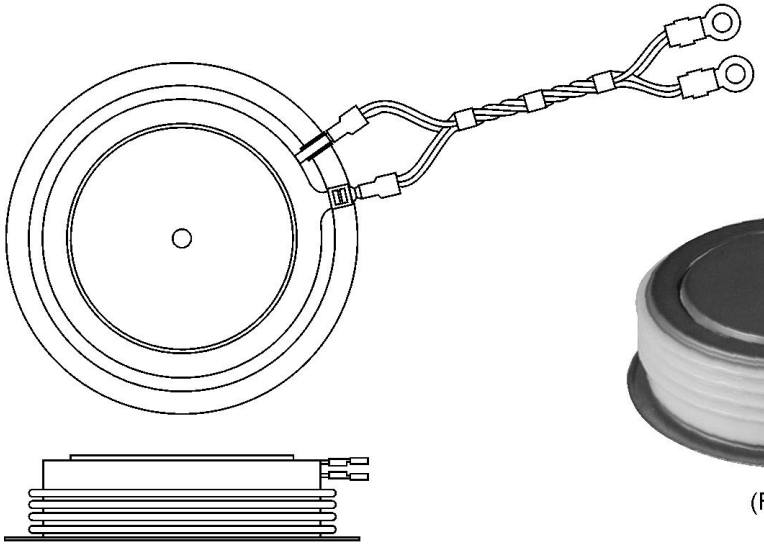



Tiristor común
GTO
Metalización de cátodo
Metalización de gate


Metalización de gate
Contacto de cátodo
Metalización de cátodo
L = 2 a 3 mm
W = 0,1 a 0,3 mm
L
n +
n +
W
p
n -
J3
J2
J1
n + p + n + p + n + p + n + p + n + p +
Cortocircuito de ánodo
Contacto de ánodo



(Fig. a)



(Fig. b)

(Fig. c)

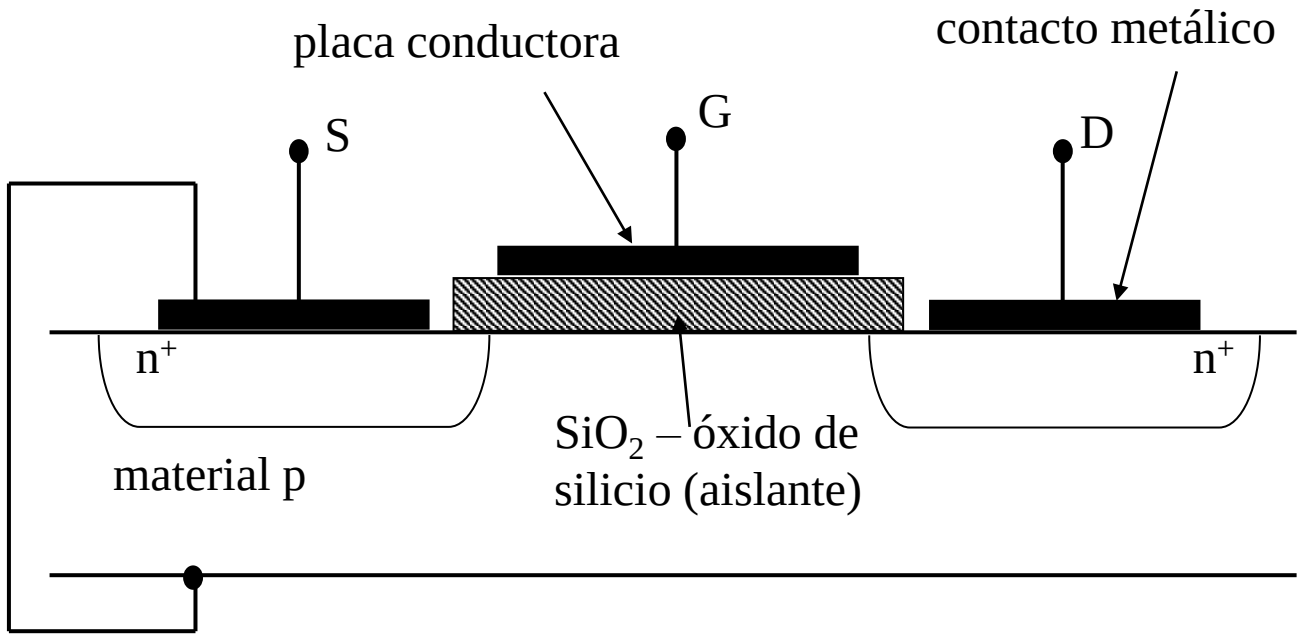
BJT

MOSFET

S = source

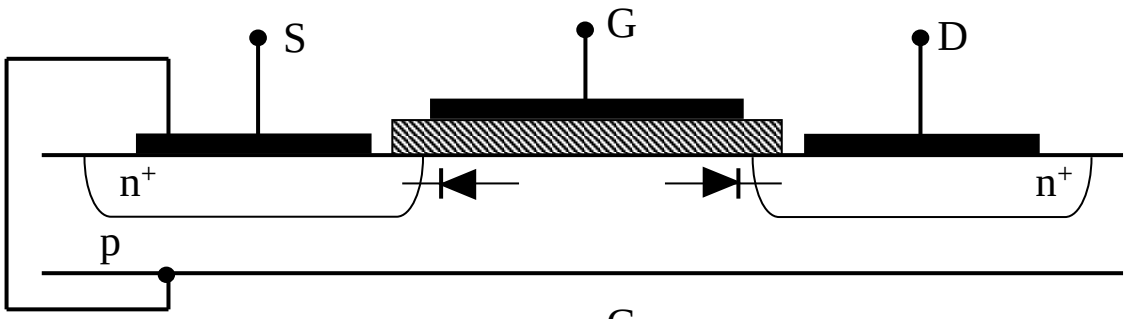
G = gate

D = drain



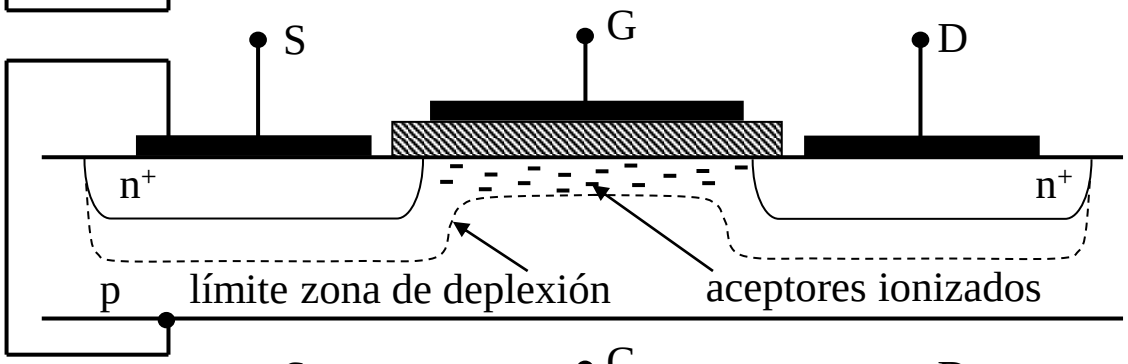
Bloqueo directo

$U_{GS}=0$



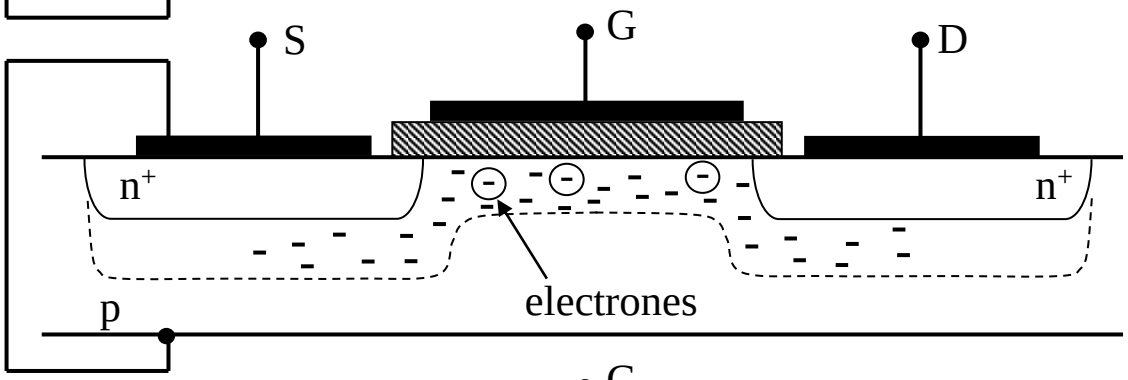
$U_{GS1}>0$

formación de zona de deplexión



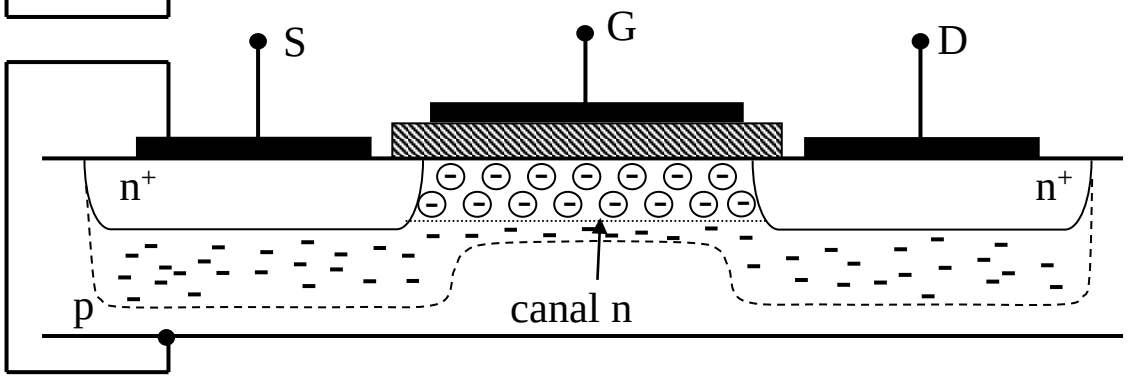
$U_{GS2}>U_{GS2}$

atracción de electrones libres



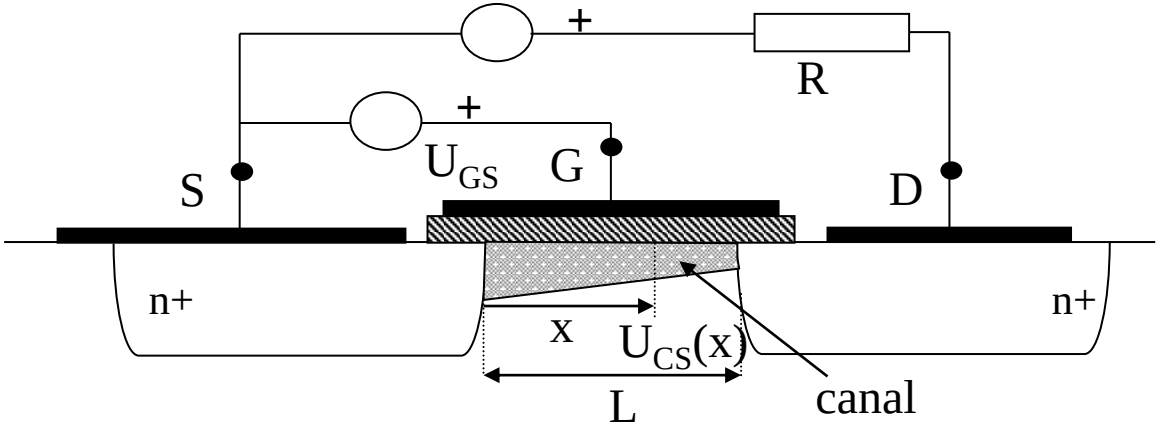
$U_{GS}>U_{GS(th)}$

formación de la zona de inversión (canal n)

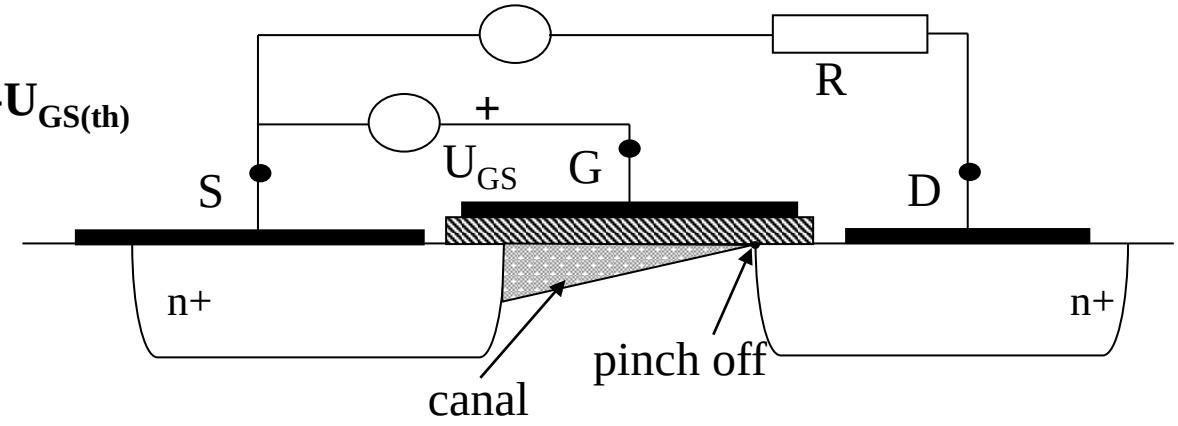


$U_{DS}<U_{GS}-U_{GS(th)}$

zona lineal o resistiva

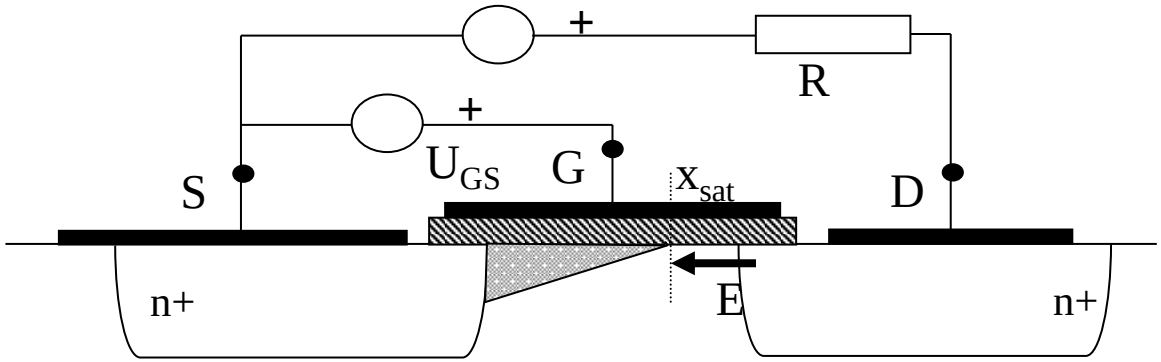


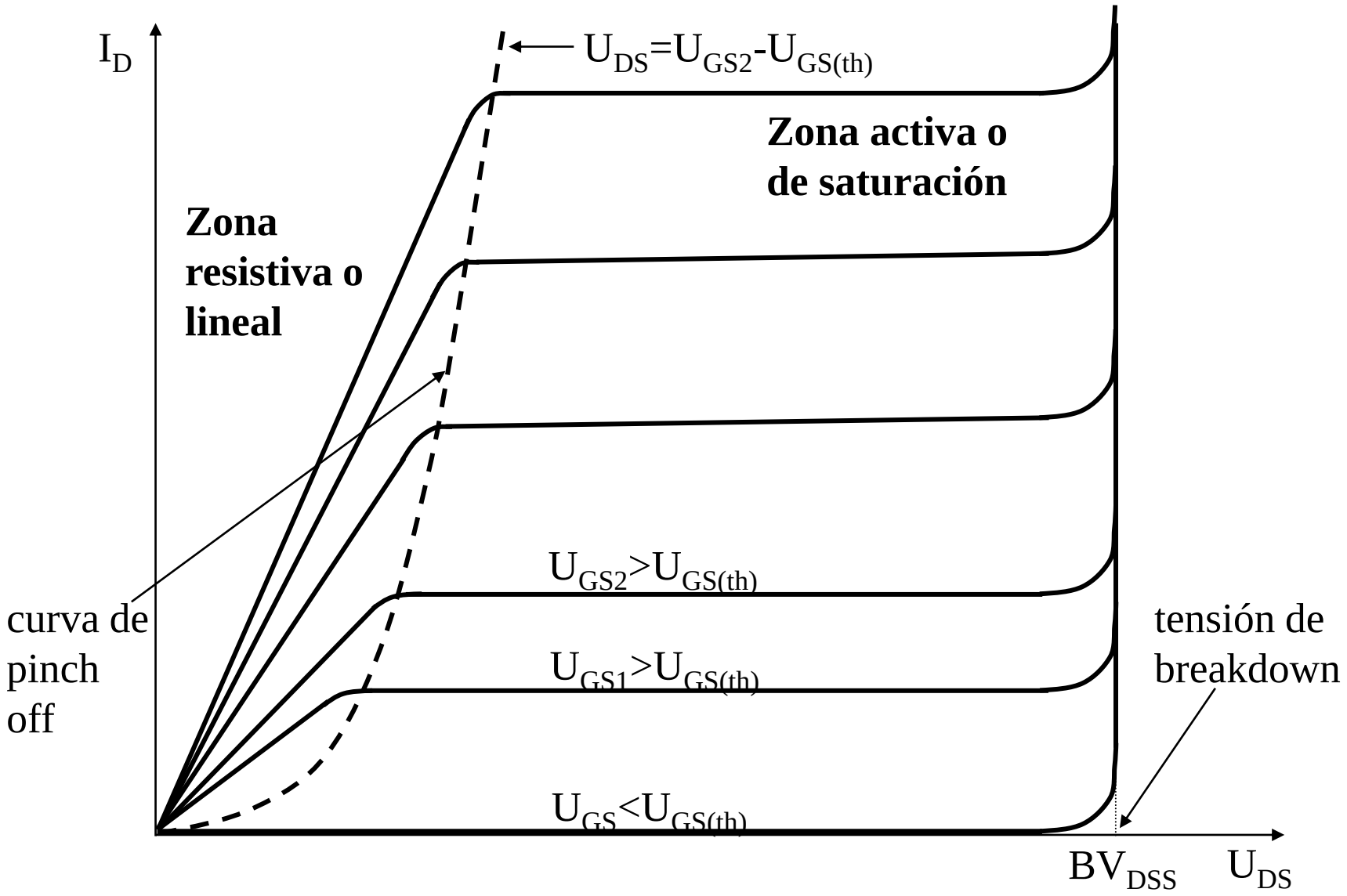
$U_{CS}(L) = U_{DS} = U_{GS} - U_{GS(th)}$

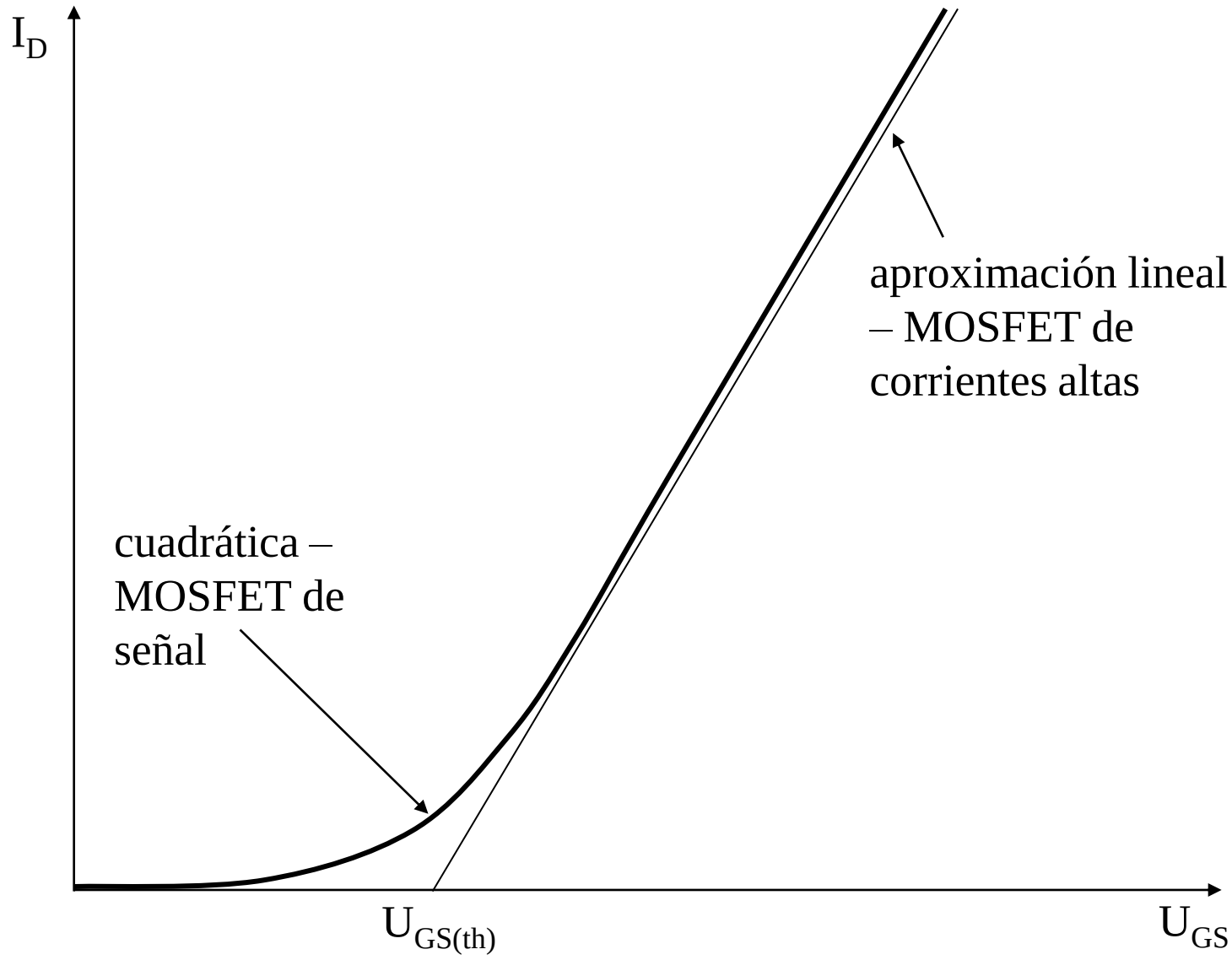


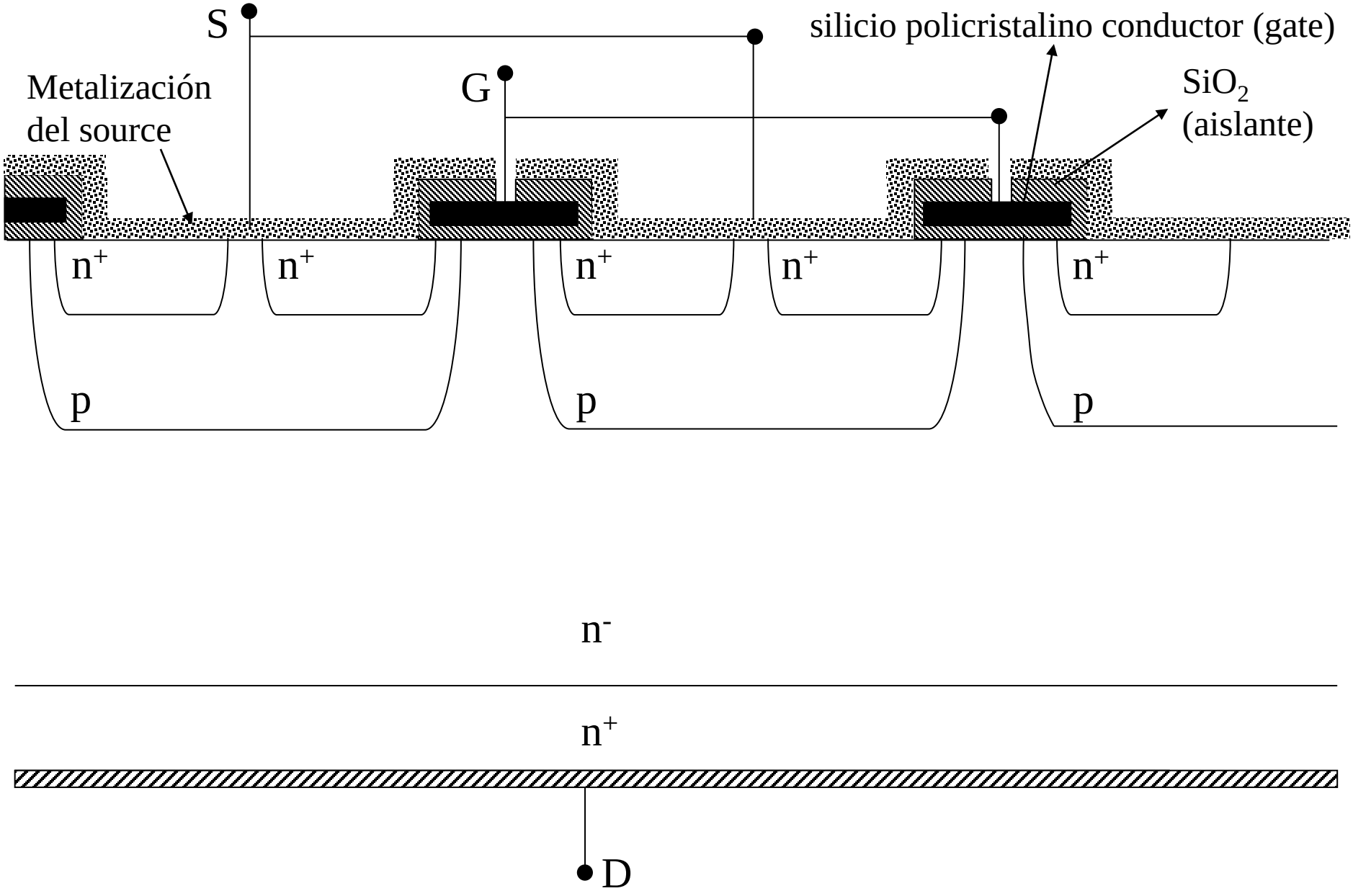
$U_{DS}>U_{GS}-U_{GS(th)}$

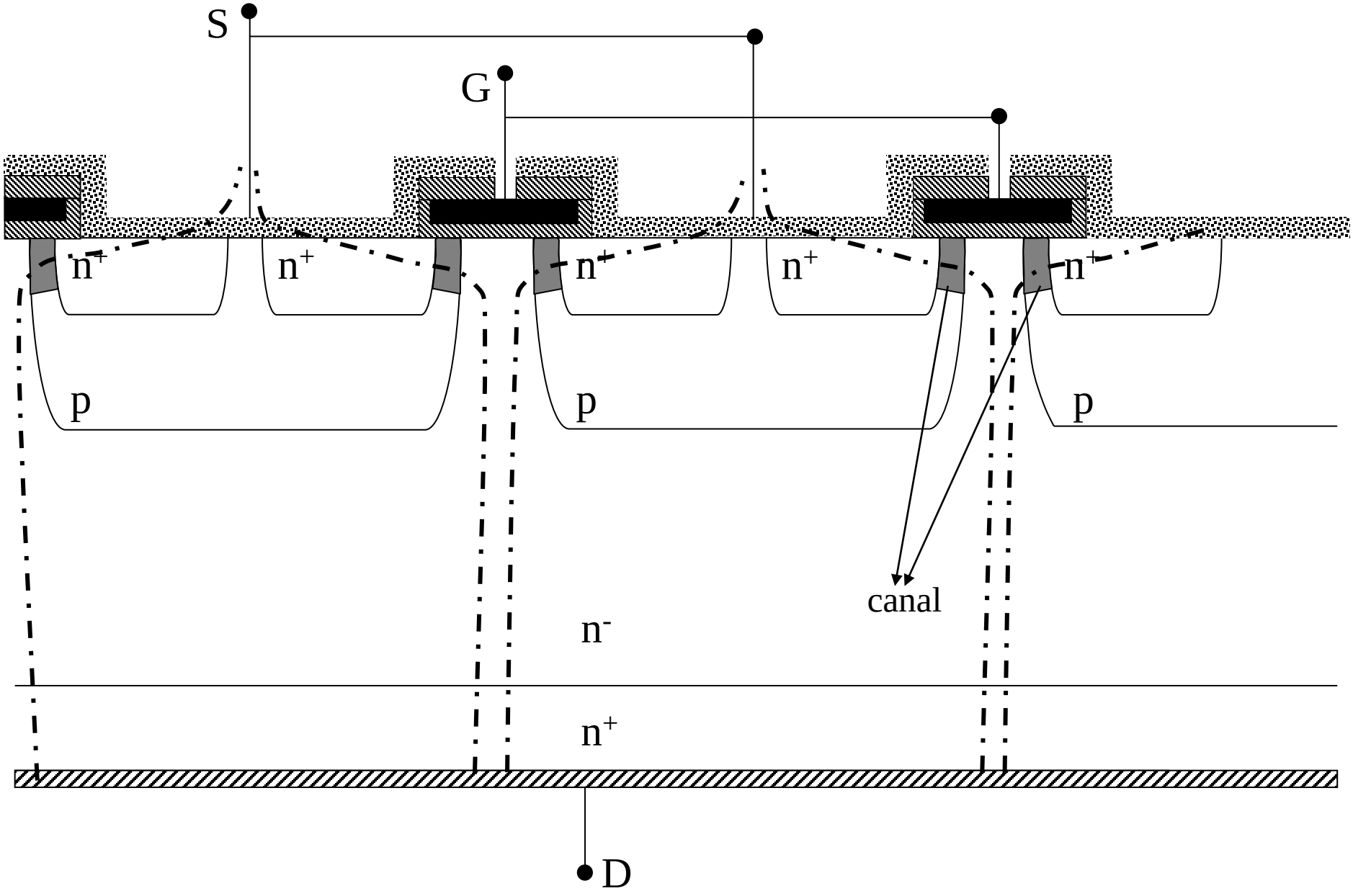
zona activa o de saturación



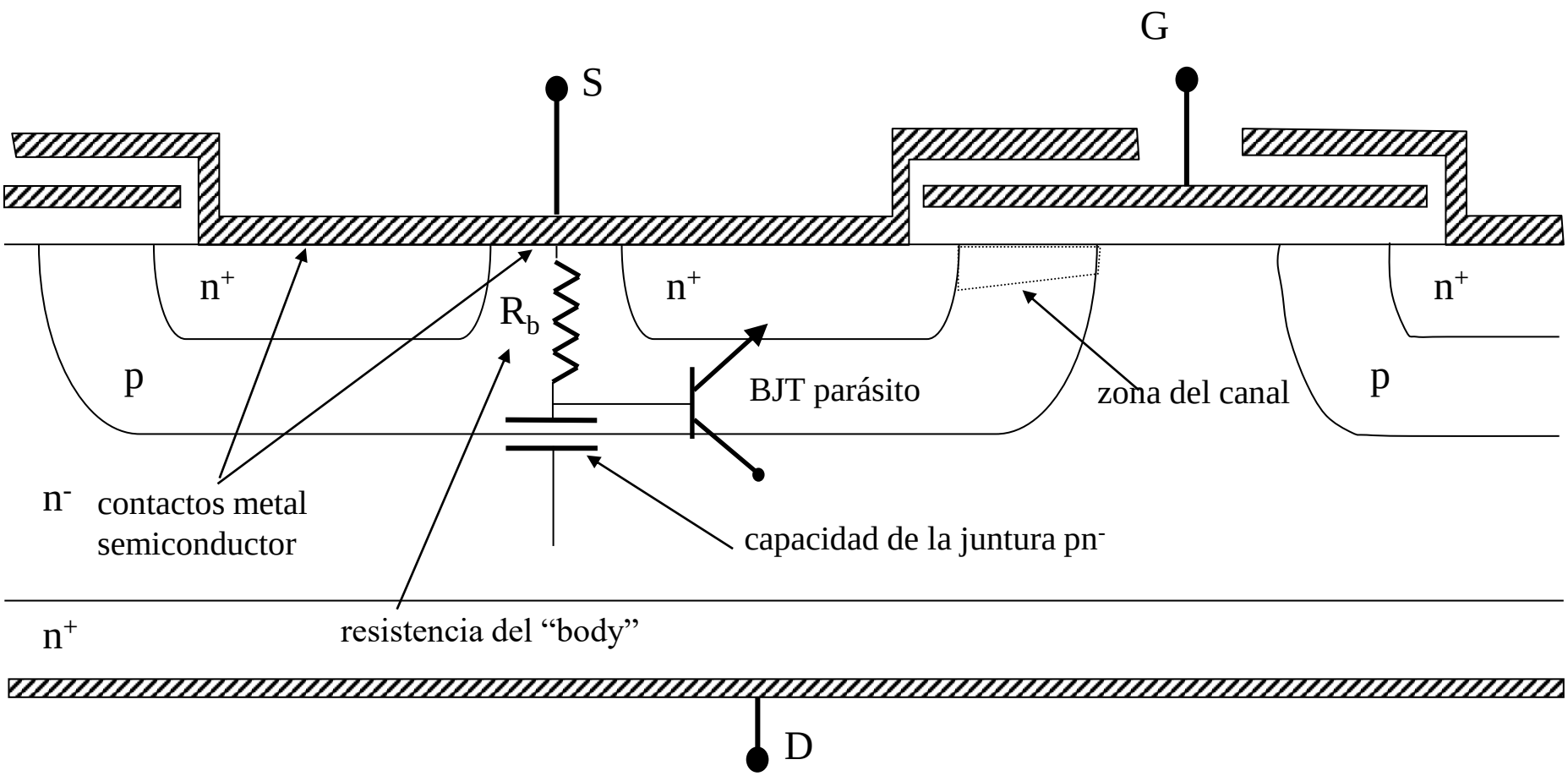

I_D
$U_{DS}=U_{GS2}-U_{GS(th)}$
Zona activa o de saturación
Zona resistiva o lineal
$U_{GS2}>U_{GS(th)}$
$U_{GS1}>U_{GS(th)}$
$U_{GS}<U_{GS(th)}$
curva de pinch off
tensión de breakdown
BV_{DSS}
U_{DS}


I_D
aproximación lineal – MOSFET de corrientes altas
cuadrática – MOSFET de señal
$U_{GS(th)}$
U_{GS}

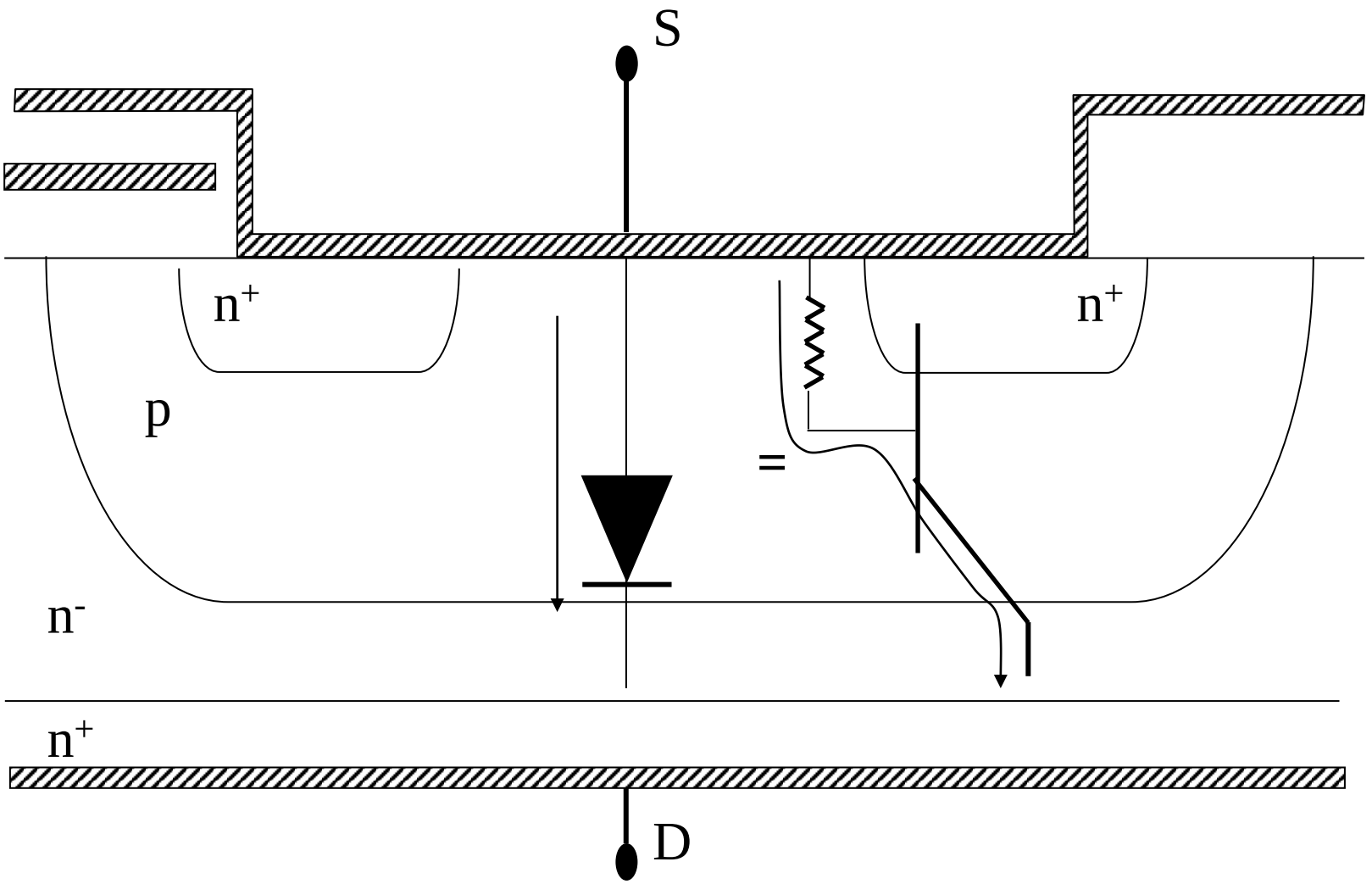

S
G
silicio policristalino conductor (gate)
Metalización
del source
SiO2
(aislante)
n+
n+
n+
n+
n+
p
p
p
n-
n+
D

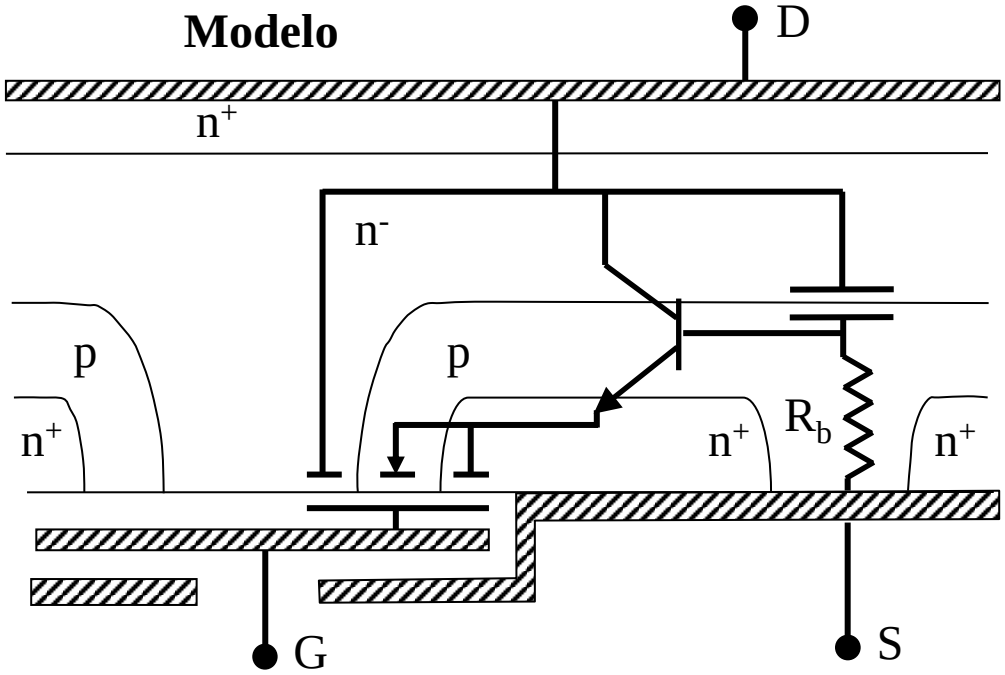

S
G
n+
n+
n+
n+
n+
p
p
p
canal
n-
n+
D

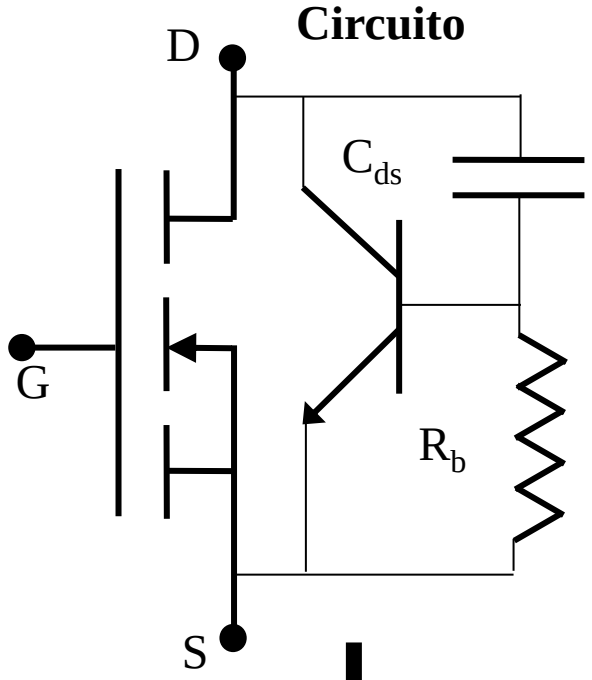
Transistor parásito



Diodo antiparalelo (juntura CB del transistor parásito)

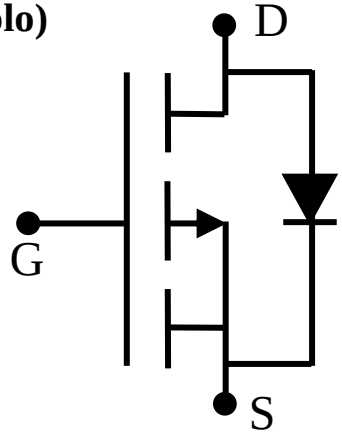






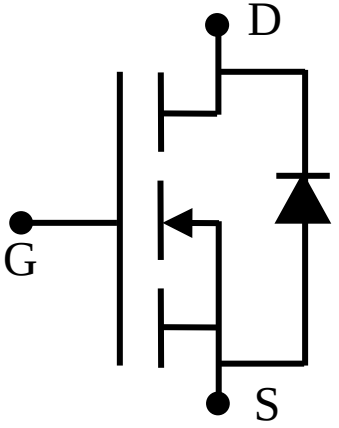
MOSFET de canal p

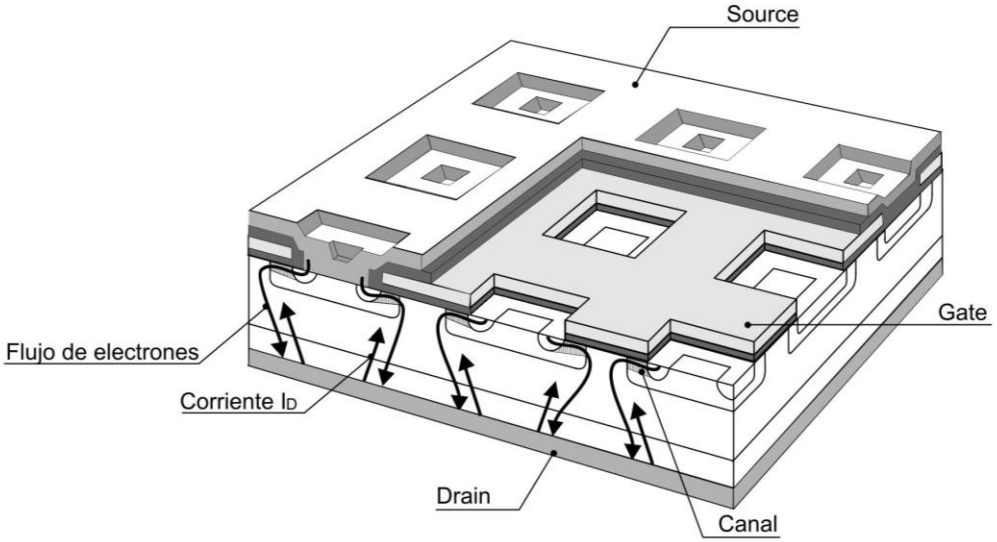
(símbolo)

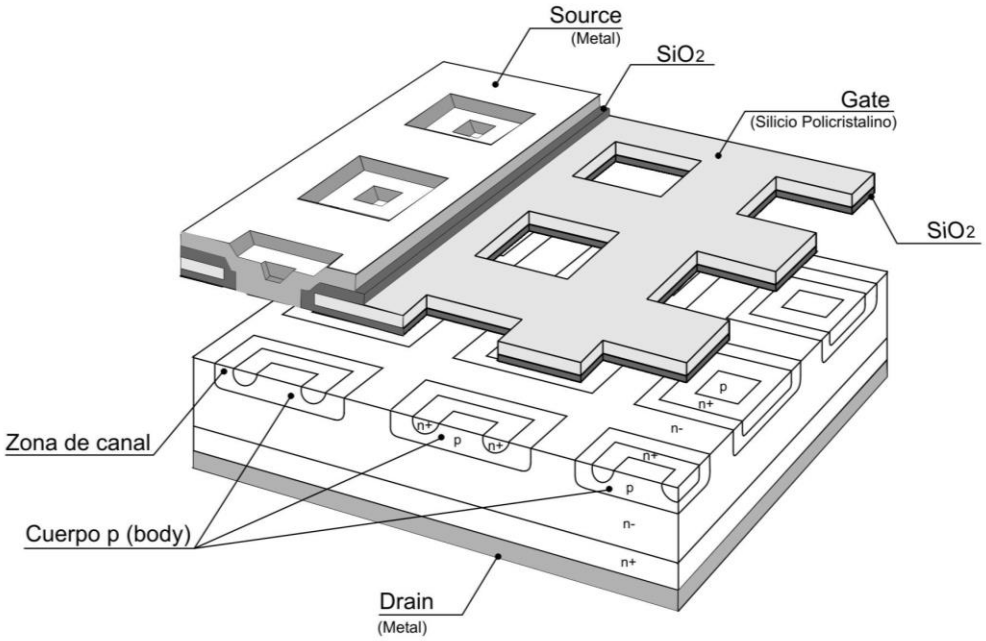


MOSFET de canal n

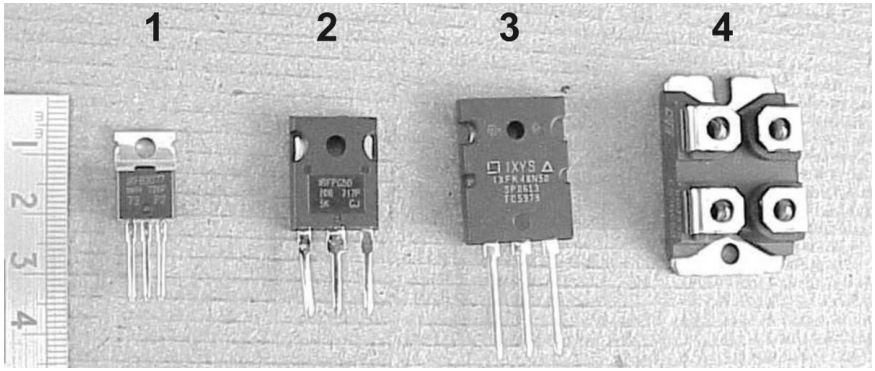
(símbolo)



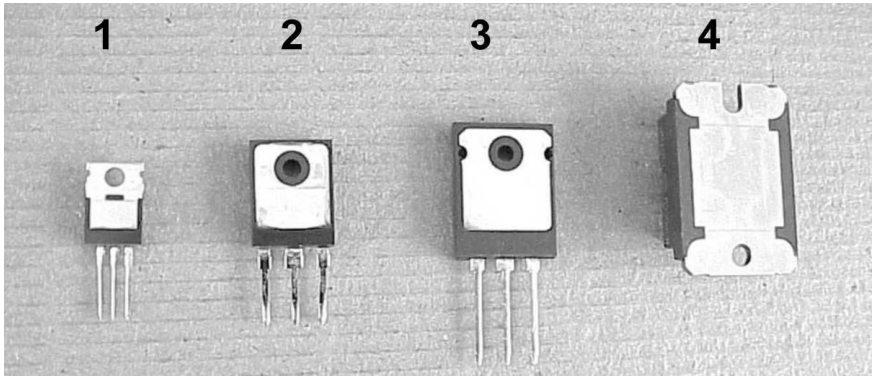

Source
Gate
Flujo de electrones
Corriente I_D
Drain
Canal


Source
(Metal)
SiO_2
Gate
(Silicio Policristalino)
SiO_2
Zona de canal
Cuerpo p (body)
Drain
(Metal)
p
n+
n-
n+
p
n-
n+
n+
p
n+

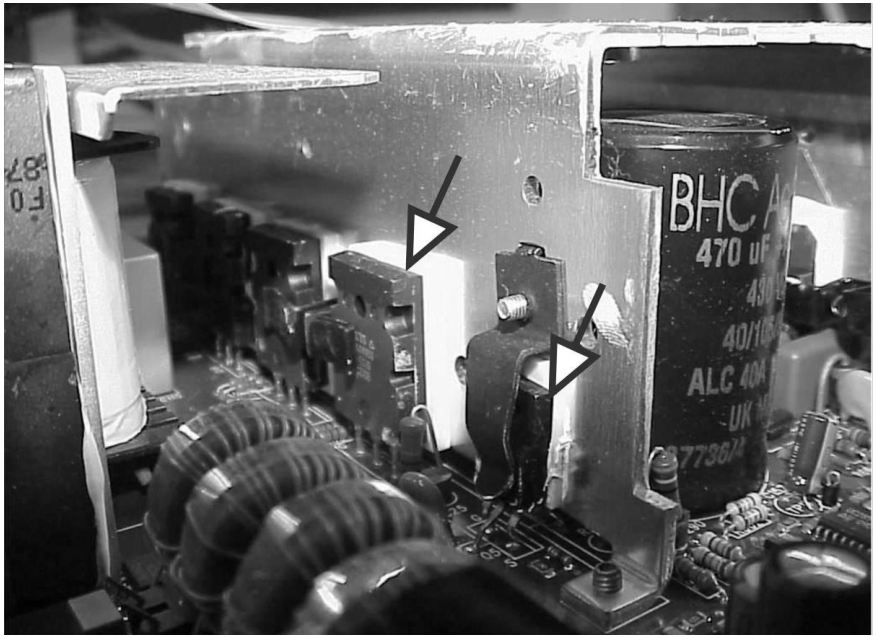
a)



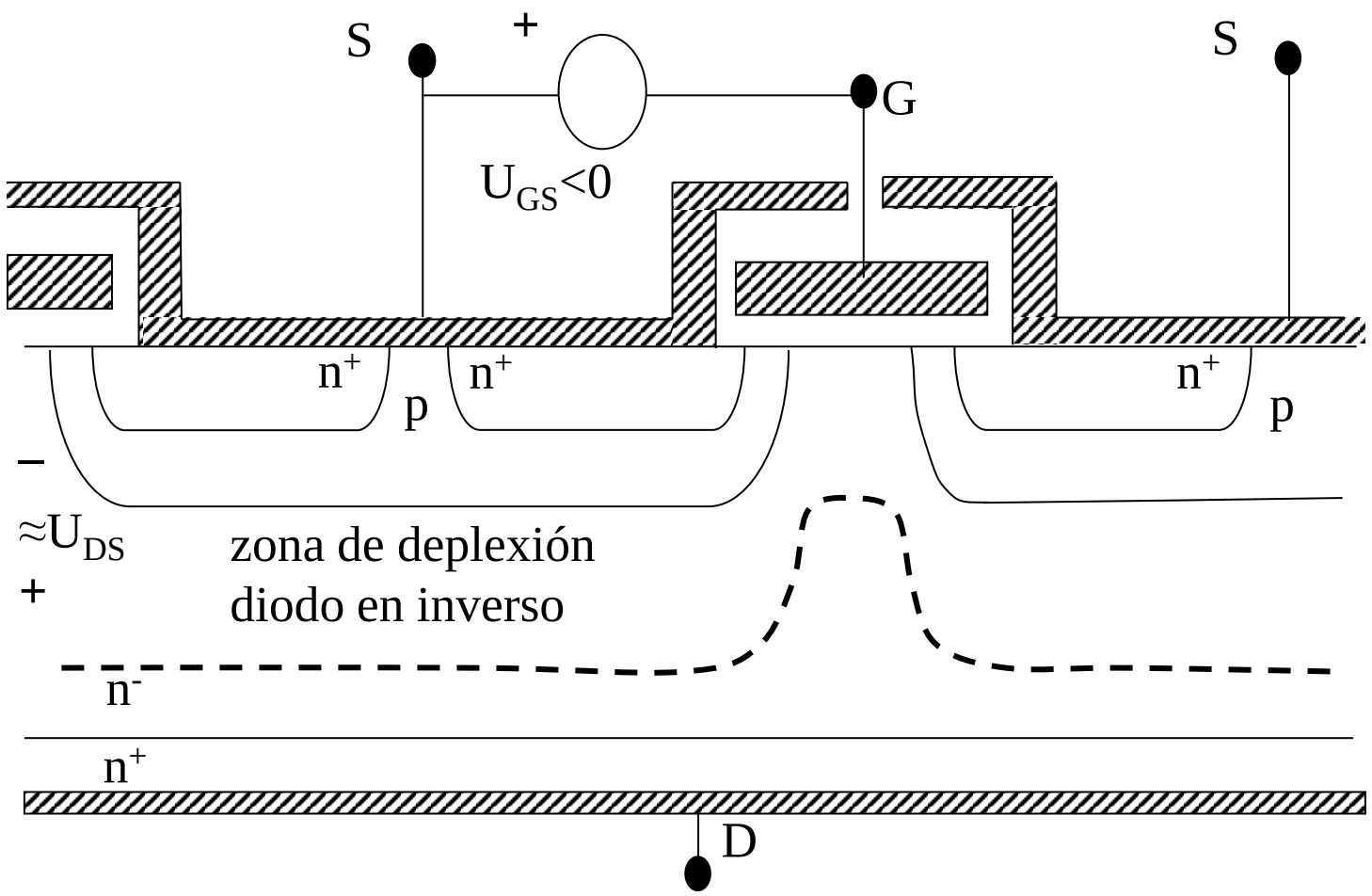
b)



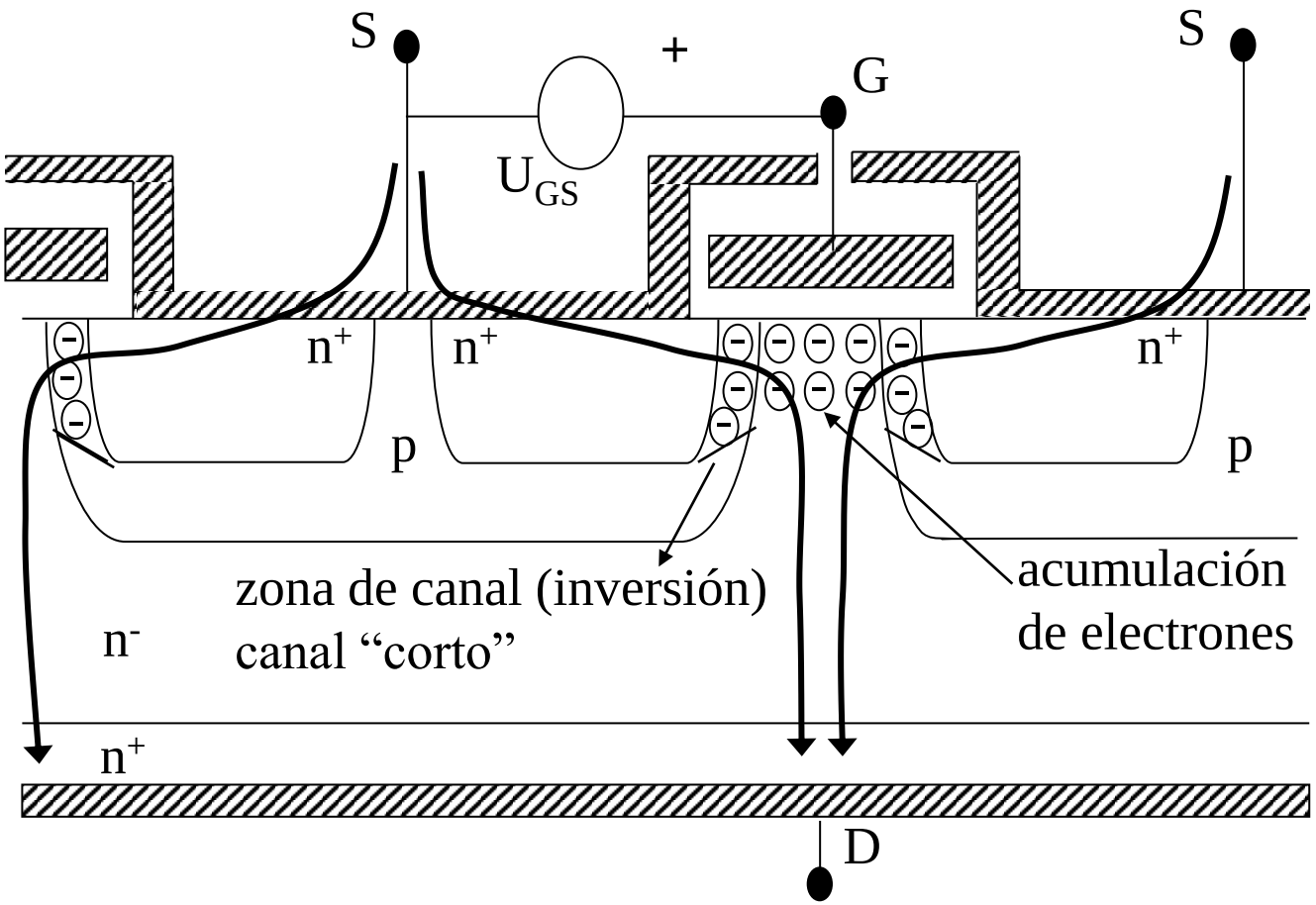
c)



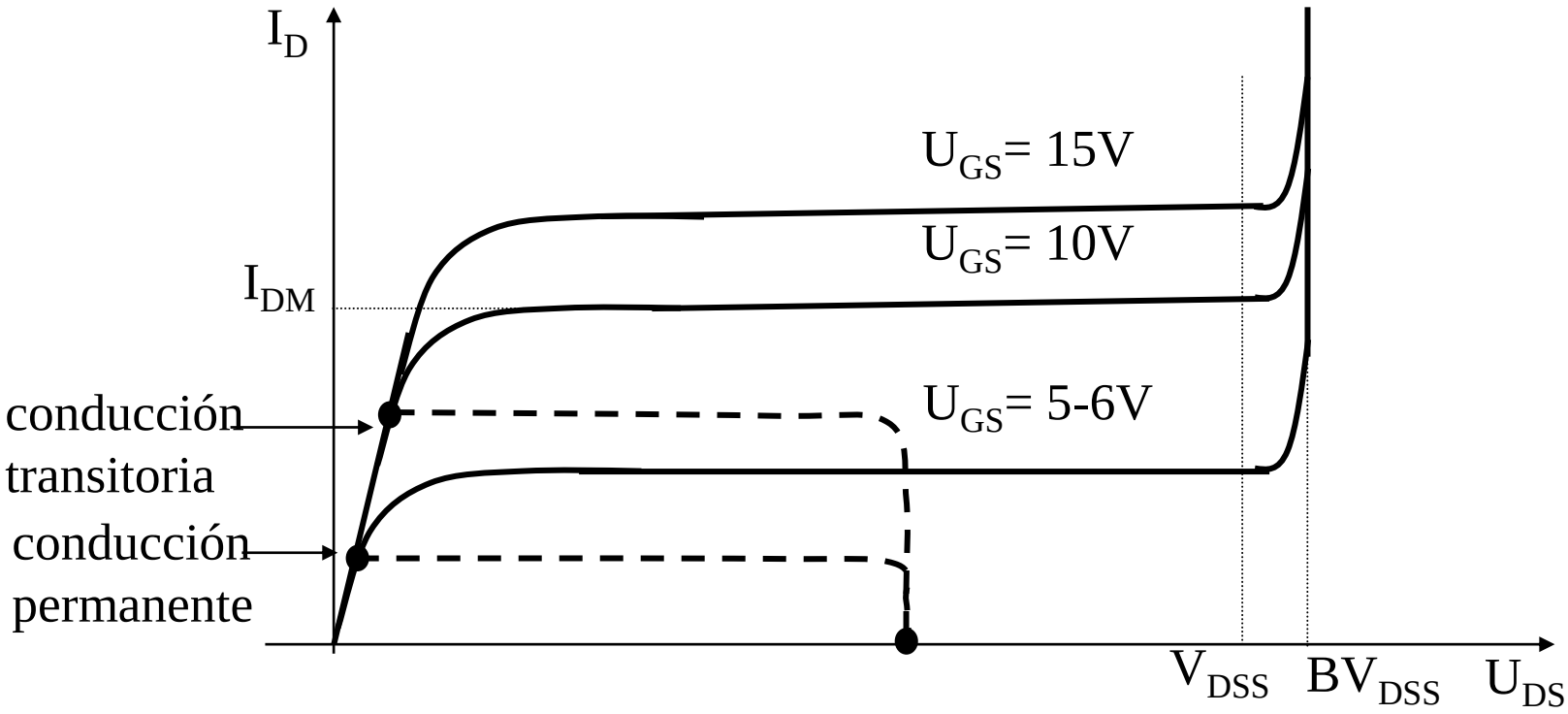
Bloqueo

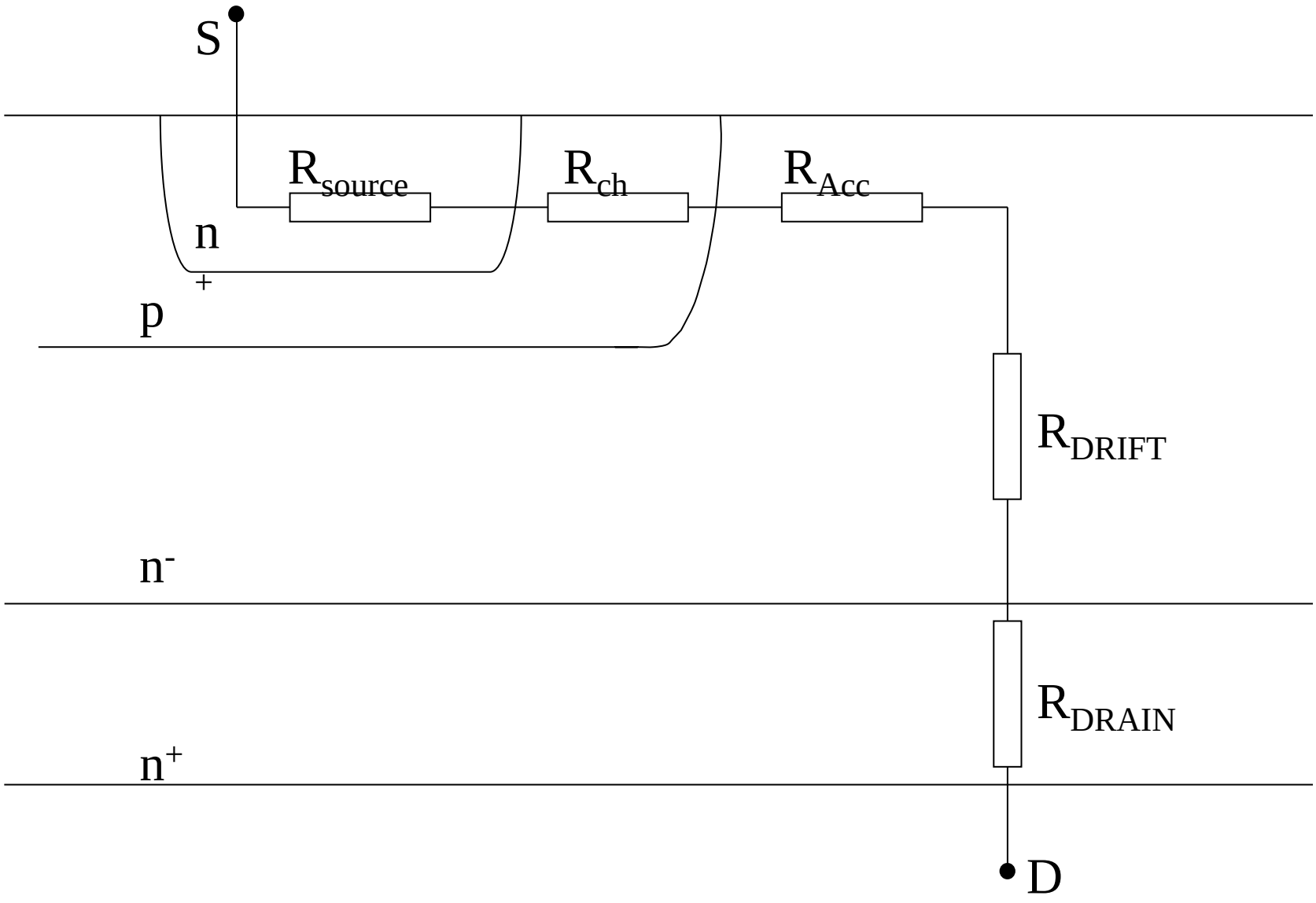

S
+
S
G
U_{GS}<0
n^+
p
n^+
n^+
p
–
$\approx U_{DS}$
+
zona de deplexión
diodo en inverso
n^-
n^+
D

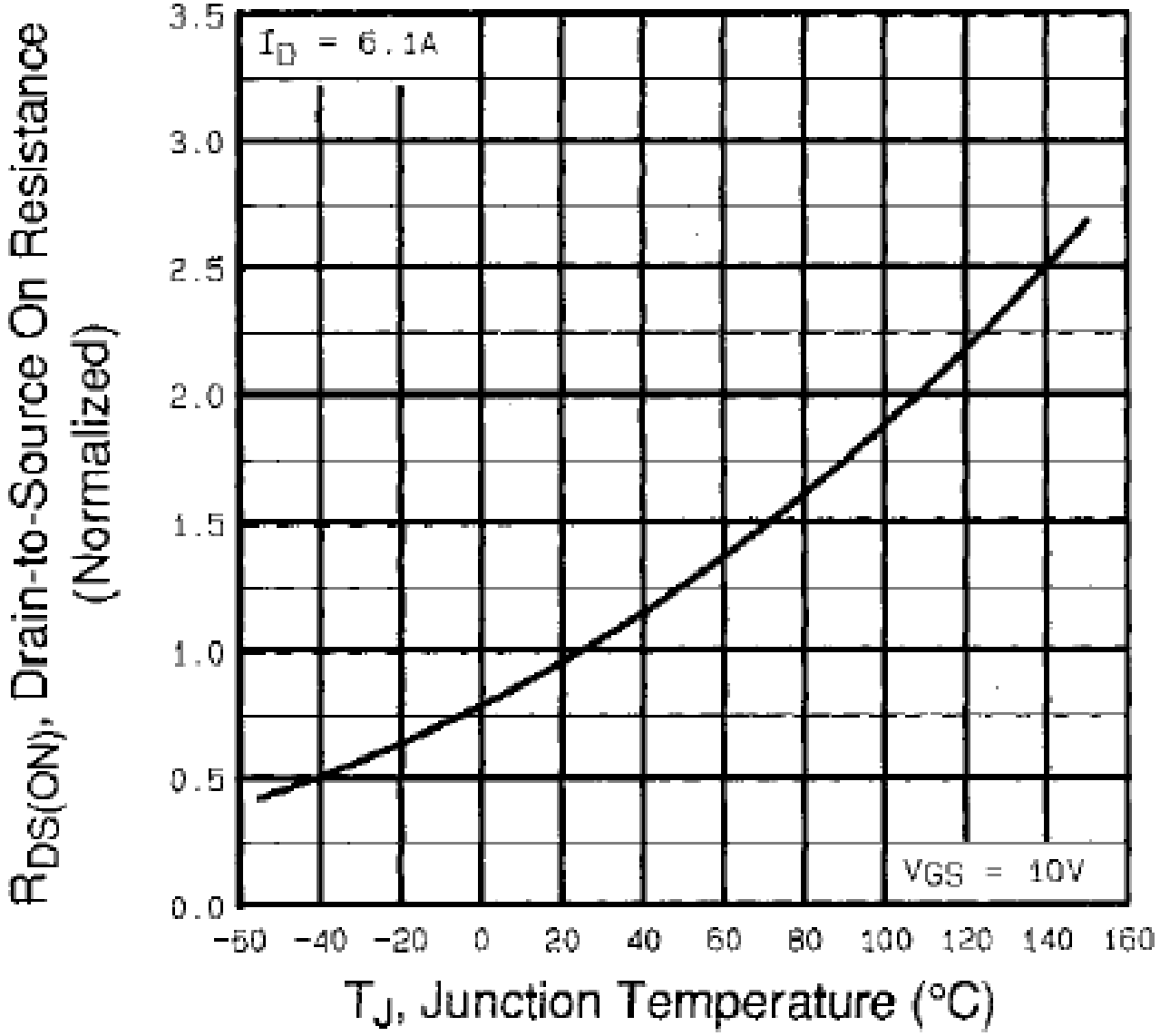
Conducción


S
+
G
S
U_{GS}
n^+
n^+
n^+
p
p
zona de canal (inversión)
canal “corto”
acumulación
de electrones
n^-
n^+
D

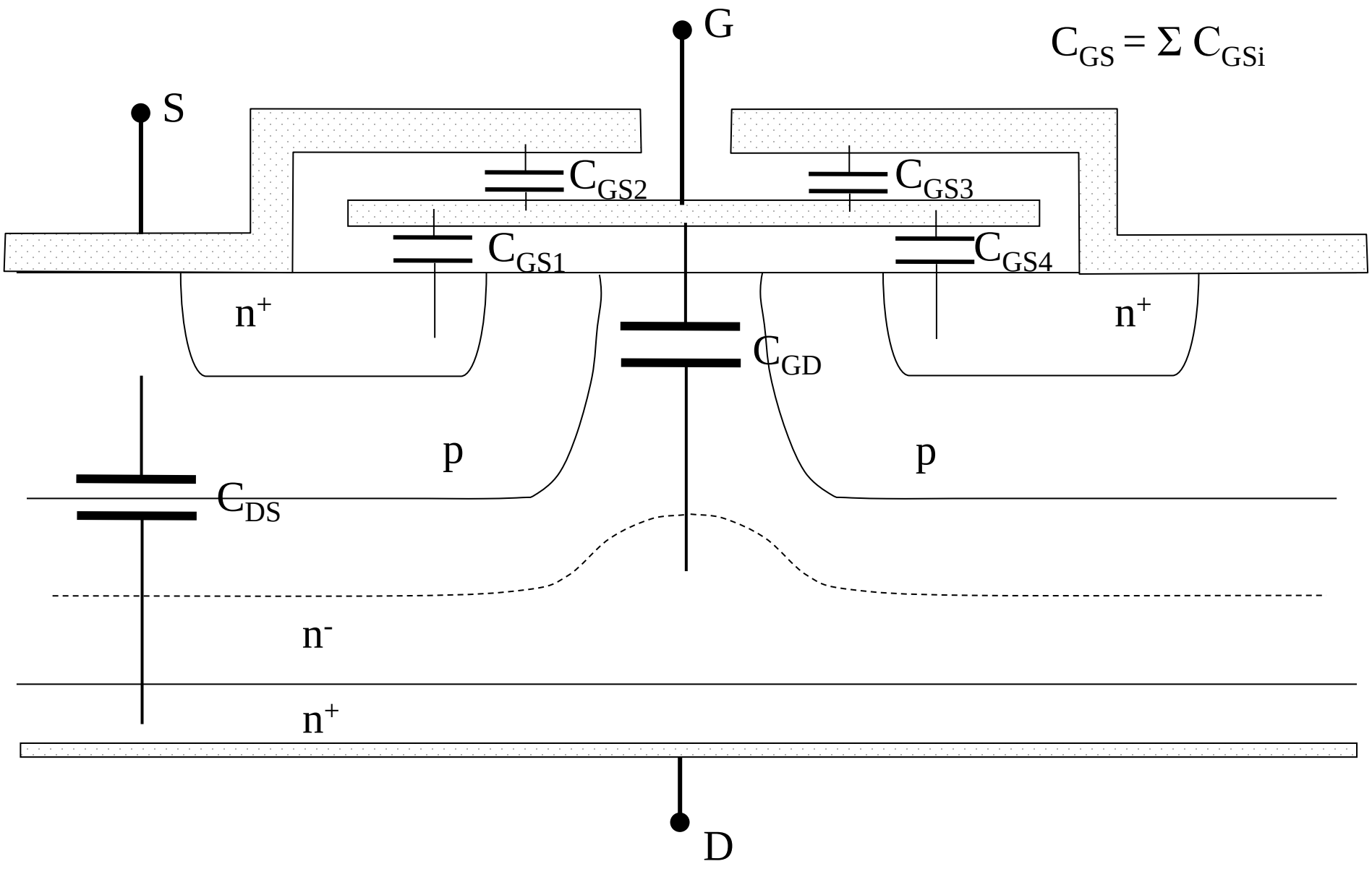
Puntos correspondientes en la curva característica

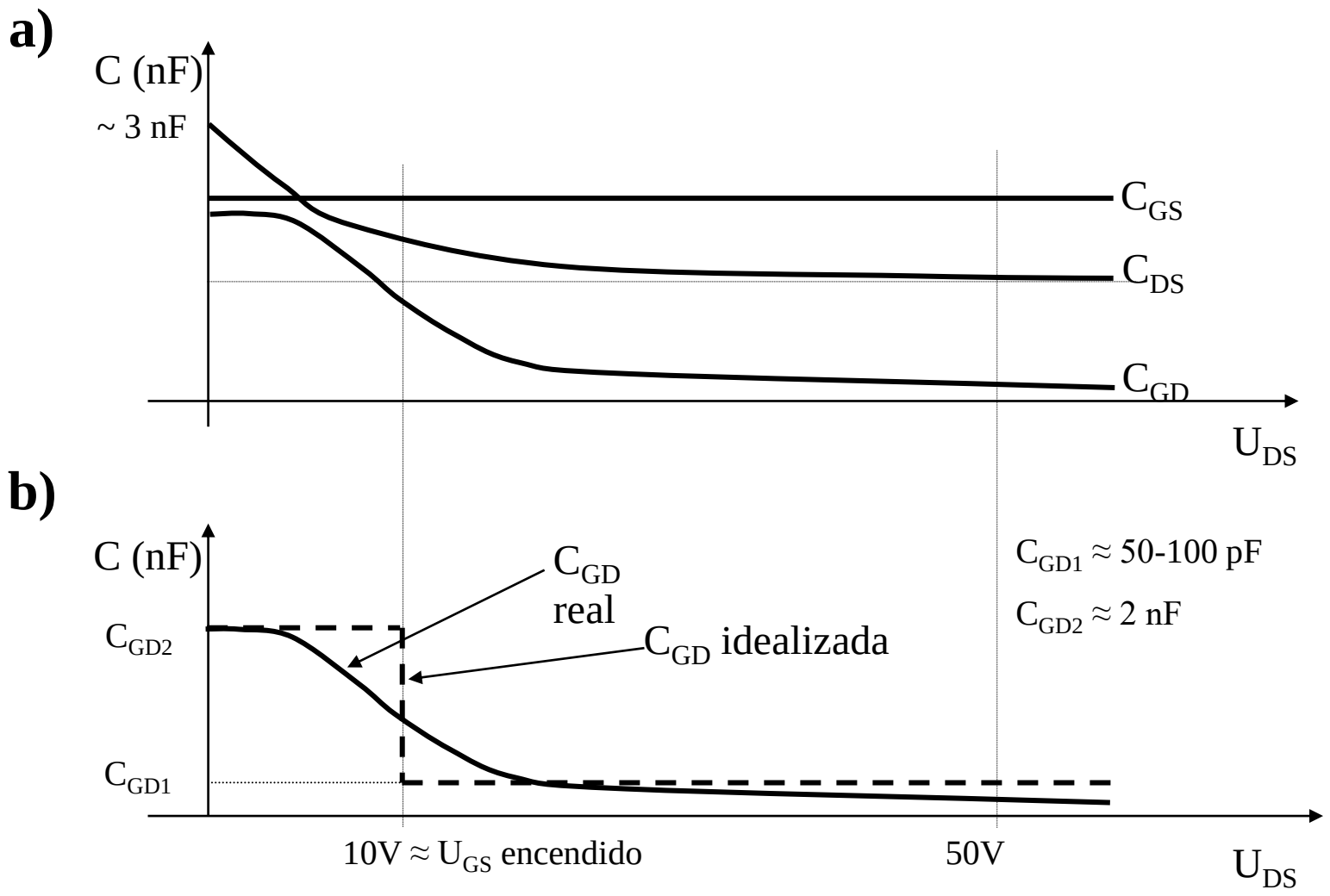



S
R_{source}
R_{ch}
R_{Acc}
n^+
p
R_{DRIFT}
n^-
R_{DRAIN}
n^+
D

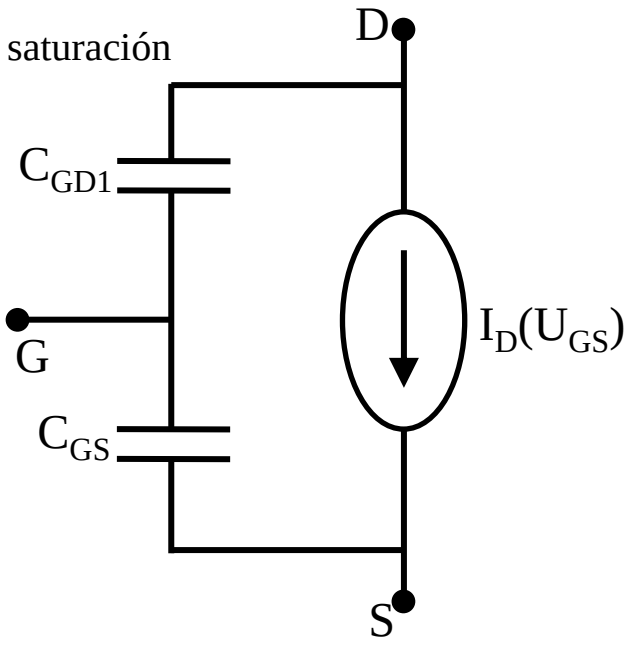

I_D = 6.1A
VGS = 10V
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-60 -40 -20 0 20 40 60 80 100 120 140 160
$R_{DS(ON)}$, Drain-to-Source On Resistance
(Normalized)
T_J, Junction Temperature (°C)

Conmutación

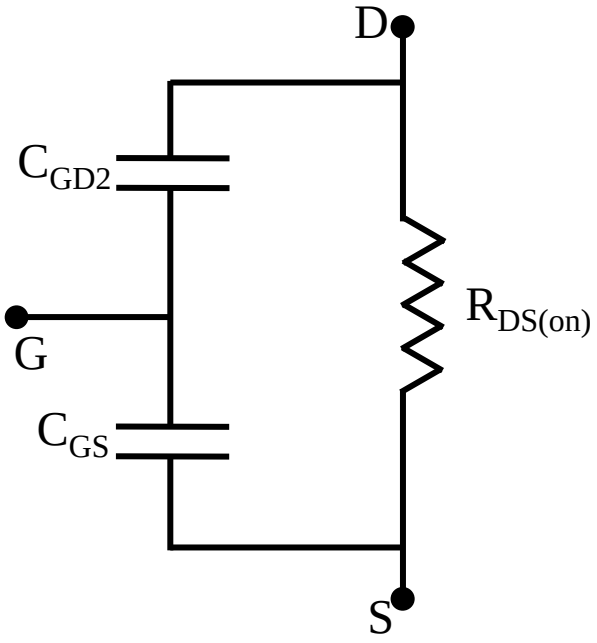

G
$C_{GS} = \Sigma C_{GSi}$
S
C_{GS2}
C_{GS3}
C_{GS1}
C_{GS4}
n^+
n^+
C_{GD}
p
p
C_{DS}
n^-
n^+
D

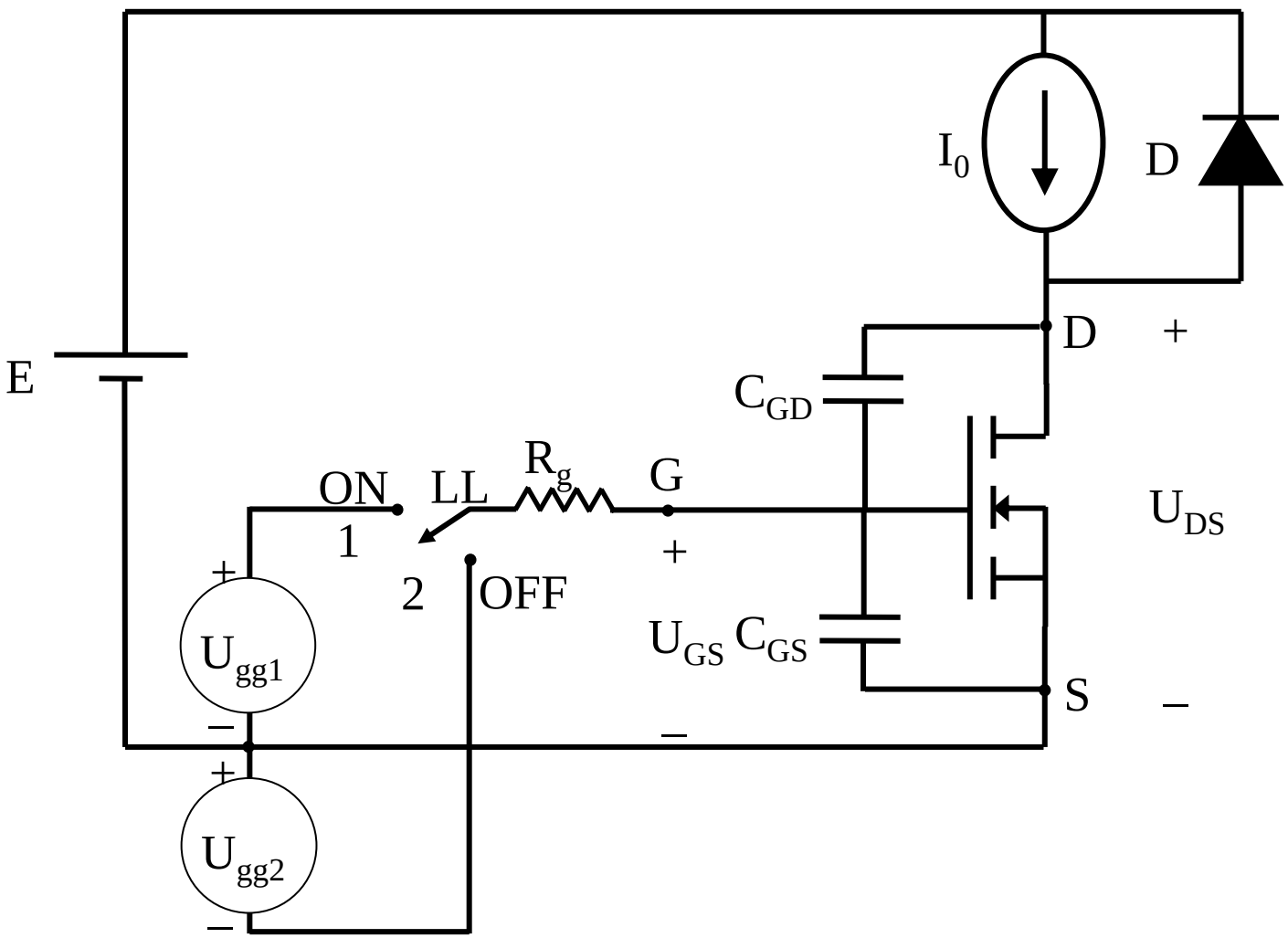

a)
C (nF)
~ 3 nF
C_{GS}
C_{DS}
C_{GD}
U_{DS}
b)
C (nF)
C_{GD} real
C_{GD} idealizada
$C_{GD1} \approx$ 50-100 pF
$C_{GD2} \approx$ 2 nF
C_{GD2}
C_{GD1}
10V ≈ U_{GS} encendido
50V
U_{DS}

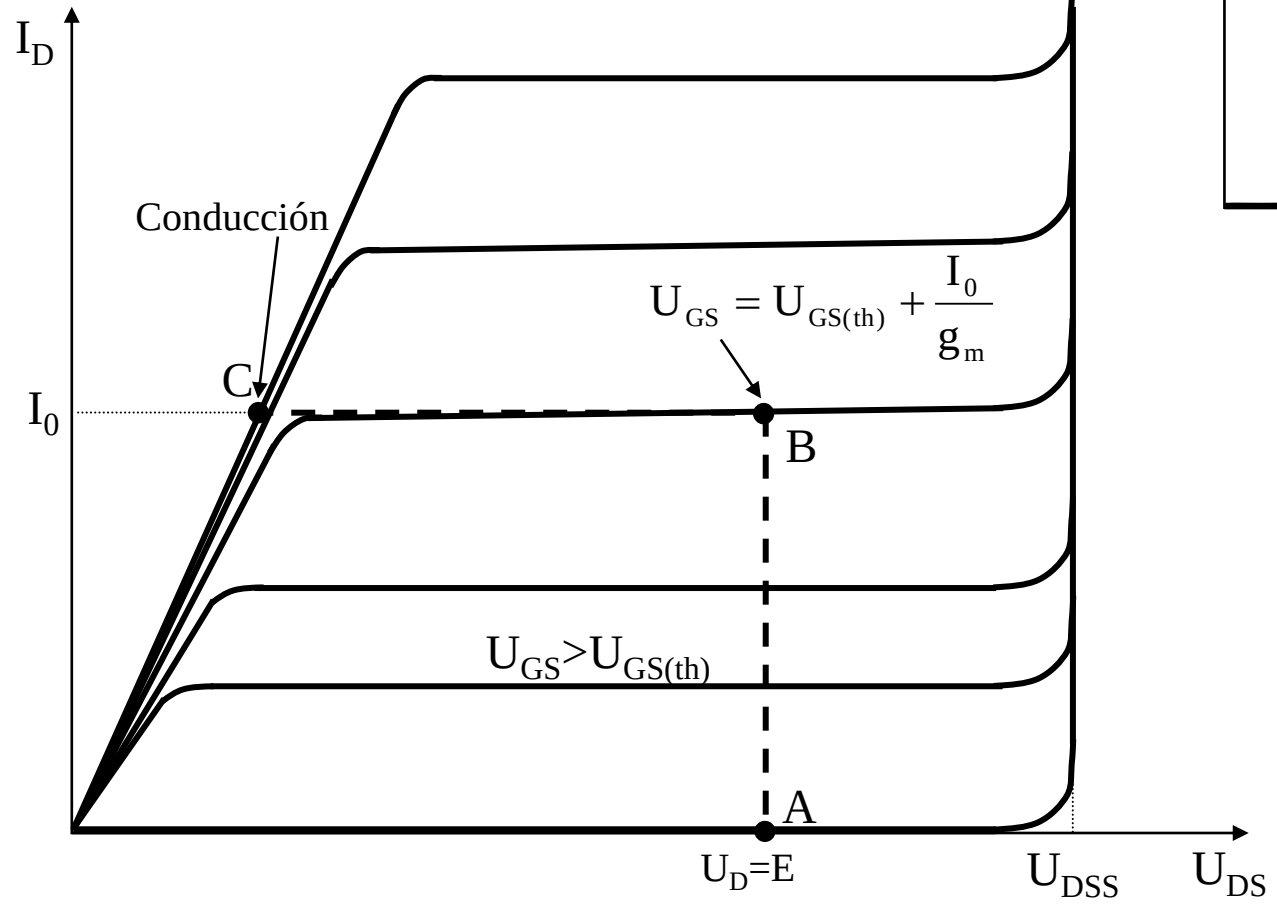
a) En la zona activa o de saturación

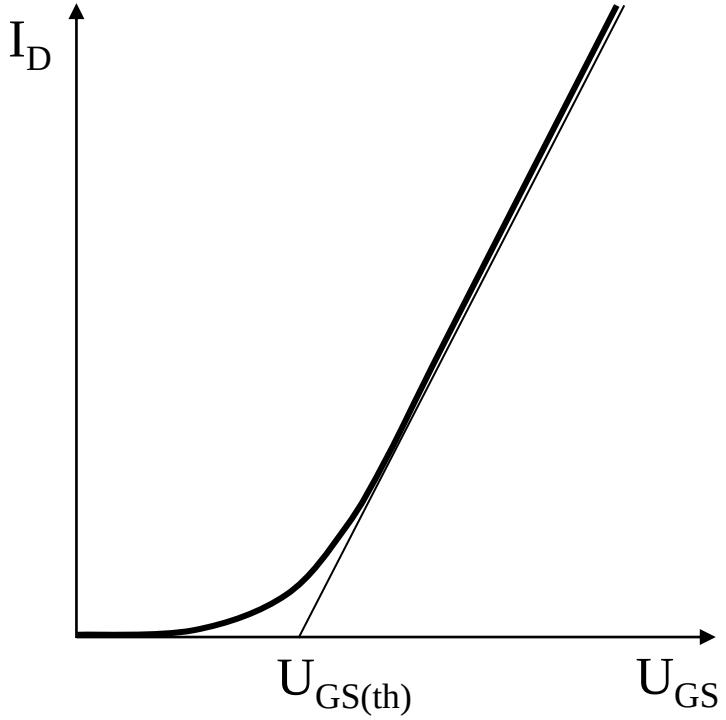


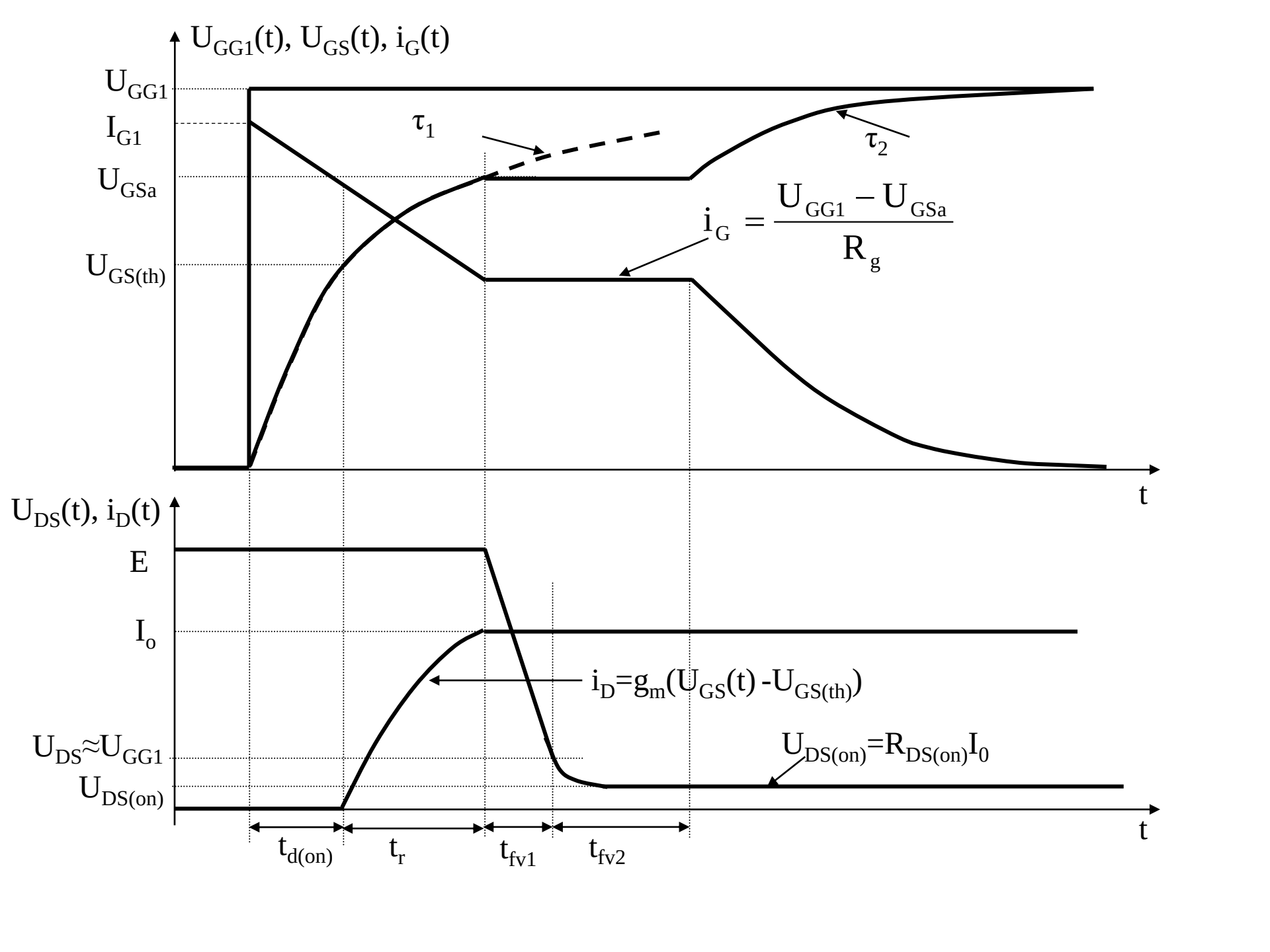
a) En la zona resistiva

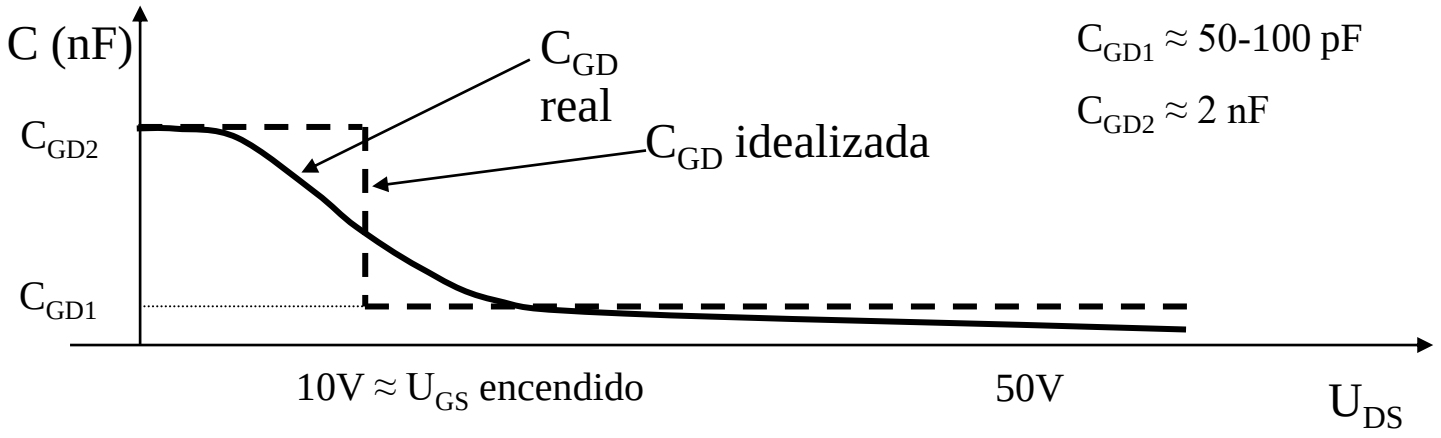


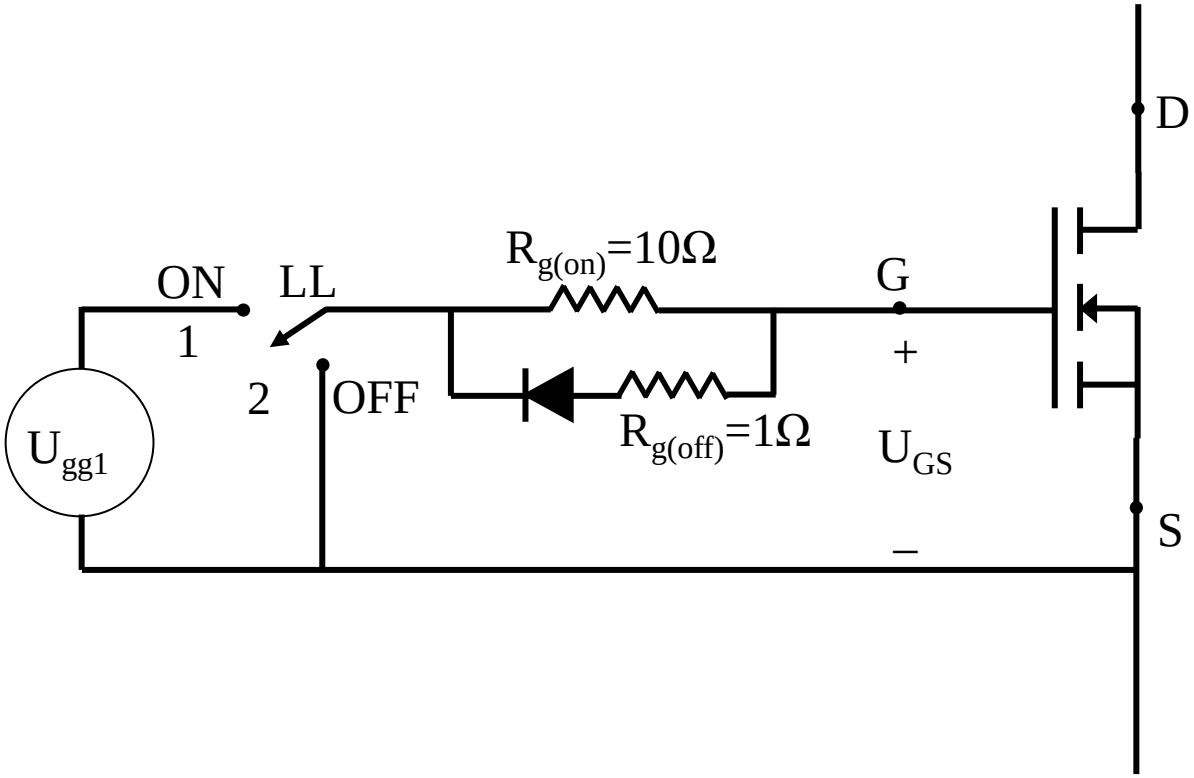

I0
D
D
+
E
CGD
Rg
ON
LL
G
UDS
1
+
+
2
OFF
Ugg1
UGS
CGS
S
–
–
+
Ugg2
–

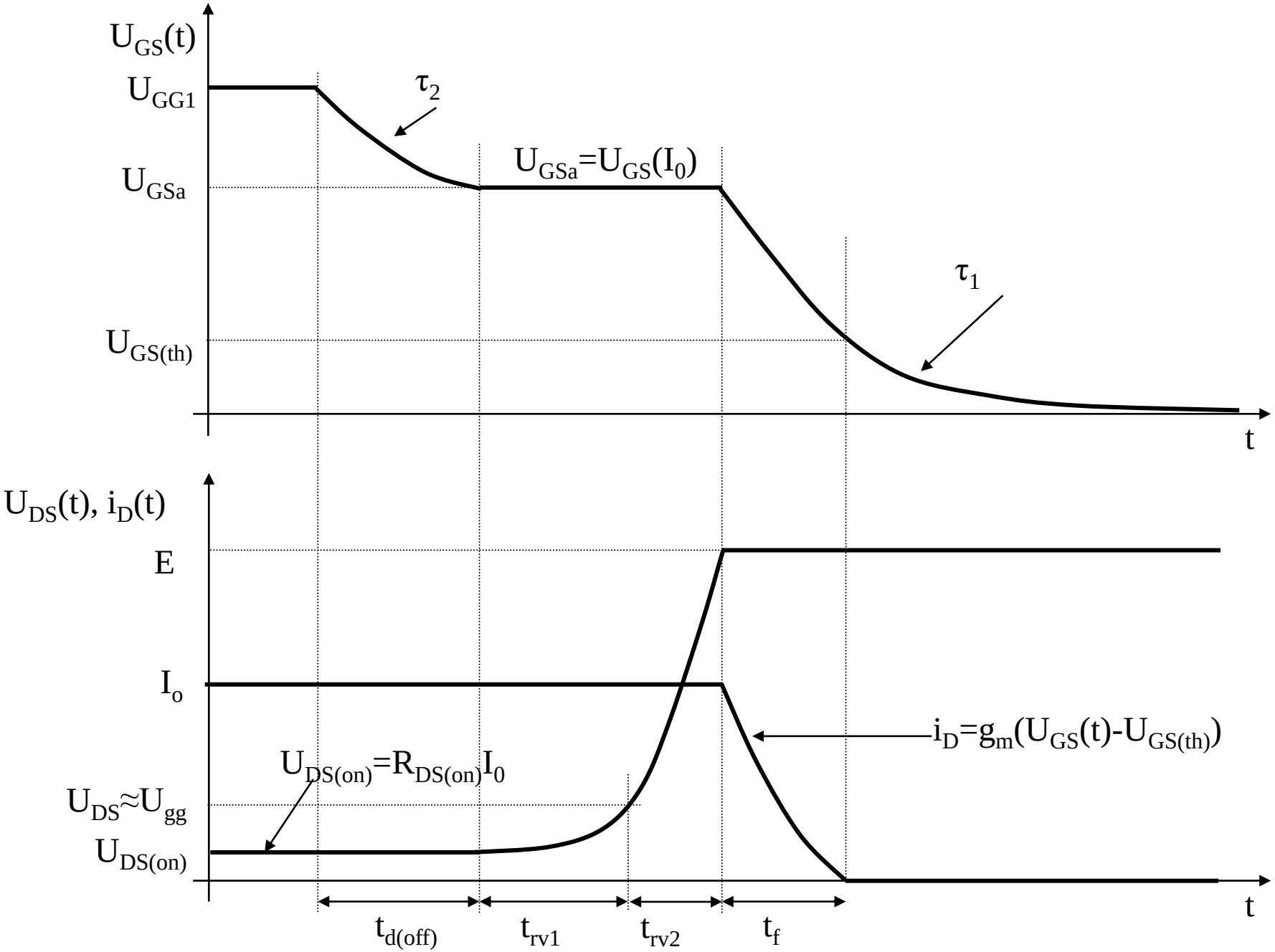

I_D
Conducción
$U_{GS} = U_{GS(th)} + \frac{I_0}{g_m}$
C
I_0
B
$U_{GS}>U_{GS(th)}$
A
U_D=E
U_{DSS}
U_{DS}
Bloqueo


I_D
$U_{GS(th)}$
U_{GS}

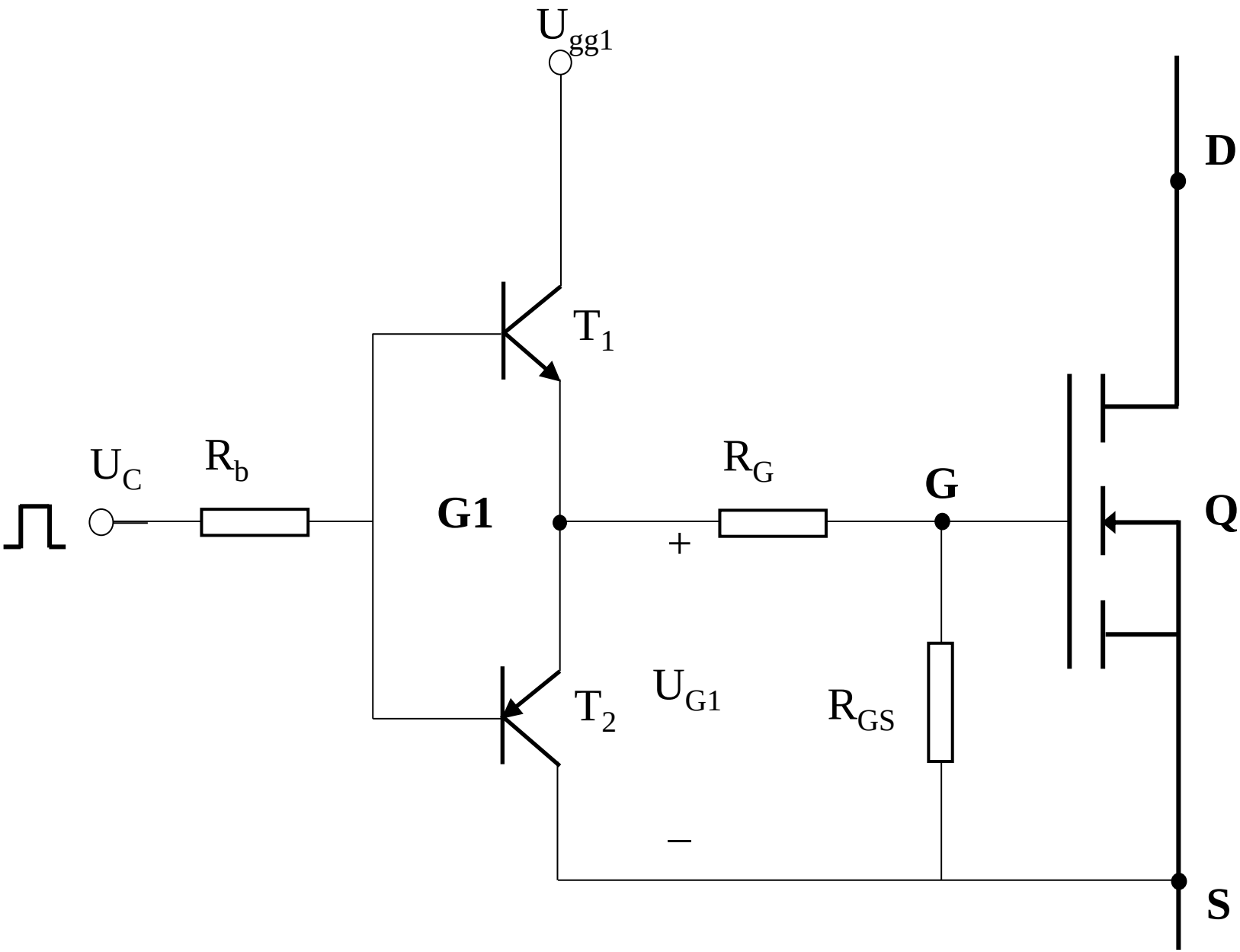

$U_{GG1}(t)$, $U_{GS}(t)$, $i_G(t)$
U_{GG1}
I_{G1}
U_{GSa}
$U_{GS(th)}$
τ_1
τ_2
$i_G = \frac{U_{GG1} - U_{GSa}}{R_g}$
t
$U_{DS}(t)$, $i_D(t)$
E
I_o
$i_D = g_m(U_{GS}(t) - U_{GS(th)})$
$U_{DS} \approx U_{GG1}$
$U_{DS(on)}$
$U_{DS(on)} = R_{DS(on)} I_0$
t
$t_{d(on)}$
t_r
t_{fv1}
t_{fv2}

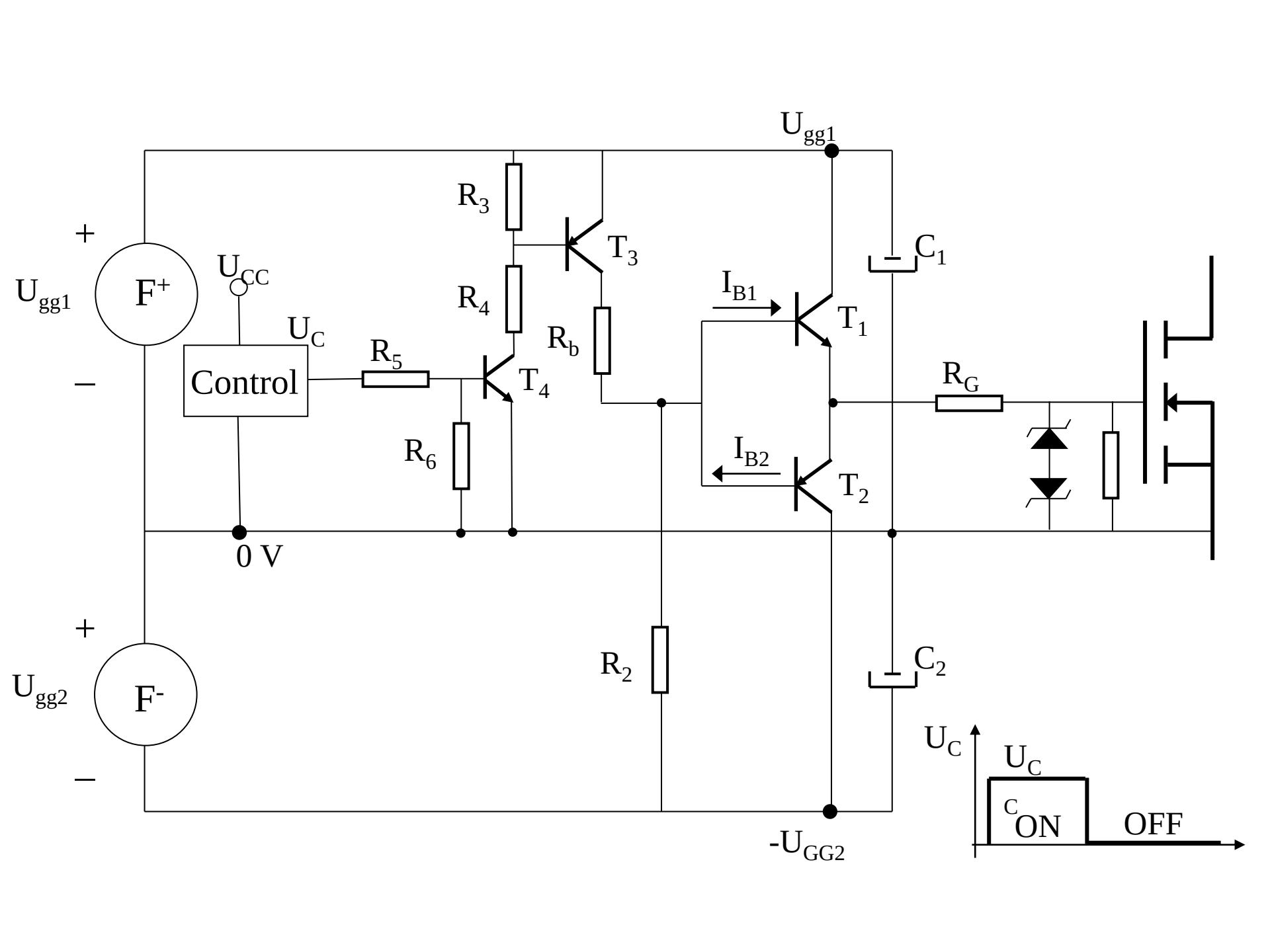

C (nF)
C_{GD2}
C_{GD1}
C_{GD} real
C_{GD} idealizada
$C_{GD1} \approx$ 50-100 pF
$C_{GD2} \approx$ 2 nF
10V ≈ U_{GS} encendido
50V
U_{DS}


D
$R_{g(on)}$=10Ω
ON
LL
G
1
+
2
OFF
U_{gg1}
$R_{g(off)}$=1Ω
U_{GS}
S
–

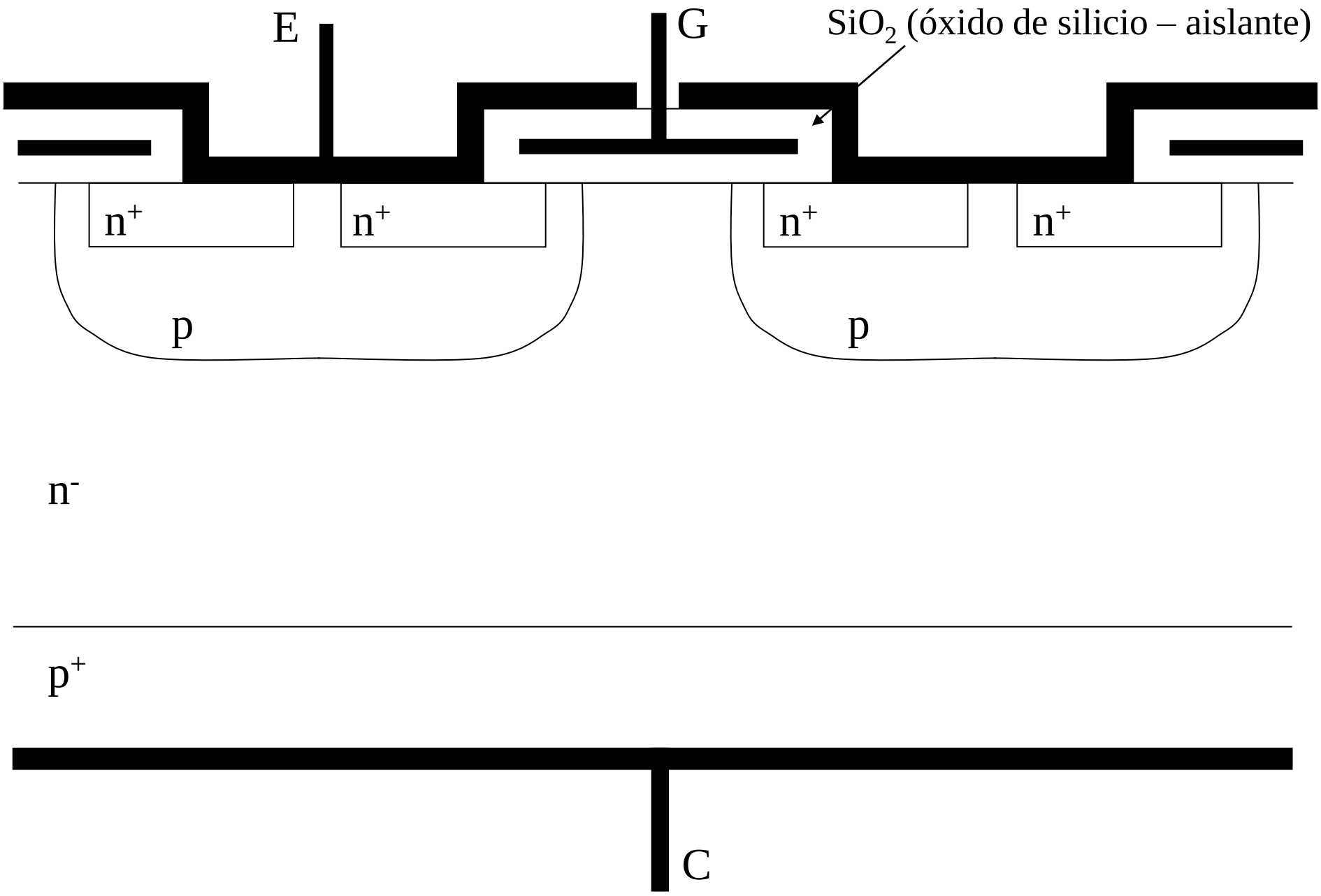

$U_{GS}(t)$
U_{GG1}
τ_2
$U_{GSa}=U_{GS}(I_0)$
U_{GSa}
τ_1
$U_{GS(th)}$
t
$U_{DS}(t)$, $i_D(t)$
E
I_o
$i_D=g_m(U_{GS}(t)-U_{GS(th)})$
$U_{DS(on)}=R_{DS(on)}I_0$
$U_{DS}\approx U_{gg}$
$U_{DS(on)}$
t
$t_{d(off)}$
t_{rv1}
t_{rv2}
t_f

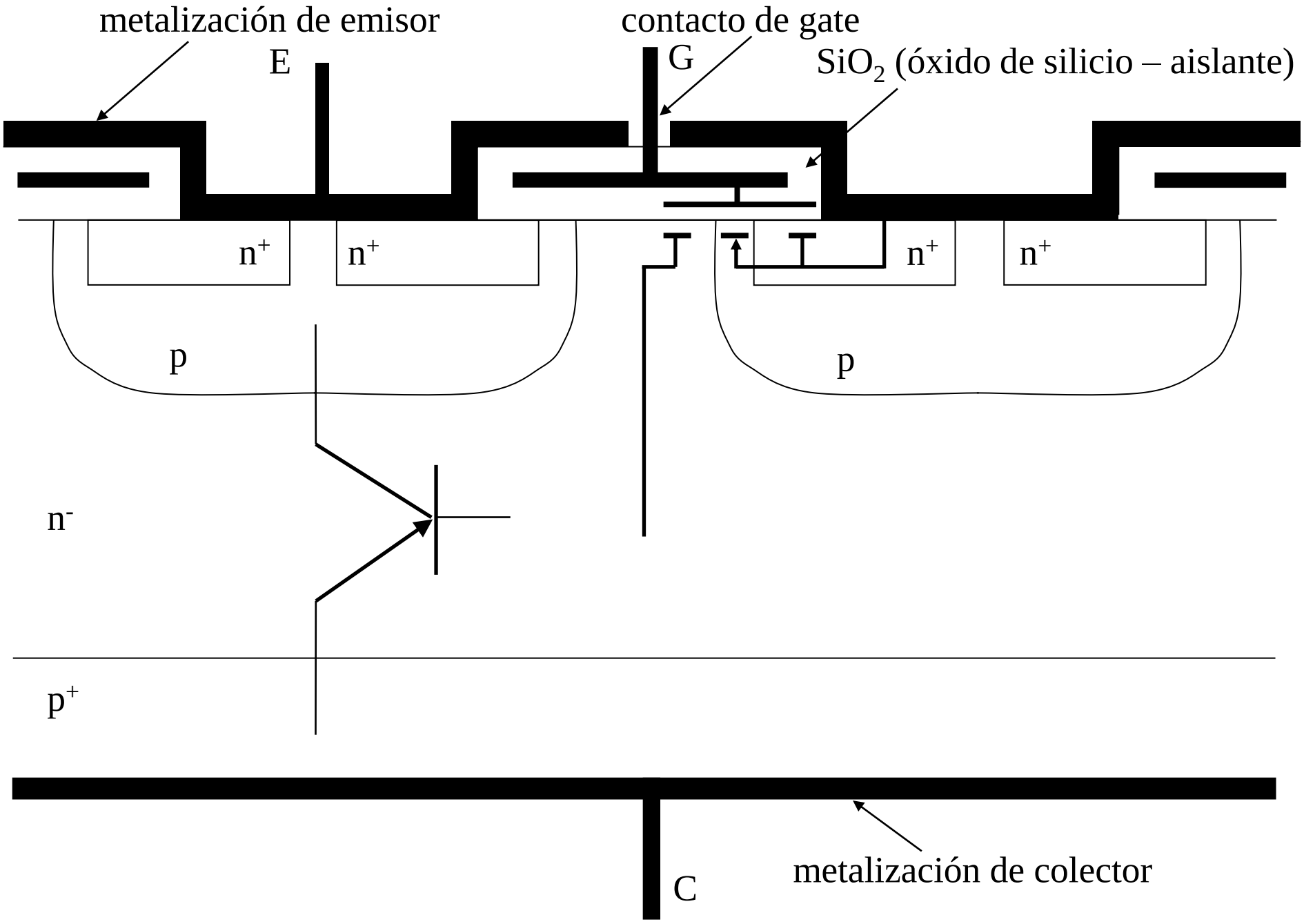
Pérdidas en el MOSFET

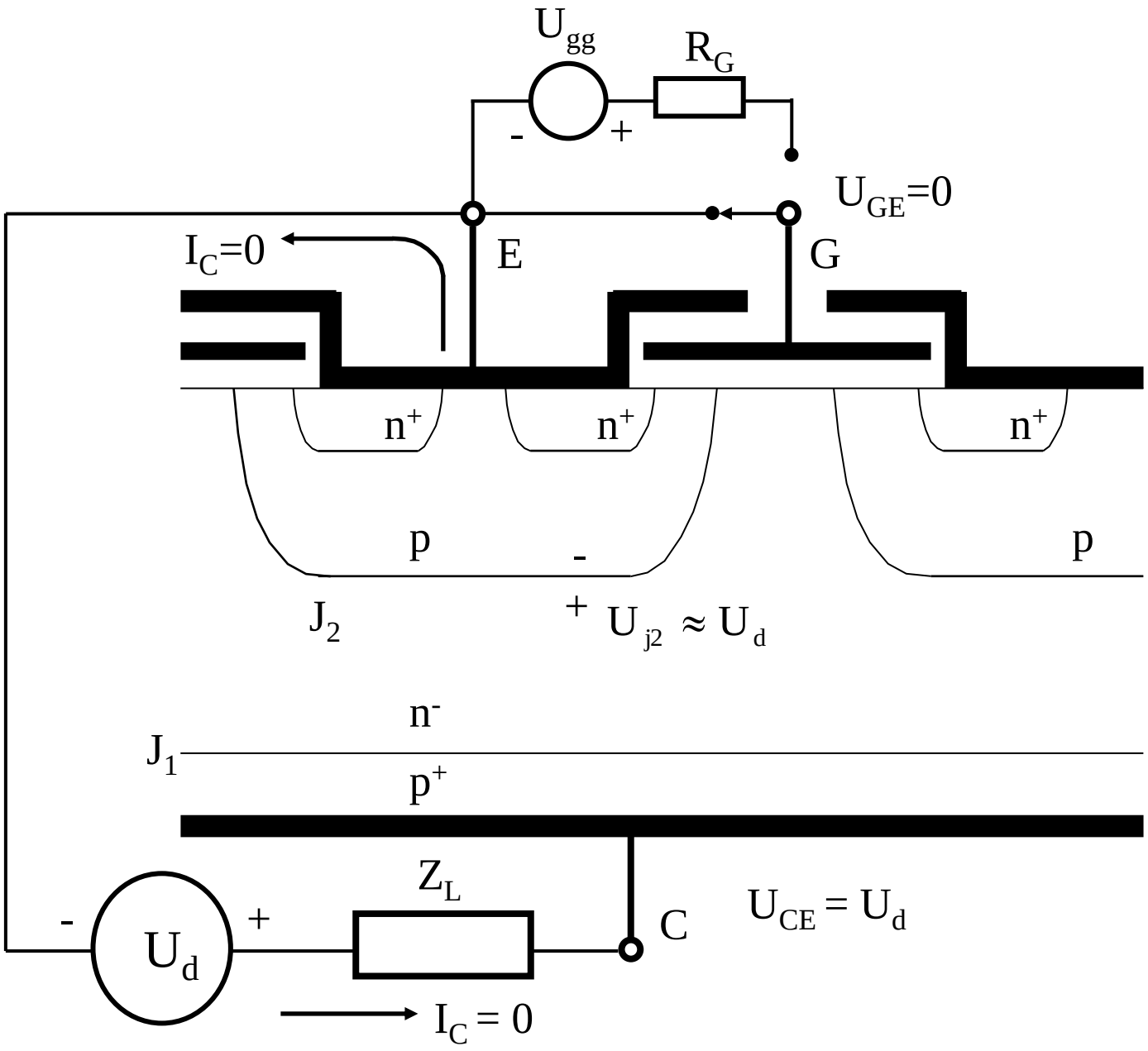

U_{gg1}
D
T_1
U_C
R_b
G1
R_G
G
Q
+
T_2
U_{G1}
R_{GS}
–
S

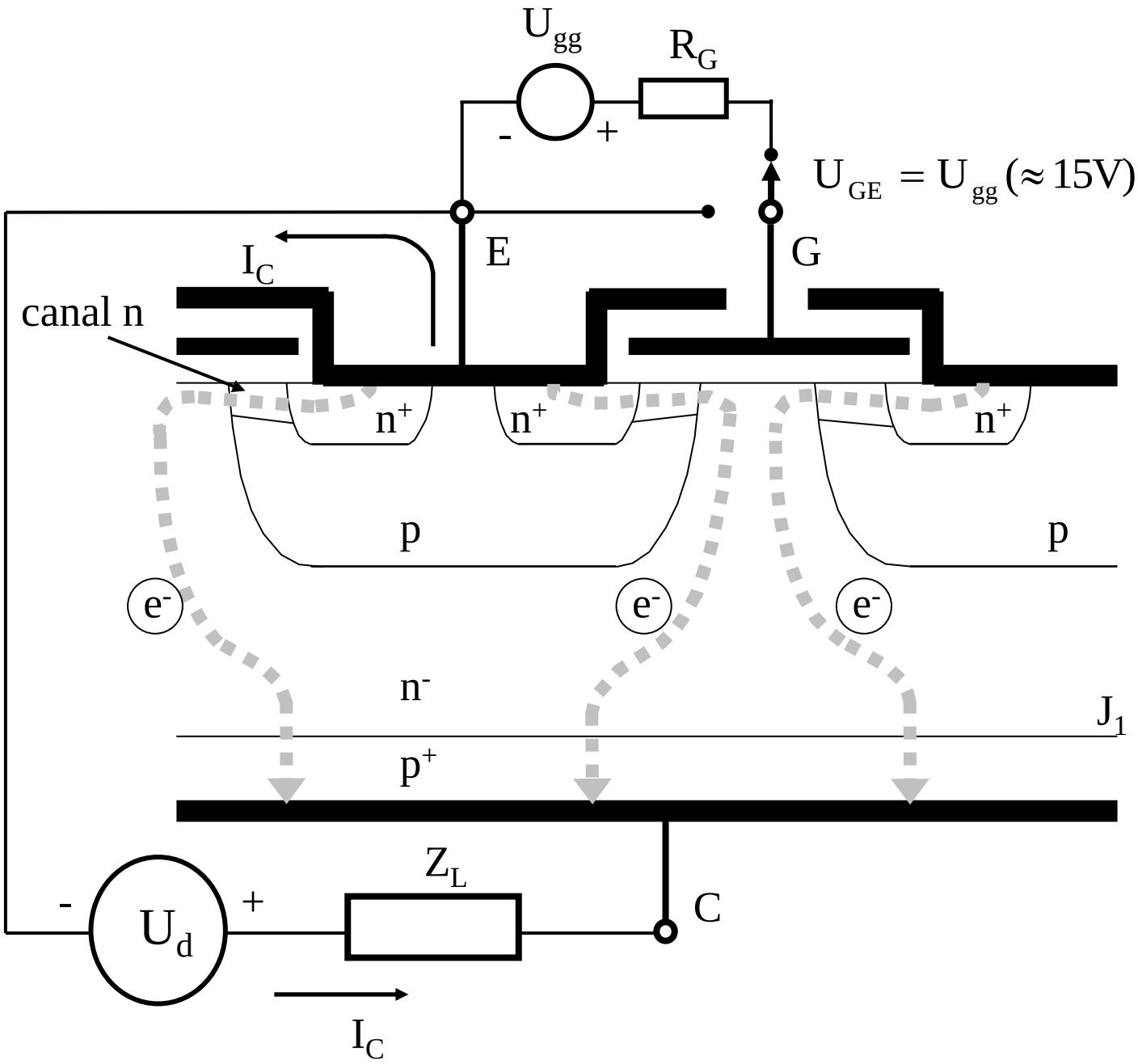

U_gg1
R_3
T_3
C_1
+
U_gg1
F+
U_CC
R_4
I_B1
T_1
U_C
R_b
Control
R_5
T_4
R_G
R_6
I_B2
T_2
0 V
+
U_gg2
F-
R_2
C_2
U_C
U_C
C
ON
OFF
-U_GG2

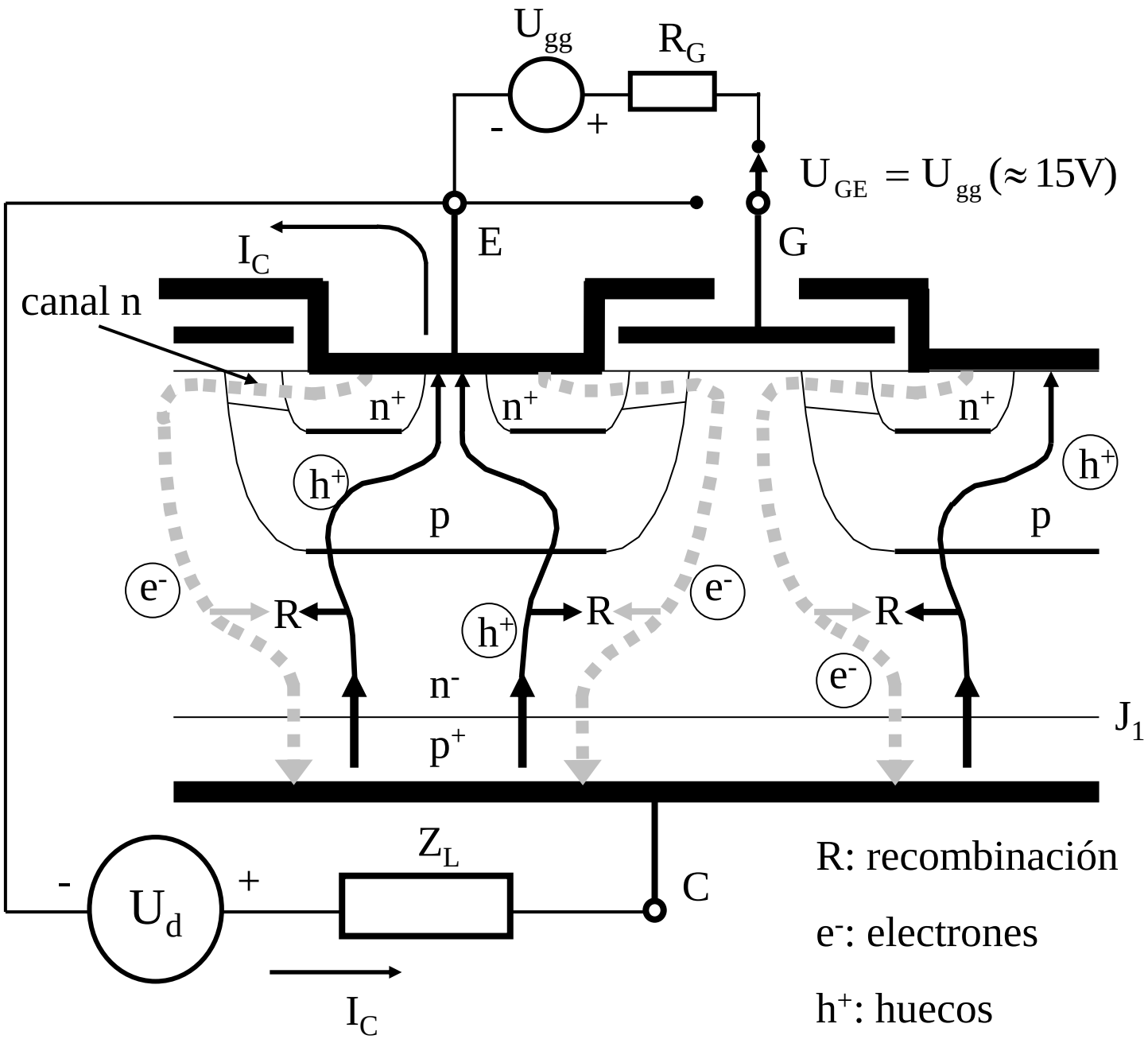
IGBT

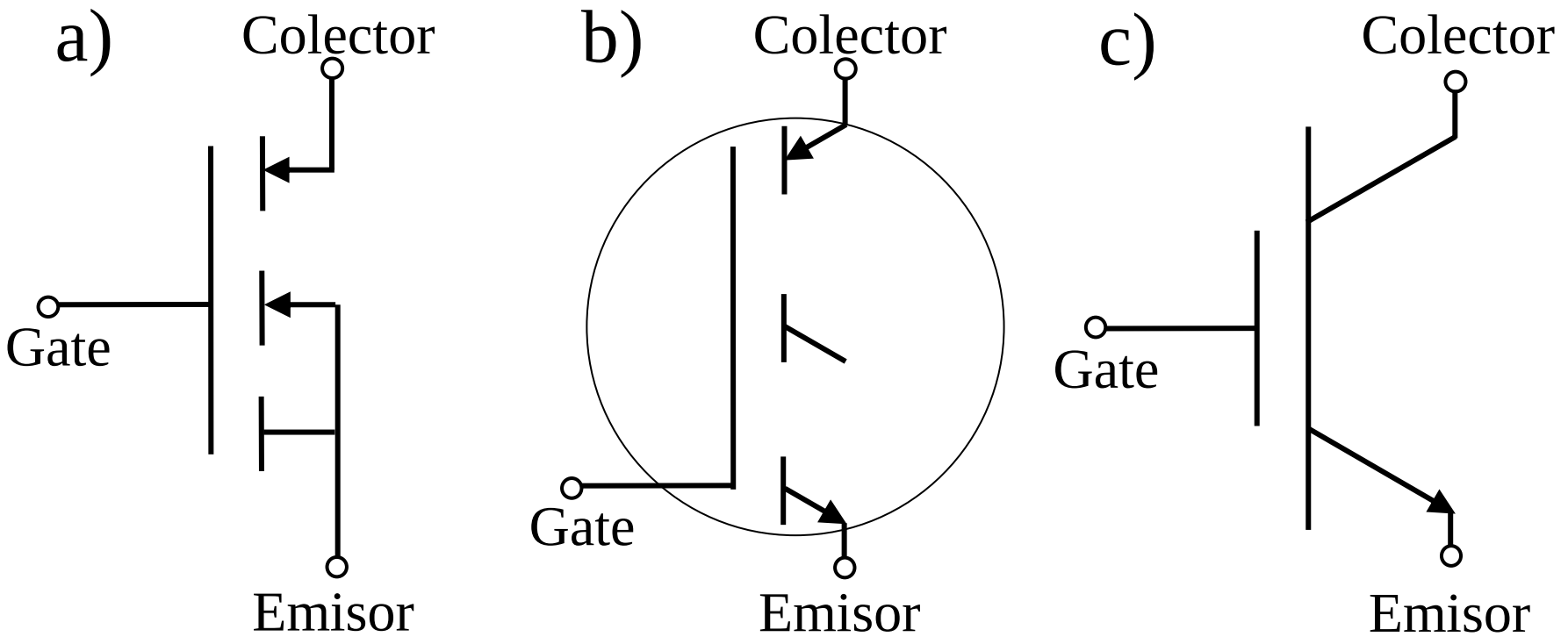

E
G
SiO2 (óxido de silicio – aislante)
n+
n+
n+
n+
p
p
n-
p+
C

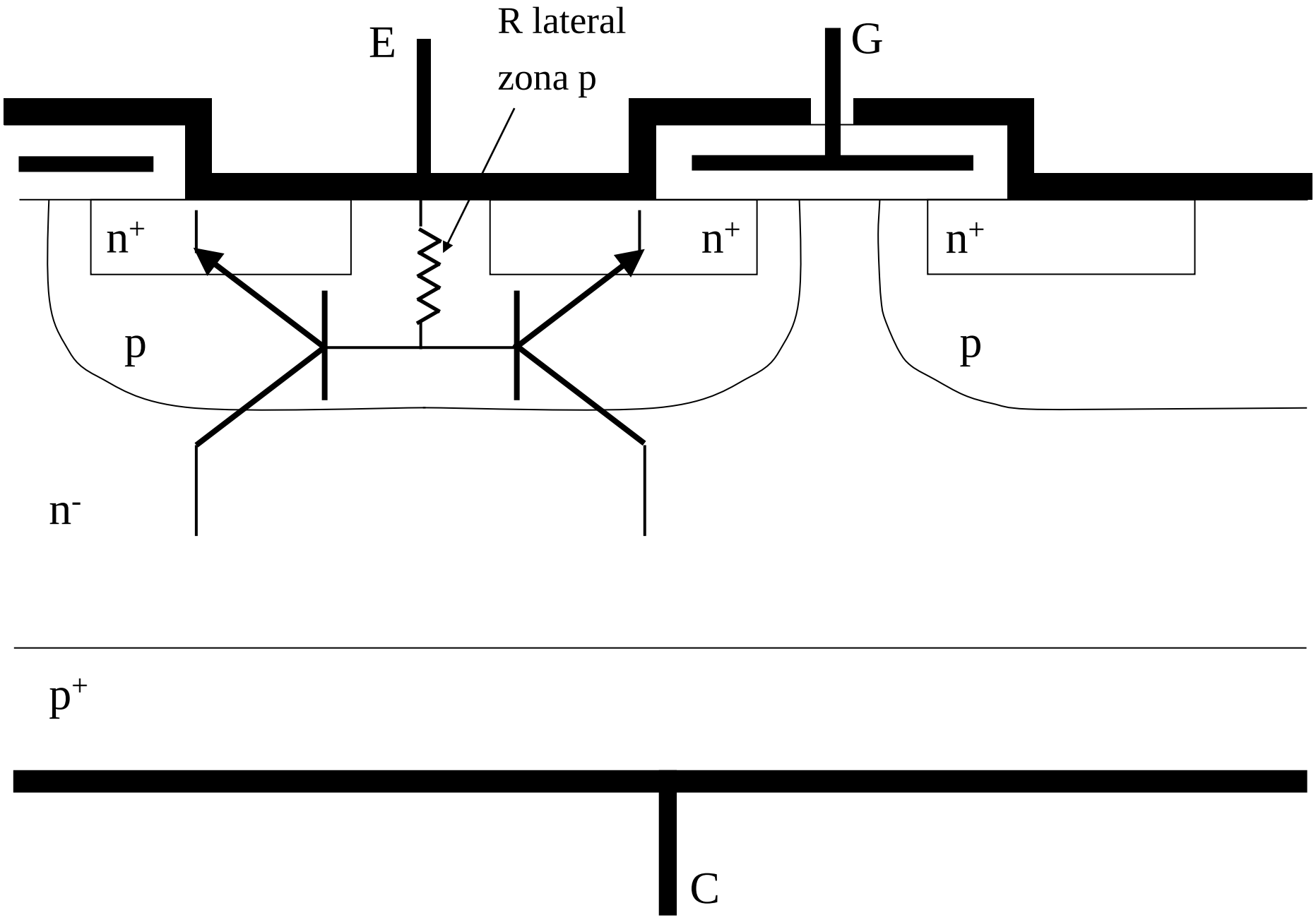

metalización de emisor
E
contacto de gate
G
SiO_2 (óxido de silicio – aislante)
n^+
n^+
n^+
n^+
p
p
n^-
p^+
C
metalización de colector

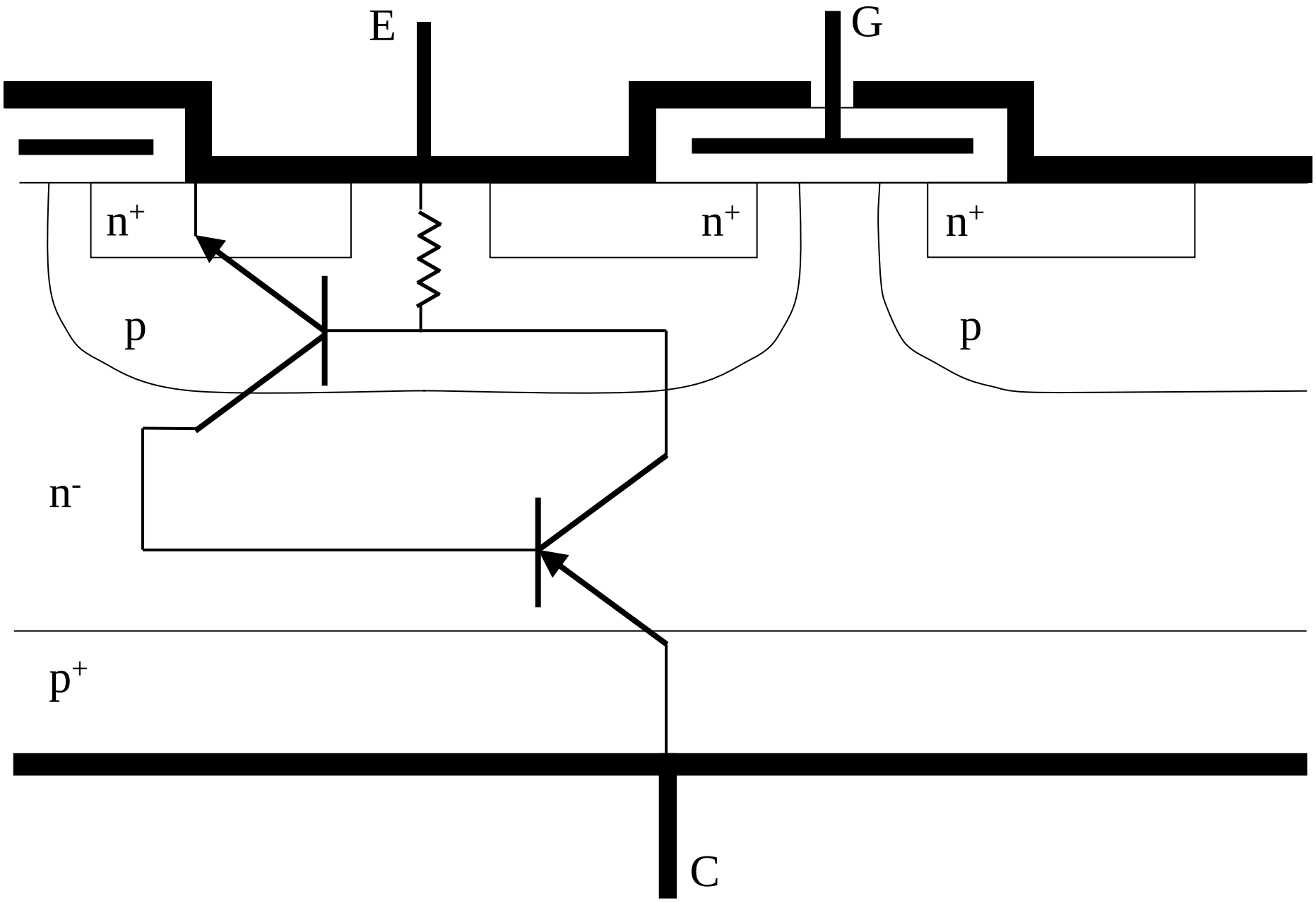

U_{gg}
R_G
-
+
$U_{GE}=0$
$I_C=0$
E
G
n^+
n^+
n^+
p
-
p
J_2
+ $U_{j2} \approx U_d$
n^-
J_1
p^+
Z_L
-
U_d
+
C
$U_{CE} = U_d$
$I_C = 0$

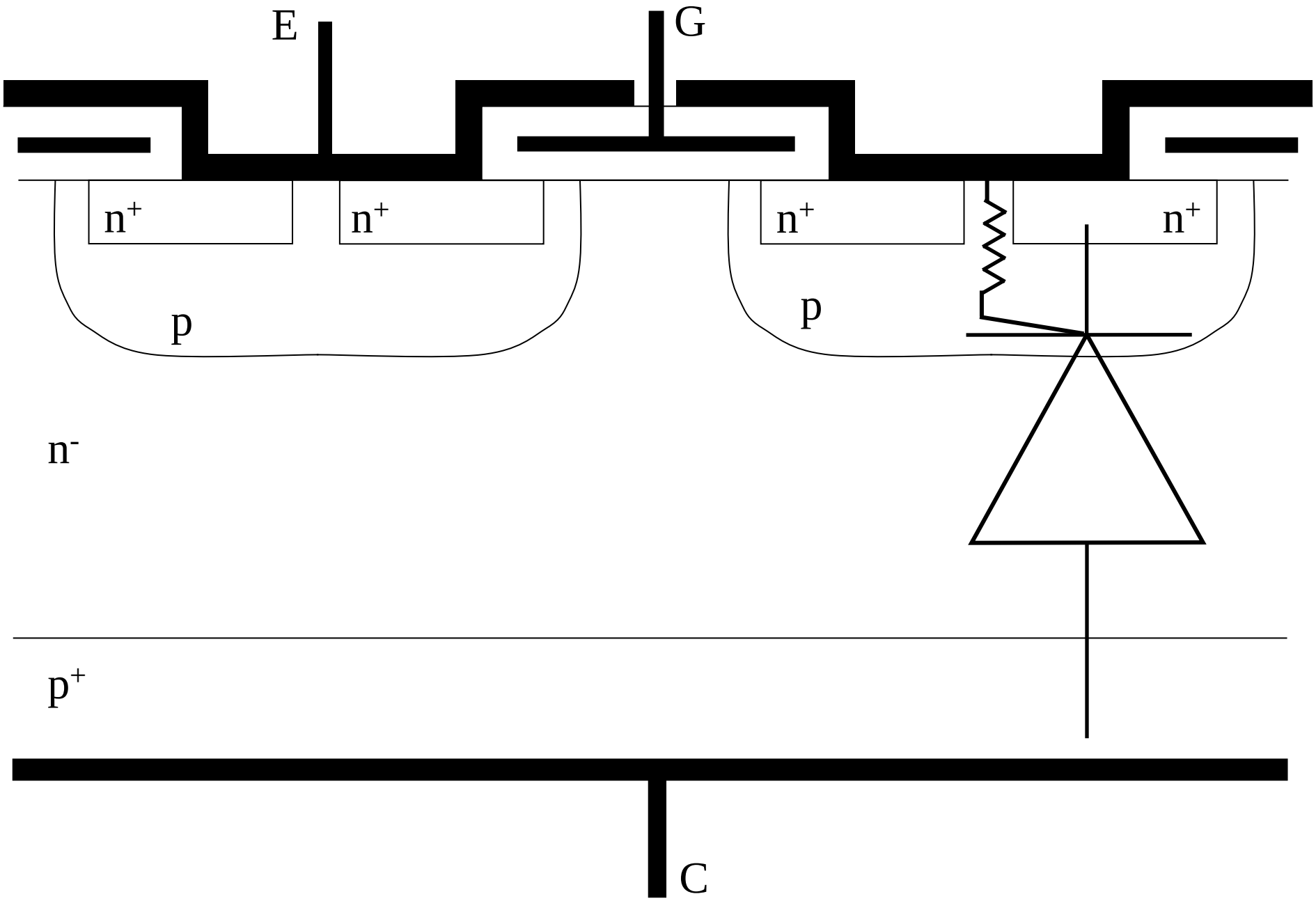

U_{gg}
R_G
-
+
$U_{GE} = U_{gg} (\approx 15V)$
E
G
I_C
canal n
n^+
n^+
n^+
p
p
e^-
e^-
e^-
n^-
J_1
p^+
Z_L
C
-
U_d
+
I_C

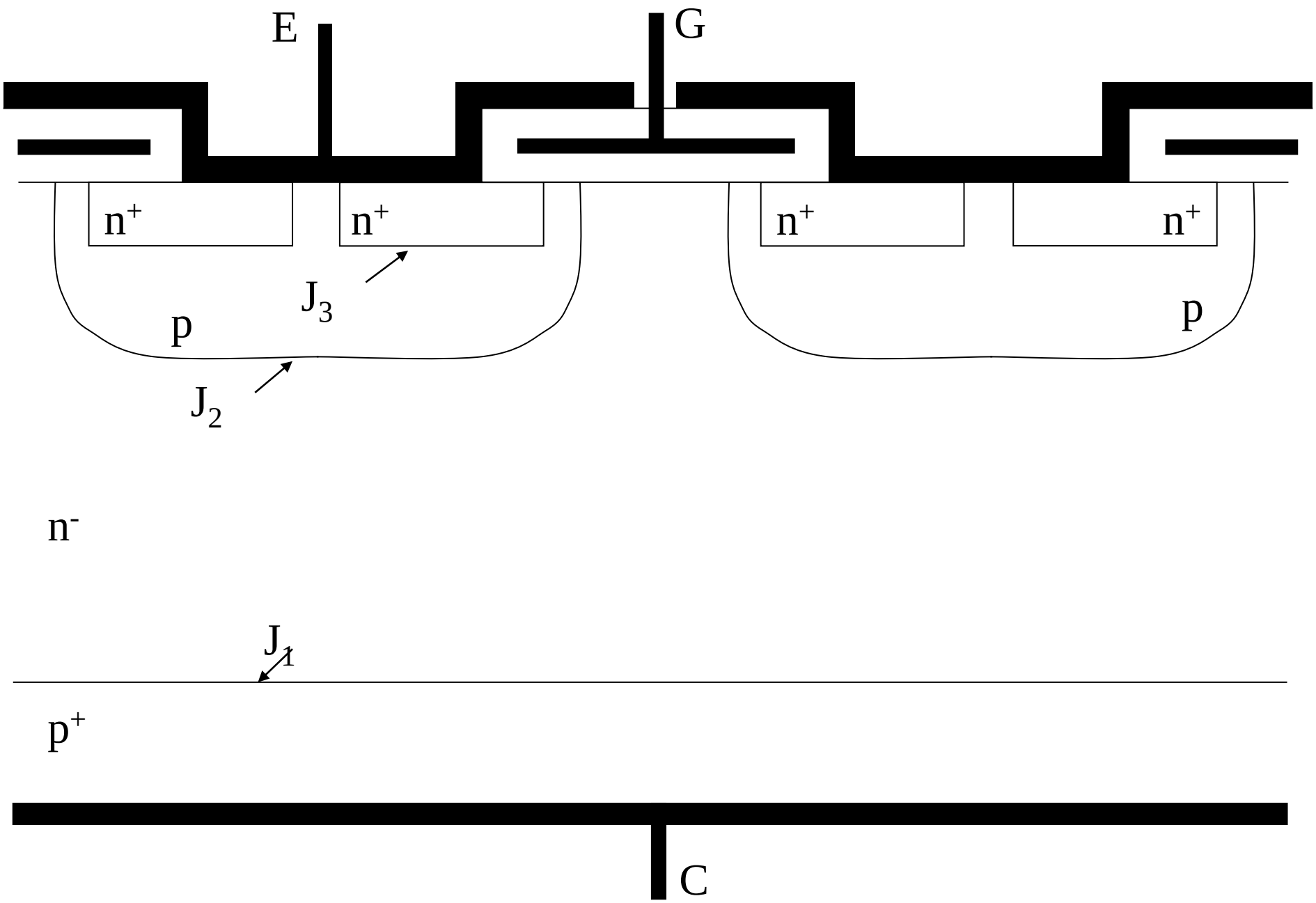

U_{gg}
R_G
-
+
$U_{GE} = U_{gg} (\approx 15V)$
E
G
I_C
canal n
n^+
n^+
n^+
h^+
h^+
p
p
e^-
R
h^+
R
e^-
R
e^-
n^-
p^+
J_1
Z_L
C
-
U_d
+
I_C
R: recombinación
e^-: electrones
h^+: huecos

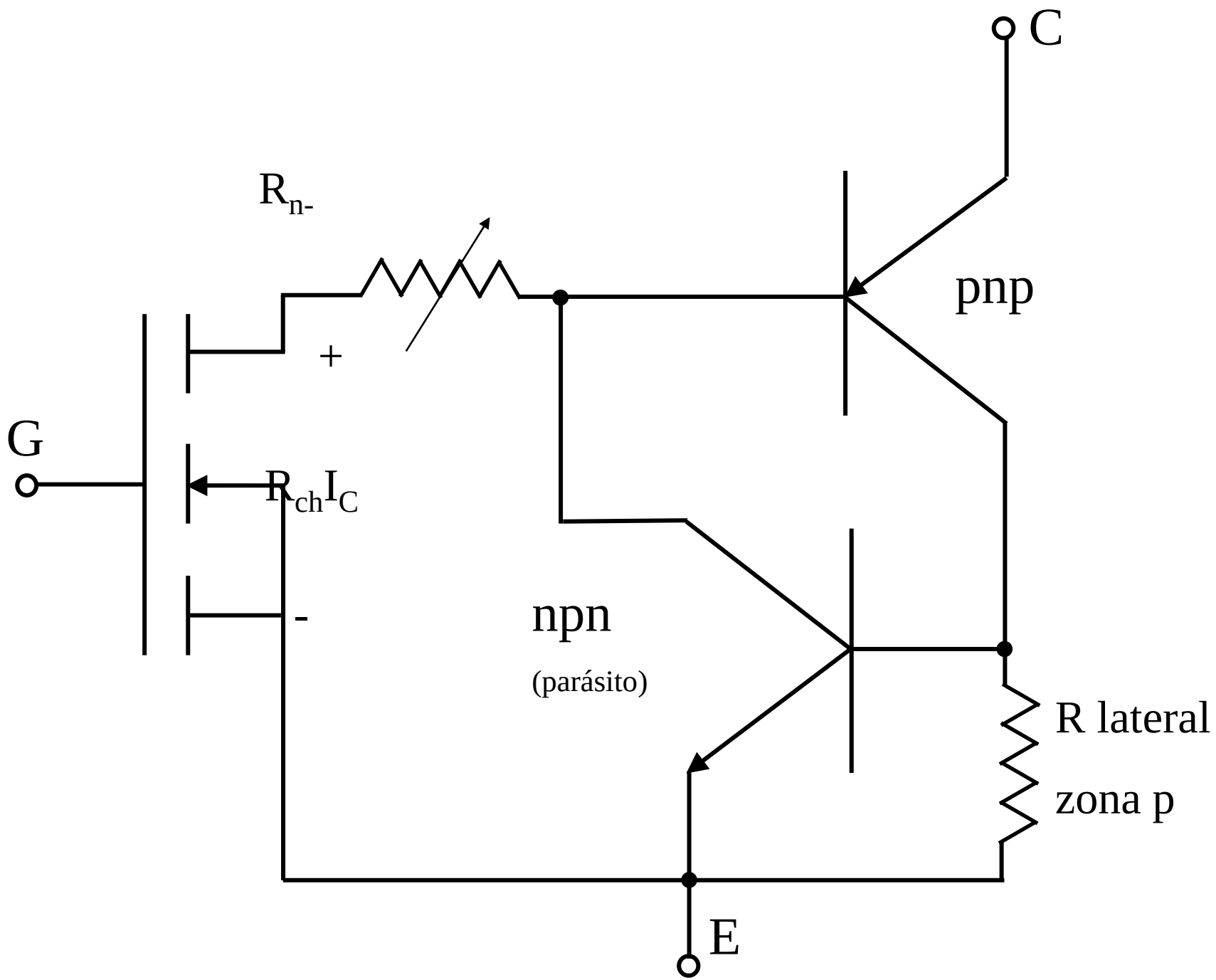

a)
Colector
Gate
Emisor
b)
Colector
Gate
Emisor
c)
Colector
Gate
Emisor

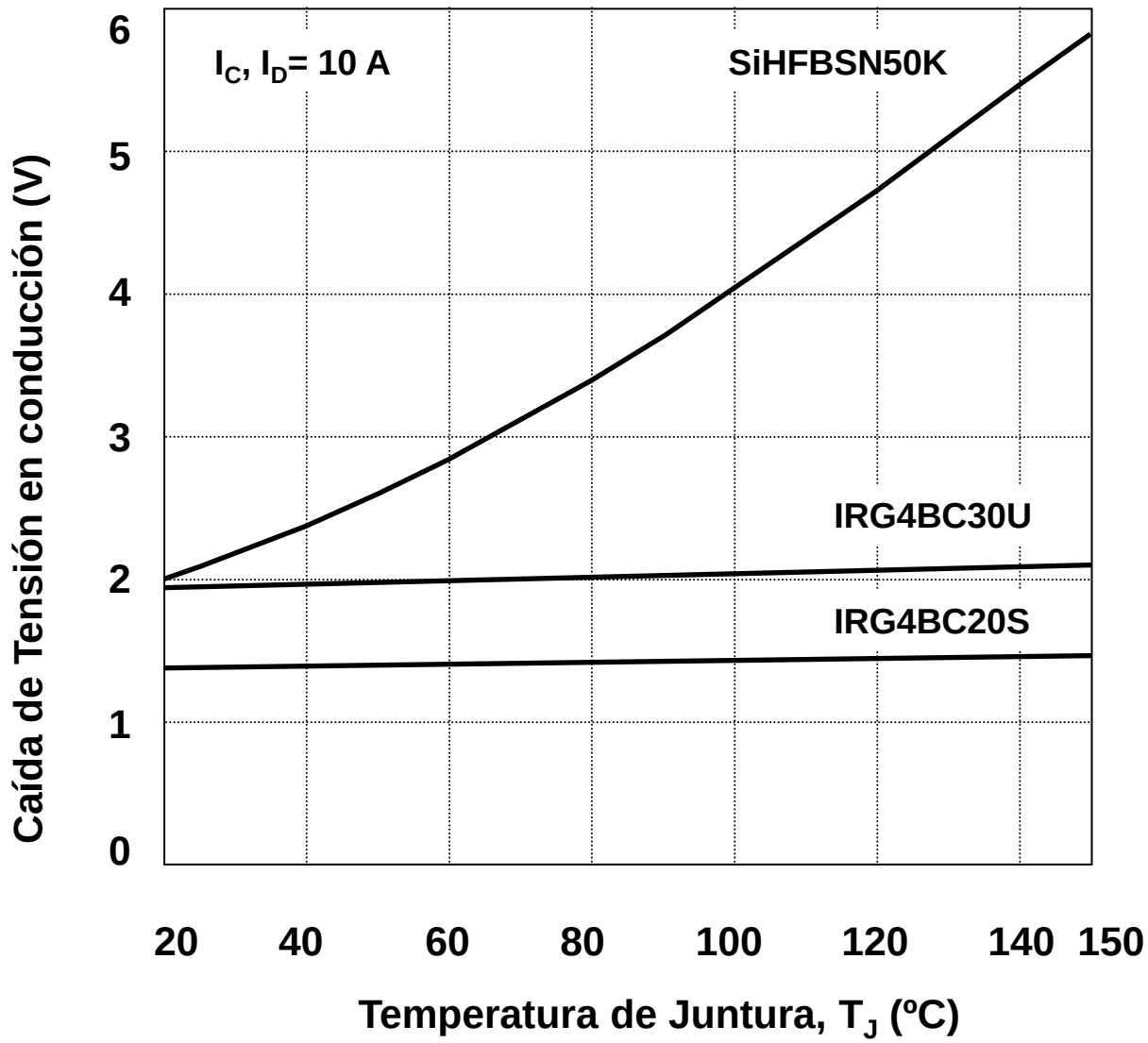

E
R lateral
zona p
G
n+
n+
n+
p
p
n-
p+
C

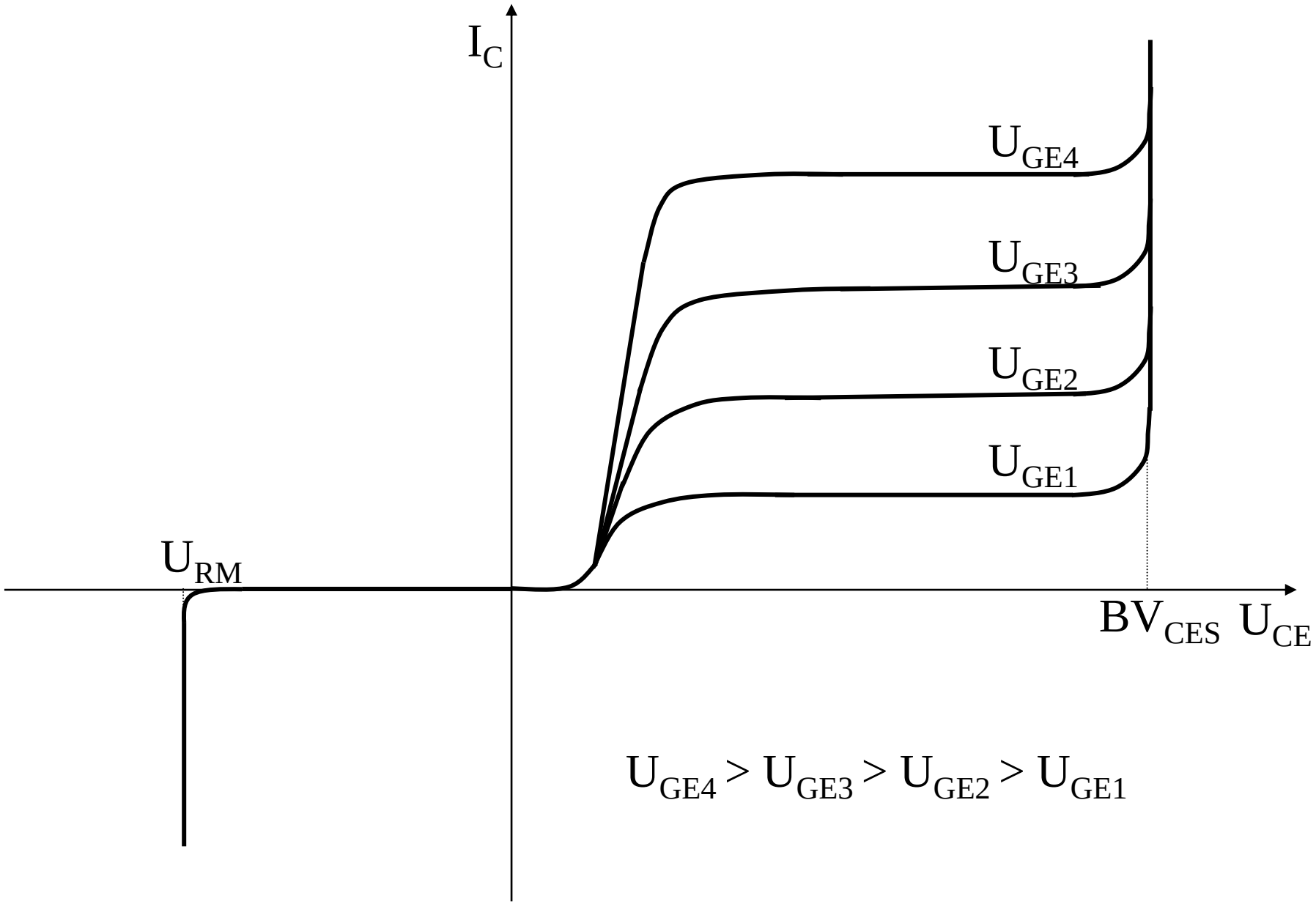

E
G
n+
n+
n+
p
p
n-
p+
C


E
G
n+
n+
n+
n+
p
p
n-
p+
C

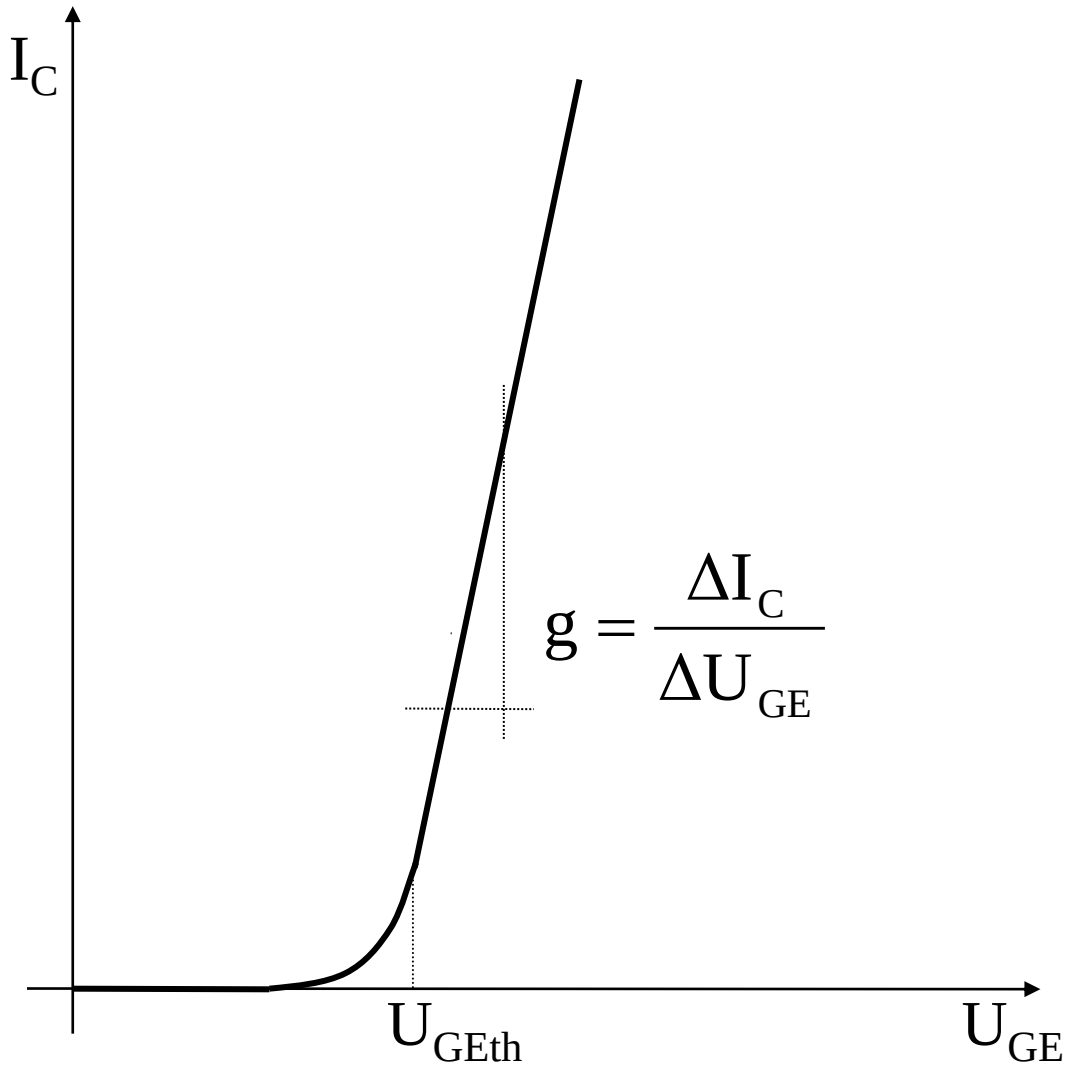

E
G
n+
n+
n+
n+
J3
p
p
J2
n-
J1
p+
C


C
R_{n-}
pnp
+
G
$R_{ch}I_C$
-
npn
(parásito)
R lateral
zona p
E

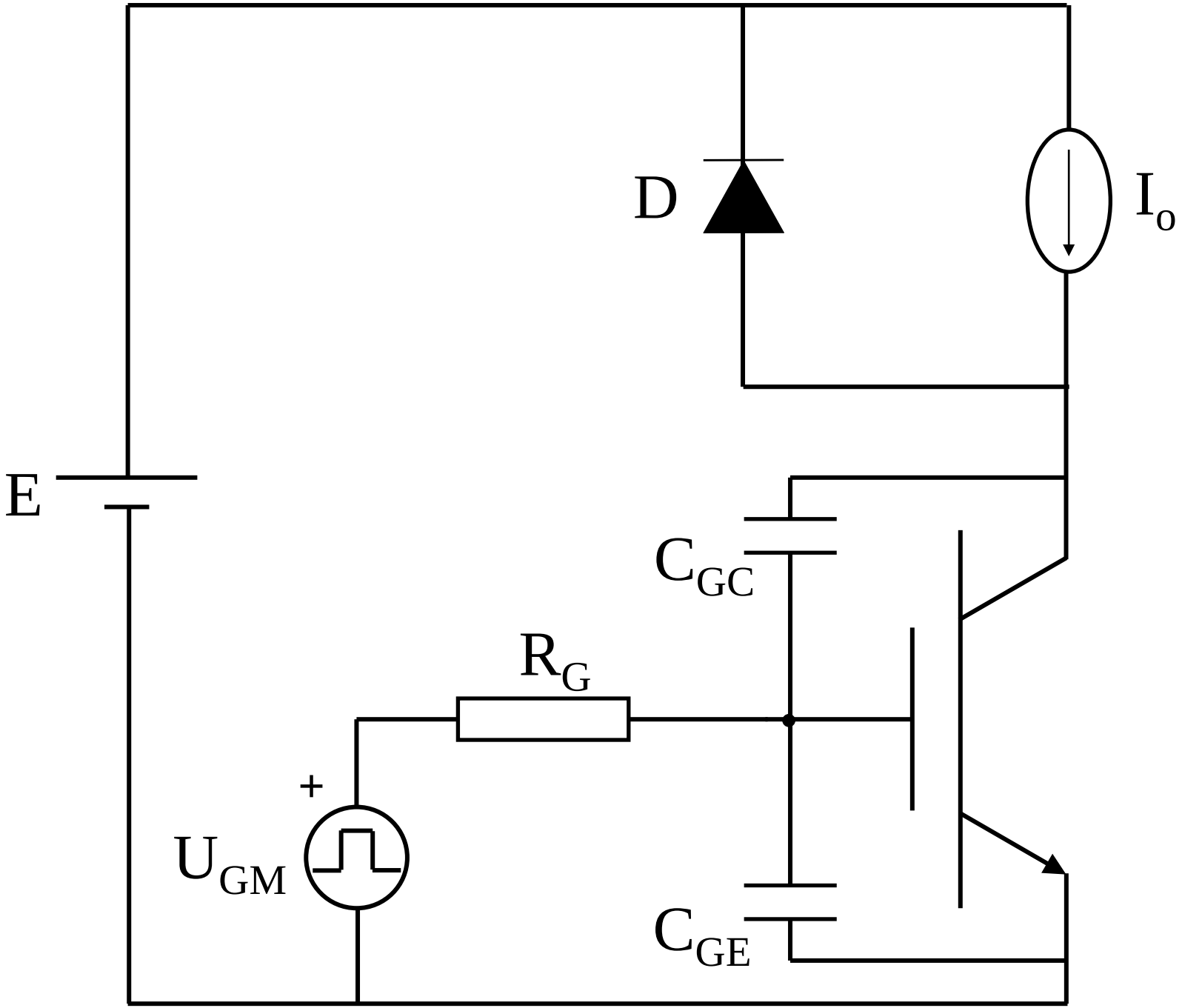

I_C, I_D= 10 A
SiHFBSN50K
IRG4BC30U
IRG4BC20S
Caída de Tensión en conducción (V)
0
1
2
3
4
5
6
20
40
60
80
100
120
140
150
Temperatura de Juntura, T_J (ºC)

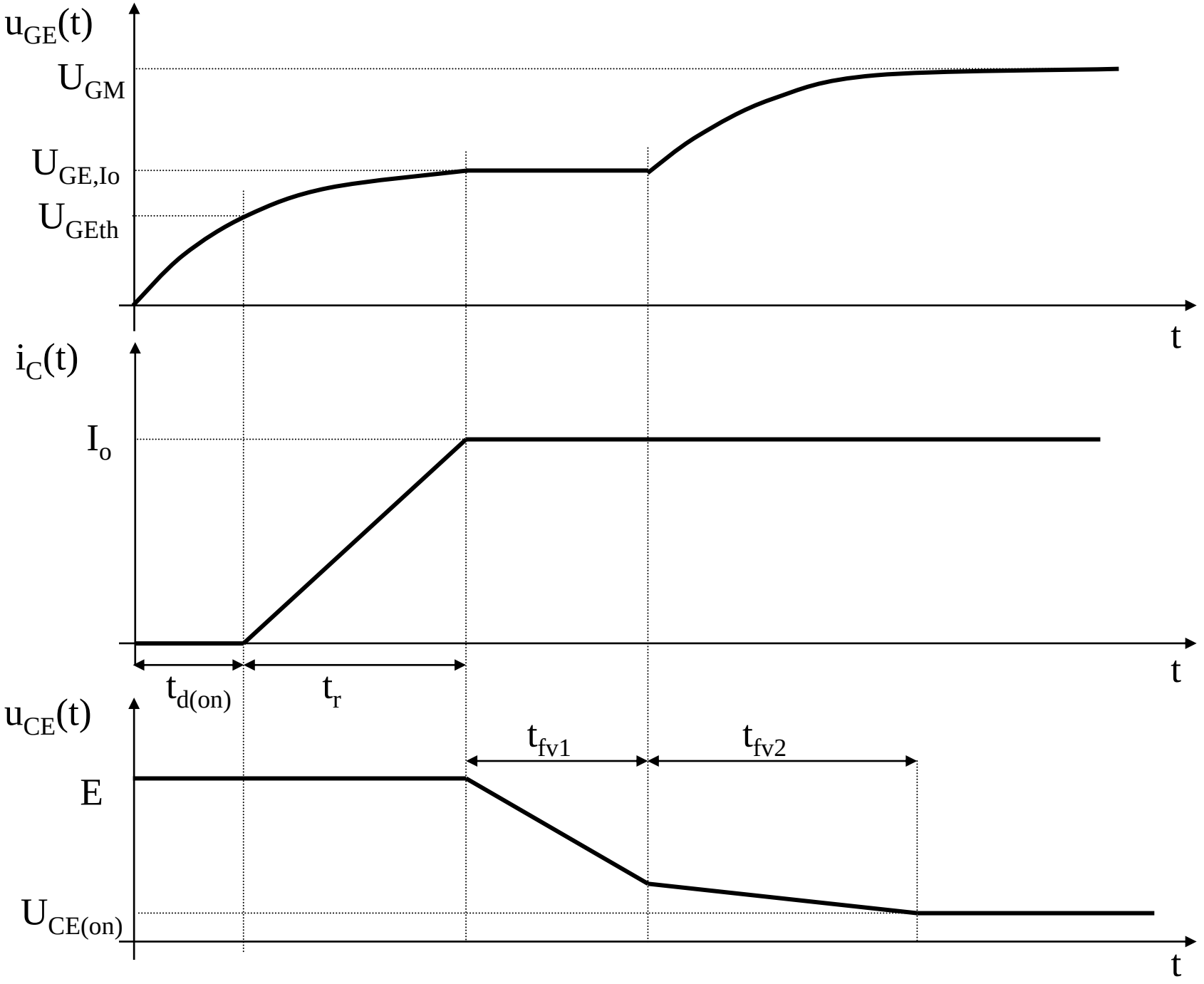


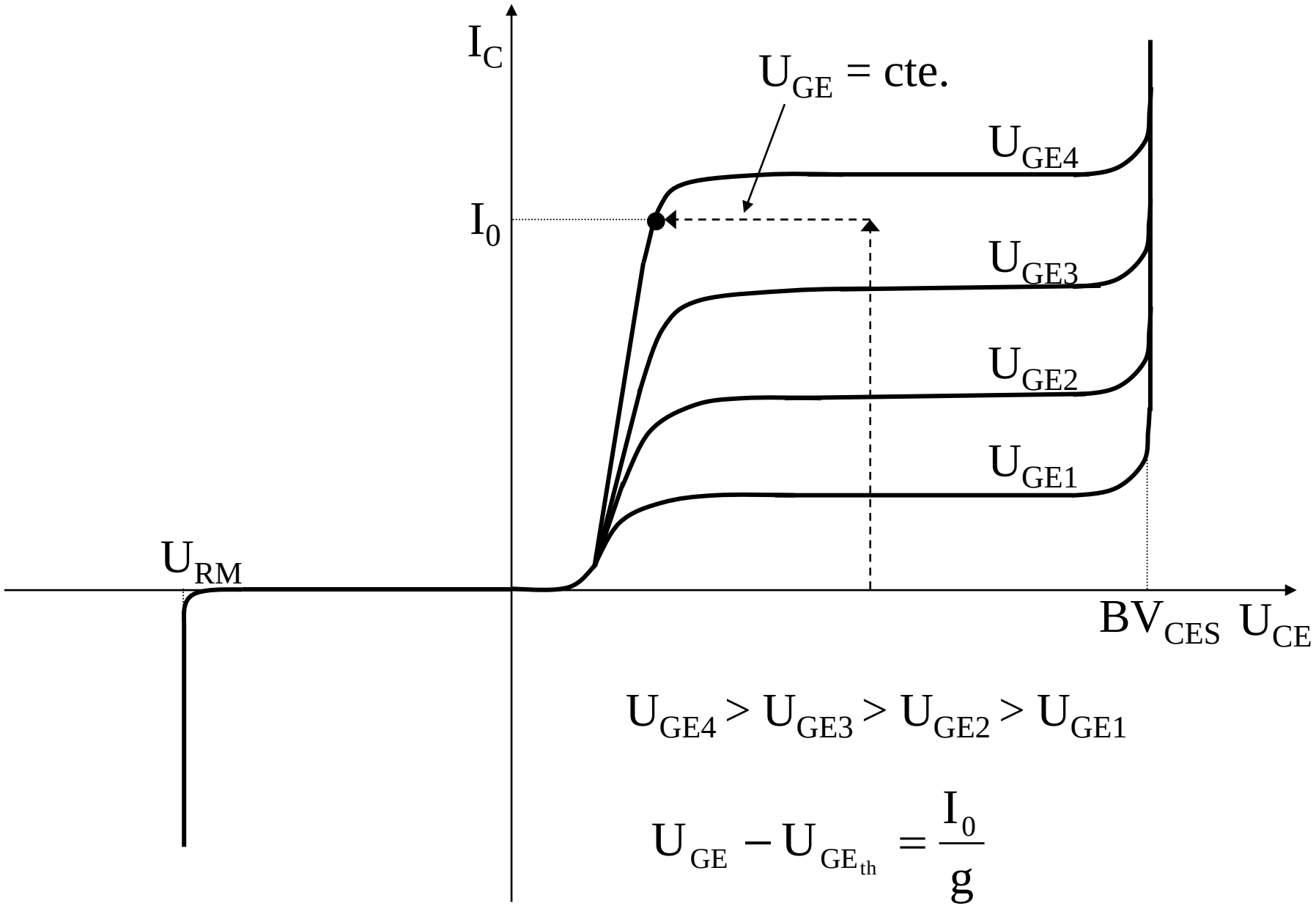
$U_{GE4} > U_{GE3} > U_{GE2} > U_{GE1}$



g = transconductancia

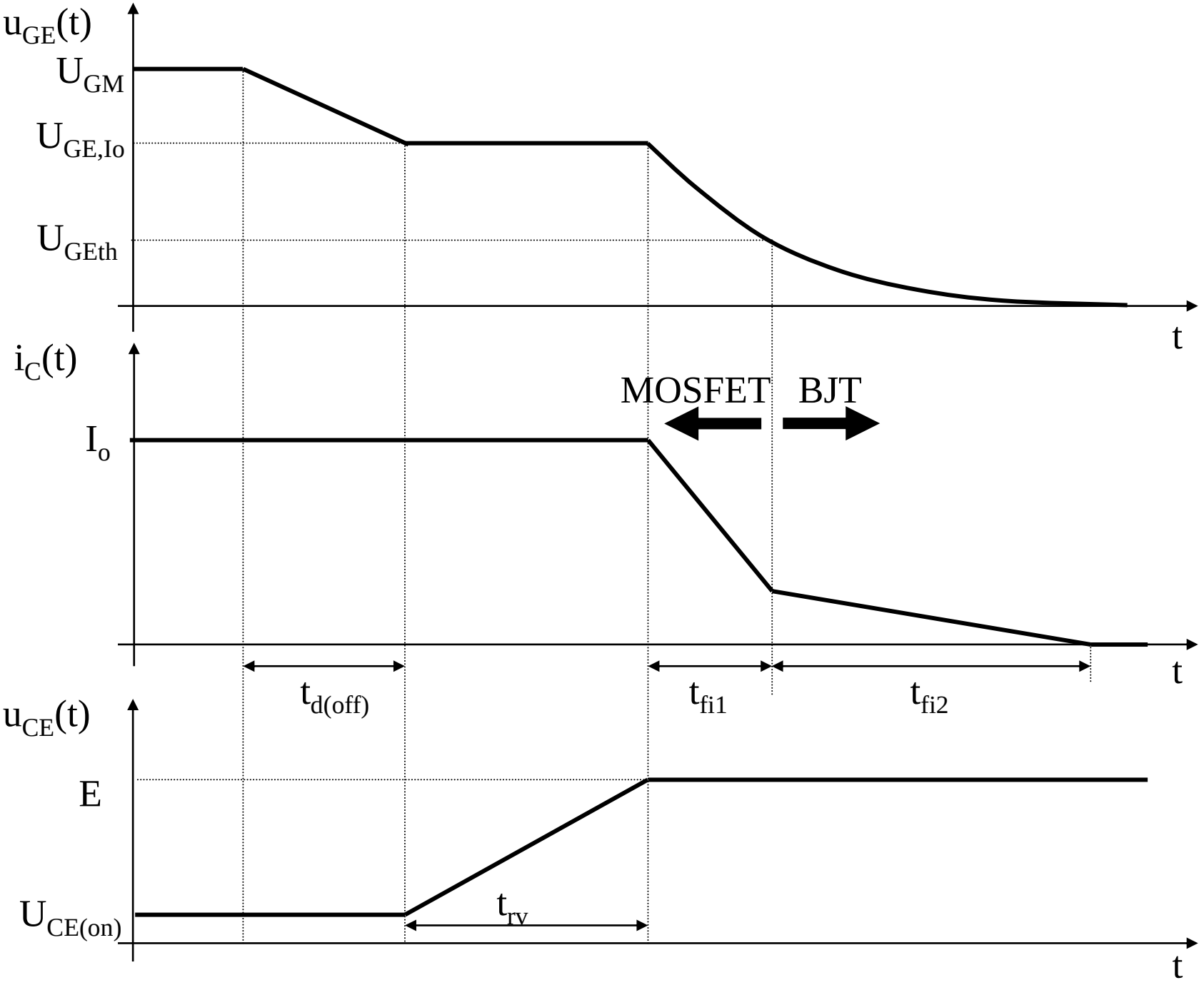

D
I_o
E
C_{GC}
R_G
+
U_{GM}
C_{GE}


$u_{GE}(t)$
U_{GM}
$U_{GE,Io}$
U_{GEth}
t
$i_C(t)$
I_o
t
$t_{d(on)}$
t_r
$u_{CE}(t)$
t_{fv1}
t_{fv2}
E
$U_{CE(on)}$
t



$$U_{GE4} > U_{GE3} > U_{GE2} > U_{GE1}$$

$$U_{GE} - U_{GE_{th}} = \frac{I_0}{g}$$


$u_{GE}(t)$
U_{GM}
$U_{GE,Io}$
U_{GEth}
t
$i_C(t)$
MOSFET
BJT
I_o
t
$t_{d(off)}$
t_{fi1}
t_{fi2}
$u_{CE}(t)$
E
$U_{CE(on)}$
t_{rv}
t